Tektronix®

496/496P
SPECTRUM ANALYZER
WITH OPTIONS

SERVICE VOLUME 1

INSTRUCTION MANUAL

Tektronix®
COMMITTED TO EXCELLENCE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

496/496P
SPECTRUM ANALYZER

WITH OPTIONS

SERVICE VOLUME 1

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

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Product Group 26

Serial Number _____

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SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

In This Manual

This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment

DANGER—High voltage.

Protective ground (earth) terminal.

ATTENTION—refer to manual.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

For detailed information on power cords and connectors, see the General Information and Specifications sections.

Refer cord and connector changes to qualified service personnel.

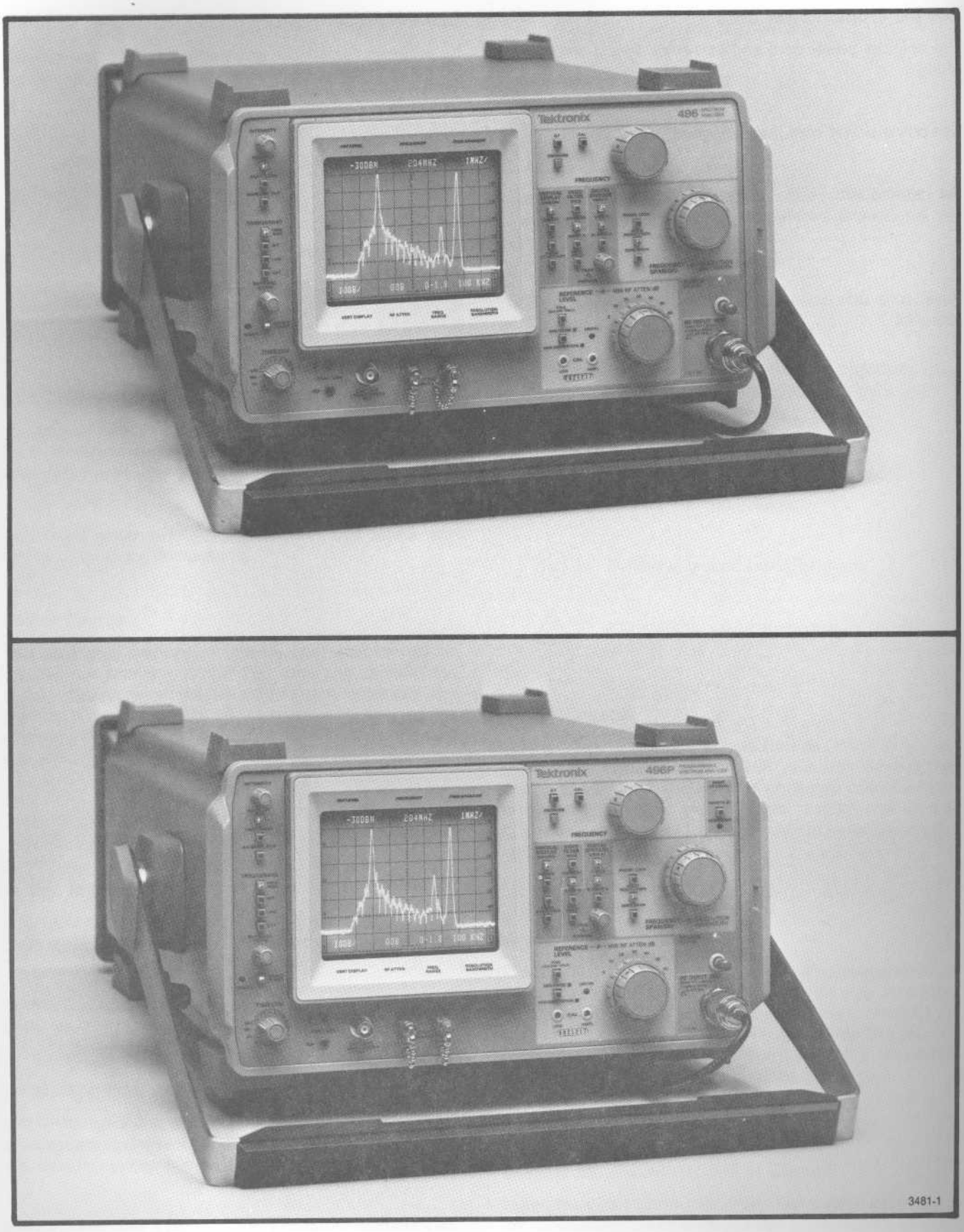
Use the Proper Fuse

To avoid fire hazard, use only the fuse specified in the parts list for your product, and which is identical in type, voltage rating, and current rating.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an atmosphere of explosive gases unless it has been specifically certified for such operation.



The 496/496P Spectrum Analyzer.

GENERAL INFORMATION AND SPECIFICATION

GENERAL INFORMATION

Introduction

The Service manual consists of two volumes that contain information necessary to test, adjust, and service the Portable Rackmount/Benchtop 496/496P Spectrum Analyzer. The intent is to provide as complete information as possible as an aid in servicing this instrument. The Table of Contents at the beginning of Volume 1 lists contents of each section contained within Volume 1.

Change information that involves manual corrections and/or additions pending manual reprint and bind, is located at the back of the Service manual in the CHANGE INFORMATION section.

History information with the updated data is integrated into the text or diagrams when a page or diagram is updated. Original pages are identified by the symbol @, revised pages by a revision date in the lower inside corner of the page. The manual may contain revisions that do not apply to your instrument; however, history information with updated data, is integrated into the text or diagram when the page or diagram is revised.

The person using these instructions should be knowledgeable in digital and analog circuit theory. Circuit analysis is primarily functional. The intent is to provide sufficient information for the technician to isolate the majority of malfunctions to a block of circuitry. Those users with an understanding of logic and analog circuitry should then be able to further isolate the malfunction to a specific component or components.

Most terminology is in accordance with those standards adapted by IEEE. A glossary of terms is provided as an appendix. Abbreviations in the documentation are in accordance with ANSI Y1.1-1972, with exceptions and additions explained in parentheses after the abbreviation. Graphic symbols comply with ANSI Y32.2-1975. Logic symbology is based on ANSI Y32.14-1973 and the manufacturer's data description. A copy of ANSI standards may be obtained from the Institute of Electrical and Electronic Engineers, 345 47th Street, New York, NY 10017.

Product Service

To assure adequate product service and maintenance for our instruments, Tektronix has established Field Offices and Service Centers at strategic points throughout the United States and in countries where our products are sold. Several types of maintenance or repair agreements are available. For example: for a fixed fee, a maintenance agreement program provides maintenance and re-calibration on a regular basis. Tektronix will remind you when a product is due for recalibration and perform the service within a specified time. Contact your local Service Center, representative, or sales engineer for details regarding: Warranty, Calibration, Emergency Repair, Repair Parts, Scheduled Maintenance, Maintenance Agreements, Pickup and Delivery, On-Site Service for fixed installations, and other services available through these centers.

Tektronix emergency repair service provides immediate attention to instrument malfunctions if you are in an emergency situation such as a field trip. Again, contact any Tektronix Service Center for assistance to get you on your way within a minimum of time.

Instrument Construction

The modular construction of the 496/496P instrument provides ready access to the major circuits. Circuit boards that contain sensitive circuits are either mounted on metal extrusions, each of which provides shielding between adjacent modules, or they are mounted within honeycomblike extrusions with a feedthrough connector through the wall of the compartment. Interconnection between boards and assemblies is provided by plugging these boards onto a main mother board. Most adjustments and test points are accessible while the instrument is operational and the modules or assemblies secured in their normal position. Extenders are provided with a Service Kit; see Maintenance section under Service Fixtures and Tools for Maintenance.

@

Any module can be removed without disturbing the structural or functional integrity of the other modules. The extenders allow most circuit board assemblies to function in an extended position for service or adjustment. The circuit boards mounted on the metal extrusion can be removed by removing the securing screws. All other circuit boards (which should require minimal service) are accessible by removing a cover plate.

NOTE

Disassembly of some modules may require special tools and procedures. These procedures will be found in the Maintenance section.

The 1st and 2nd LO phaselock circuits contribute to the 496/496P stability. Circuits are completely rf isolated to ensure spurious free response, yet the close proximity minimizes losses or interactions with other functions. All compartments are enclosed on both sides by metal plates and all interconnections between compartments are made by feedthrough terminals rather than cables. If the compartments are opened, be sure that the shields and covers are properly reinstalled before operating.

Elapsed Time Meter

A 5000 hour elapsed time indicator, graduated in 500 hour increments, is installed on the Z Axis/RF Interface circuit board. This provides a convenient way to check operating time. The meter on new instruments may indicate from 200 to 300 hours elapsed time. Most instruments go through a factory burn-in time to improve reliability. This is similar to using aged components to improve reliability and operating stability.

Changing Power Input Range

The following procedures describe how to set the input power range.

a. Disconnect the power plug and remove the cover.

b. Remove the access plate at the upper left corner (viewed from the rear) of the power module.

c. Shift plug P1029 to the appropriate pins on J1029 as indicated by the silk screen nomenclature. Replace the access plate.

NOTE

The earlier version power supply module did not have this access plate. To access P1029 proceed as follows:

1) Set the instrument on its face and remove the four screws that hold the power supply module to the side rails. Lift the module off the instrument.

2) Remove the top and bottom screws then the side screw that holds the two sections of the power supply module together. Separate the two sections to expose the power supply circuit board.

3) Shift the plug P1029 (upper left corner) to the appropriate pins on J1029. Re-install the two sections and the power supply module.

d. Remove the input power specification plate over the input fuse on the back panel. Turn the plate over and reinstall so the exposed information on power specifications is correct.

e. Change the input fuse to the new value specified on the information plate.

f. Replace the cover and the power cord; then connect the instrument to the appropriate power source.

NOTE

The power cord supplied with the instrument and instrument power voltage requirements depend on the available power source (see the Specification part of this section for power cord options).

Replacing Fuses

Besides the input (back panel) fuse, the 496/496P power module has five fuses for the dc supplies (+300 V, F3014; +100 V, F1034; +17 V, F1014; +9 V, F1031; −7 V, F1011). Access to these fuses can be gained by removing the access plate at the upper right corner of the power module, or by separating the two sections as described for changing the input power range. Fuses are identified with stamped circuit numbers on the circuit board.

Selected Components

Some components, such as microcircuits, are selected to meet Tektronix specifications. These components are indicated in the parts list and carry a Tektronix Part Number under the Mfr. Part Number column.

Selected value components that compensate for parameter differences between active components are identified on the circuit diagram and in the parts list as a "SEL" value. The component description lists either the nominal value or a range of value. If the procedure for selection is not obvious, such as setting the gain or response of a stage, the criteria for selection is explained in the Calibration or Maintenance section of the manual. Where the selection procedure is obvious, such as establishing the frequency of an oscillator, no procedure is given.

Component Circuit Numbering Scheme

In this instrument, circuit numbers were assigned according to the components physical location on the board. For example, a component such as a resistor, located within row 2 column 08, is R2080. The fourth digit of the number is an expander used to designate two or more common components within a given grid, such as R2080, R2082, etc.

Chassis mounted components are assigned a three digit number to help identify their location.

The Replaceable Electrical Parts list prefixes these circuit numbers with an assembly number. R2080, on assembly A20, becomes A20R2080. Assembly and subassembly numbers are assigned in numerical order by location within the instrument.

Firmware Version and Error Message Readout

This feature of the 496/496P provides readout of the firmware version when the power on/off is cycled. During initial power-up cycle, the firmware version flashes on screen for approximately two seconds. The Replaceable Electrical Parts list section, under Memory Board (A54), lists the ROM's and their Tektronix part number for each firmware version.

An additional feature is error message readout. The following is a list of these messages and their meaning.

Error No.	Meaning
57	Tune routine failed in carry from lower DAC.
58	Failed to phaselock.
59	Lost lock.
60	Failed to recenter when phaselock cancelled or when going to an unlocked span.

Rackmount/Benchtop Versions

The rackmount version of the 496/496P Spectrum Analyzer is the 496/496P in a rackmount cabinet. Access to all front panel connectors is provided with Option 31 of this version. Additional cooling is provided and a front panel accessories drawer in the cabinet provides storage for most accessories. The benchtop version is the same as the rackmount with the exception of the side rails.

SPECIFICATION

The following list of instrument characteristics and features apply to the basic 496/496P Spectrum Analyzer after a 30-minute warmup, except as noted. Changes to the basic specifications due to the addition of options follow the basic listings.

Differences in the electrical and environmental characteristics for the rackmount/bench versions of the 496/496P are described in the Rackmount/Benchtop section of this manual. Refer to section 6 for this information.

The Performance Requirement column describes the limits of the characteristic, and the Supplemental column describes features and typical values or information that may be useful to the user. Procedures to verify performance requirements are provided in the Calibration section of the Service instructions. The Performance Check procedures require sophisticated equipment as well as technical expertise to perform.

The Operators Manual contains a procedure that checks all functions of the 496/496P. This check is recommended for incoming inspections to verify that the instrument is functioning properly.

Table 1-1
ELECTRICAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Information
	FREQUENCY RELATED	
Center Frequency		
Range		0 MHz to 1800 MHz
Accuracy after 1 hour warmup over CF range.	±(5 MHz + 20% of Span/Div)	
TUNE command accuracy (after 1 hour warmup–applies only to 496P under remote control)		
Span/Div >50 kHz	±7% of frequency or ±75 kHz, whichever is greater	
Span/Div ≤50 kHz	±7% of frequency or ±100 Hz, whichever is greater	
Repeatability of frequency setting (ambient temperature change must be ≤10°C–applies only to 496P under remote control)		±(2 MHz +10% of Span/Div) or ±(0.1% of frequency +10% of Span/Div of previous settings to the same frequency, whichever is greater
Delta Frequency readout accuracy after 1 hour warm up, Span/Div ≤50 kHz.	±5% of the Delta Frequency readout	For Span/Div >50 kHz, readout is in MHz; for Span/Div ≤50 kHz, readout is in kHz
Readout Resolution		1 MHz
Residual FM (short term)		
Phaselock On	≤10 Hz p-p over 20 mS	Video Filter Off
Phaselock Off	≤1 kHz p-p over 20 mS	Video Filter Off
Frequency Drift Excursion (at constant temperature and fixed center frequency)		
Phaselock On		
After 30 minute warm up	≤3.3 kHz in 10 min	≤20 kHz in 1 hour
After 1 hour warm up	≤330 Hz in 10 min	≤2 kHz in 1 hour
Phaselock Off		
After 1 hour warm up	≤33 kHz in 10 min	≤200 kHz in 1 hour
"Static" Resolution Bandwidth (–6 dB)	30 Hz, then 100 Hz to 1 MHz in decade steps, plus an AUTO position; resolution bandwidth is within 20% of selected bandwidth	In AUTO position the bandwidth is selected by an internal computer, depending on the setting of the Span/Div, Time/Div, Vertical Display, and Video Filter controls; the Span/Div controls the bandwidth when both Time/Div and Resolution Bandwidth are set to AUTO
Shape Factor (60 dB/6 dB)	7.5:1 or less; 15:1 or less for 30 Hz Resolution Bandwith	

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
Phaselock Noise Sidebands	At least −75 dBc at 30 times the Resolution Bandwidth offset from the Center Frequency (−70 dBc for 100 Hz Resolution Bandwith or less)	
Pulse Stretcher Fall Time		30 μs/division, ±50%
Video Filter		
Narrow		Reduces video bandwidth to approximately 1/300th of selected Resolution Bandwidth and 1/100th for 30 Hz Bandwidth
Wide		Reduces video bandwidth to approximately 1/30th of selected Resolution Bandwidth and 1/10th for 30 Hz Bandwidth
Frequency Span/Div		
Range		From 50 Hz/Div to 100 MHz/Div in a 1-2-5 sequence
MAX Span		When selected, the entire effective frequency range is scanned and displayed
Zero Span		When selected, the horizontal axis of the crt is calibrated in time (instead of frequency); the span/div readout is changed to time/div
Accuracy	Within 5% of the selected Span/Div over the center eight divisions of the ten-division crt display	
Frequency Response and Display Flatness		
1 kHz to 1.8 GHz	±1.5 dB about the mid-point (mean) between the two extremes	Frequency response is measured with RF attenuation ≥10 dB; the response figure includes the effects of input vswr, mixer, and gain variations Variations in display flatness contribute about 1 dB to the response figure
AMPLITUDE RELATED		
Vertical Display Modes		10 dB/div, 2 dB/div, Linear, and ΔA.
Reference Level (full screen, top of graticule)		
Range		−123 dBm to +40 dBm (+40 dBm includes a maximum safe input of +30 dBm and 10 dB of IF gain reduction) for 10 dB/div and 2 dB/div log modes; 20 nV/div to 2 V/div (1 W maximum safe input) in LIN Mode

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
Steps		10 dB, 1 dB, and 0.25 dB for relative (Δ) measurements in log mode; 1-2-5 sequence and 1 dB equivalent increments in LIN mode
Accuracy		Accuracy is a function of changes in RF Attenuation, Resolution Bandwidth, Display Mode, and Reference Level (see amplitude accuracies of these functions); the RF attenuator steps 10 dB for reference level changes above −30 dBm (−20 dBm when MIN NOISE is active) unless MIN RF ATTENUATION is greater than normal. The IF gain increases 10 dB for each 10 dB Reference Level change below −30 dBm (−20 dBm when MIN NOISE is active)
Display Dynamic Range		80 dB at 10 dB/div, 16 dB at 2 dB/div, and 8 divisions in LIN mode
Accuracy	±1.0 dB/10 dB to a maximum cumulative error of ±2.0 dB over the 80 dB window and ±0.4 dB/2 dB to a maximum cumulative error of ±1.0 dB over the 16 dB window; LIN mode is 5% of full scale	
RF Attenuator		
Range		0 to 60 dB in 10 dB steps
Accuracy 1 kHz to 1.8 GHz	Within 0.3 dB/10 dB to a maximum of 0.7 dB over the 60 dB range	
IF Gain		
Range		93 dB of gain increase, 10 dB of gain decrease (with MIN NOISE activated) in 10 dB and 1 dB steps
Accuracy	Gain steps are monotonic (same direction) with the following limits: Within 0.2 dB/dB to a maximum of 0.5 dB/9 dB, except at the decade transitions of −19 to −20 dBm, −29 to −30 dBm, −39 to −40 dBm, −49 to −50 dBm, −59 to −60 dBm, and −69 to −70 dBm, where an additional 0.5 dB can occur for a total of 1.0 dB per decade. Maximum deviation over the 90 dB range is within ±2 dB.	Gain Variation between Resolution Bandwidths
Gain Variation between Resolution Bandwidths	<0.5 dB	Measured at −20 dB REF LEVEL and 10 dB RF ATTEN

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
Differential Amplitude		ΔA mode provides differential measurement in 0.25 dB increments
Accuracy		dB difference / Steps / Error 0.2 dB / 1 / 0.05 dB 2.0 dB / 8 / 0.4 dB 10.0 dB / 40 / 1.0 dB 50.0 dB / 200 / 2.0 dB Within the reference level range of of −123 dBm to +30 dBm
Range		From 10 dB above to 40 dB below the reference level established when the ΔA mode was activated Do not use the ΔA mode outside the +30 dBm to −123 dBm reference level range; total range is at least 50 dB
Equivalent Input Noise Sensitivity Resolution		
Bandwidth		
30 Hz	−126 dBm	
100 Hz	−123 dBm	
1 kHz	−115 dBm	
10 kHz	−105 dBm	
100 kHz	−95 dBm	
1 MHz	−85 dBm	
Spurious Response		
Residual (no input signal, referenced to mixer input)	−100 dBm or less	
Third-order Intermodulation Distortion (Min Distortion mode)	At least −70 dBc below any two on-screen signals	
Harmonic Distortion (cw signal, Min Distortion mode)	At least −60 dBc for a full-screen signal	
Zero Frequency Spur (referenced to input mixer)	−20 dBm or less	
INPUT SIGNAL CHARACTERISTICS		
RF INPUT		Type N female connector
Input Impedance		50 Ω; vswr 1.3:1 (typically 1.2:1) with 10 dB or more RF attenuation

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
Input Level		
Optimum level for linear operation		−30 dBm referred to input mixer; full screen not exceeded and MIN Distortion control setting
1 dB compression point	−19 dBm, no RF attenuation	
Maximum input level		
RF attenuation at 0 dB		+30 dBm typical (limited by mixer burnout)
With 20 dB or more RF attenuation		+30 dBm (1 W) continuous, 75 W peak, pulse width 1 μs or less with a maximum duty factor of 0.001 (attenuation limit) **NEVER apply Dc to the RF INPUT**
LO Emissions (referenced to input mixer)	Less than −70 dBm to 18 GHz	
EXT IN HORIZ/TRIG		Dc coupled input for horizontal drive; ac coupled for trigger signal
Input voltage Range		
Sweep		0 to 10 V, ±10% (dc + peak ac) for full screen deflection
Trigger	1.0 V peak (minimum) Frequency range 15 Hz to 1 MHz	Maximum input: 50 V (dc + peak ac) Maximum ac input: 30 V rms to 10 kHz, then derate linearly to 3.5 V rms at 100 kHz and above; pulse width is 0.1 μs minimum
ACCESSORY (J104)		This connector is for future applications
OUTPUT SIGNAL CHARACTERISTICS		
Calibrator (CAL OUT)	−20 dBm, ±0.3 dB at100 MHz, ±1.7 kHz	Comb markers are provided for frequency and span calibration
1st and 2nd LO		Provides access to the output of the respective local oscillators (1st LO +7.5 dBm minimum to a maximum of +15 dBm, 2nd LO −16 dBm minimum to a maximum of +15 dBm) These ports must be terminated in 50 Ω at all times
Vertical	Provides 0.5 V, ±5% of signal per division of video above and below the centerline	Source impedance approximately 1 kΩ

Table 1-1 (cont)

Characteristic	Performance Requirement	Supplemental Information
Horiz Out	Provides 0.5 V either side of center. Full range −2.5 V to +2.5 V, ±10%	Source impedance approximately 1 kΩ
Pen Lift		TTL compatible, nominal +5 V to lift pen
IF Out		Output of the 10 MHz IF level is approximately −16 dBm for a full screen signal at −30 dBm input reference level Nominal impedance 50 Ω
IEEE Std 488-1978 Port (GPIB) 496P		In accordance with 488 standard
Probe Power		Provides operating voltage (+5 V, +15 V, −15 V, and Ground) for active probes (see Fig. 1-1)
GENERAL CHARACTERISTICS		
Sweep		
Sweep Time	20 μs/div to 5 s/div in 1-2-5 sequence (10 s/div in Auto)	Triggered, auto, manual, and external
Accuracy	±5%	
Triggering	≥2.0 division of signal for internal; lowest external trigger level is 1 V peak	Internal, external, free run, and single sweep; external is ac coupled (15 Hz to 1 MHz) Largest allowable external trigger is 50 V (dc + peak ac)
Crt Readout		Displays: reference level, frequency, frequency span/div, vertical display, RF attenuation, and resolution bandwidth

Characteristics	Description
POWER REQUIREMENTS	
Input Voltage	90 to 132 Vac or 180 to 250 Vac, 48 to 440 Hz
Power	210 Watts maximum, 3.2 amperes at 115 V and 60 Hz
Leakage Current	5 mA peak

NOTE

If power to this instrument is interrupted, it may be necessary to re-initialize the microcomputer; when power is restored, turn the POWER switch Off for 5 seconds then back On.

PROBE POWER. The PROBE POWER connector on the rear panel of this instrument provides operating power for active probe systems. It is not recommended that these connectors be used as a power source for applications other than the compatible probes or other accessories which are specifically designed for use with this source.

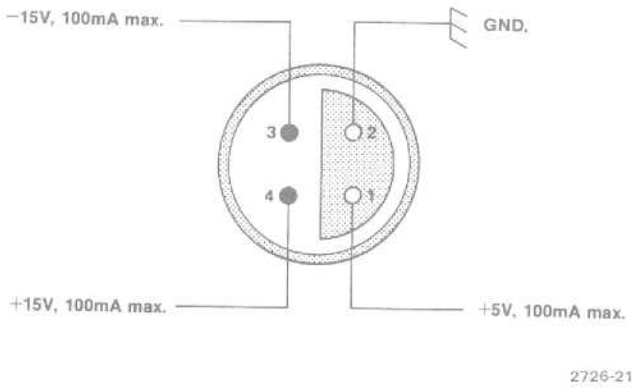


Fig. 1-1. Probe power connector pin out.

Table 1-2
ENVIRONMENTAL CHARACTERISTICS

Meets MIL T-28800B, type III, class 3, style C specifications as follows:

Characteristic	Description
Temperature	
Operating and Humidity	−15°C to +55°C/95% (+5%,−0%) relative humidity
Non-operating	−60°C to +75°C

NOTE

After storage at temperatures below the operating range, the microcomputer may not initialize on power-up. If so, allow the instrument to warm up for 15 minutes and re-initialize the microcomputer by turning the POWER Off for 5 seconds then back On.

Altitude	
Operating	4,500 m (15,000 feet)
Non-operating	12,000 m (40,000 feet)
Humidity (Non-operating)	Five cycles (120 hours) of MIL-Std-810
Vibration	Method 514 Procedure X (modified)
Operating	Resonant searches along all three axes at 0.025 inch p-p, frequency varied from 10—55 Hz for 15 minutes All major resonances must be minimum per axis plus dwell at reasonant frequency of 55 Hz for 10 minutes minimum per axis Instrument is secured to vibration platform during test. Total vibration time minutes

Table 1-2 (cont)

Characteristic	Description	
Shock (Operating and Non-operating)	Three shocks of 30 g, one-half sine,11 ms duration, each direction along each major axis (total of 18 guillotine-type shocks	
Transit drop (free fall)	12 inch, one per each of six faces and eight corners	
Electromagnetic Interference (EMI)	Within limits described in MIL-Std-461	
	Test Method	**Remarks**
Conducted emissions	CE01	10 kHz to 20 kHz only
	CE03 20 kHz to 50 Mhz on power leads	Except 30 to 35 kHz, relaxed by 15 dB
Conducted susceptibility	CS01 30 Hz to 50 kHz on power leads	Full limits
	CS02 50 kHz to 400 MHz on power leads	Full limits
	CS06 Spikes on power leads	Full limits
Radiated emissions	RE01 30 Hz to 30 kHz magnetic field	Relaxed by 10 dB for fundamental, 2nd, and 3rd harmonic of power line
	RE02 14 to 10 GHz	Full limit
Radiated susceptibility	RS01 30 Hz to 30 kHz magnetic field	Full limit
	RS03 Up to 1 GHz	Full limit

Table 1-3
PHYSICAL CHARACTERISTICS

Characteristics	Description
Weight (standard accessories and cover except manuals)	42 pounds (19.6 kg) maximum
Dimensions (Fig. 1-2)	
Without front cover, handle, or feet	6.9 x 12.87 x 19.65 inches (17.5 x 32.69 x 49.91 cms)
With front cover, handle, and feet	9.15 x 15.05 x 23.1 inches (handle folded back over instrument), 28.5 inches (handle fully extended)

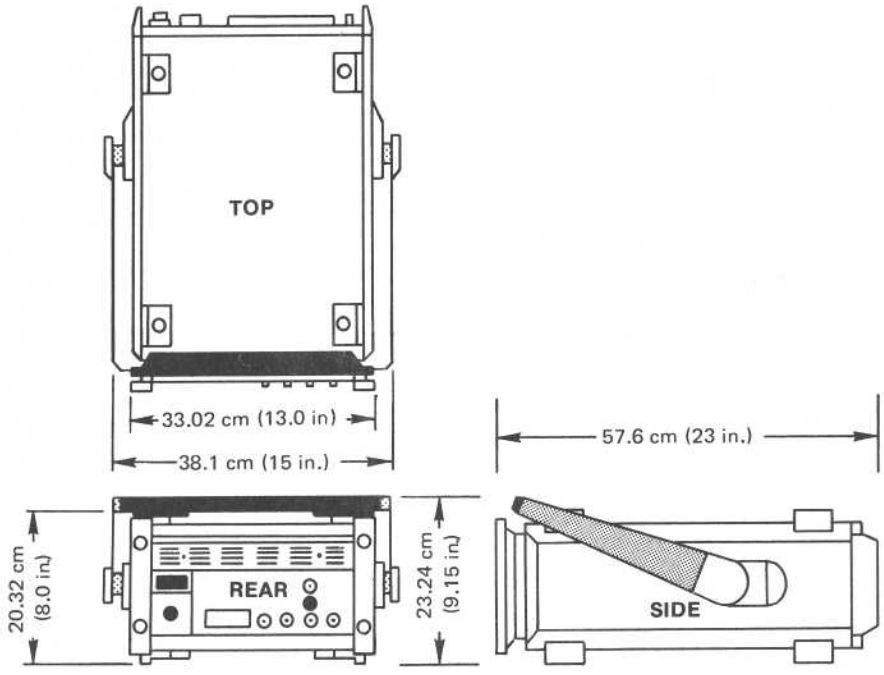


Fig. 1-2. Dimensions.

ACCESSORIES

See Accessories page following Replaceable Mechanical Parts list, Volume 2.

OPTIONS

Options available for the 496/496P and their resultant changes to the specifications are listed below. Options are factory installed at the time of the initial order. Contact your local Tektronix Field Office for additional information.

OPTION 30

Rackmount version of 496/496P Spectrum Analyzer.

OPTION 31

Rackmount version of 496/496P with cables from front panel connectors to connectors at the back of the cabinet.

OPTION 32

Benchtop version of 496/496P Spectrum Analyzer.

OPTIONS FOR POWER CORD CONFIGURATION

Tektronix has implemented options that provide internationally approved power cord and plug configurations. These are shown and illsutrated in Fig. 1-3.

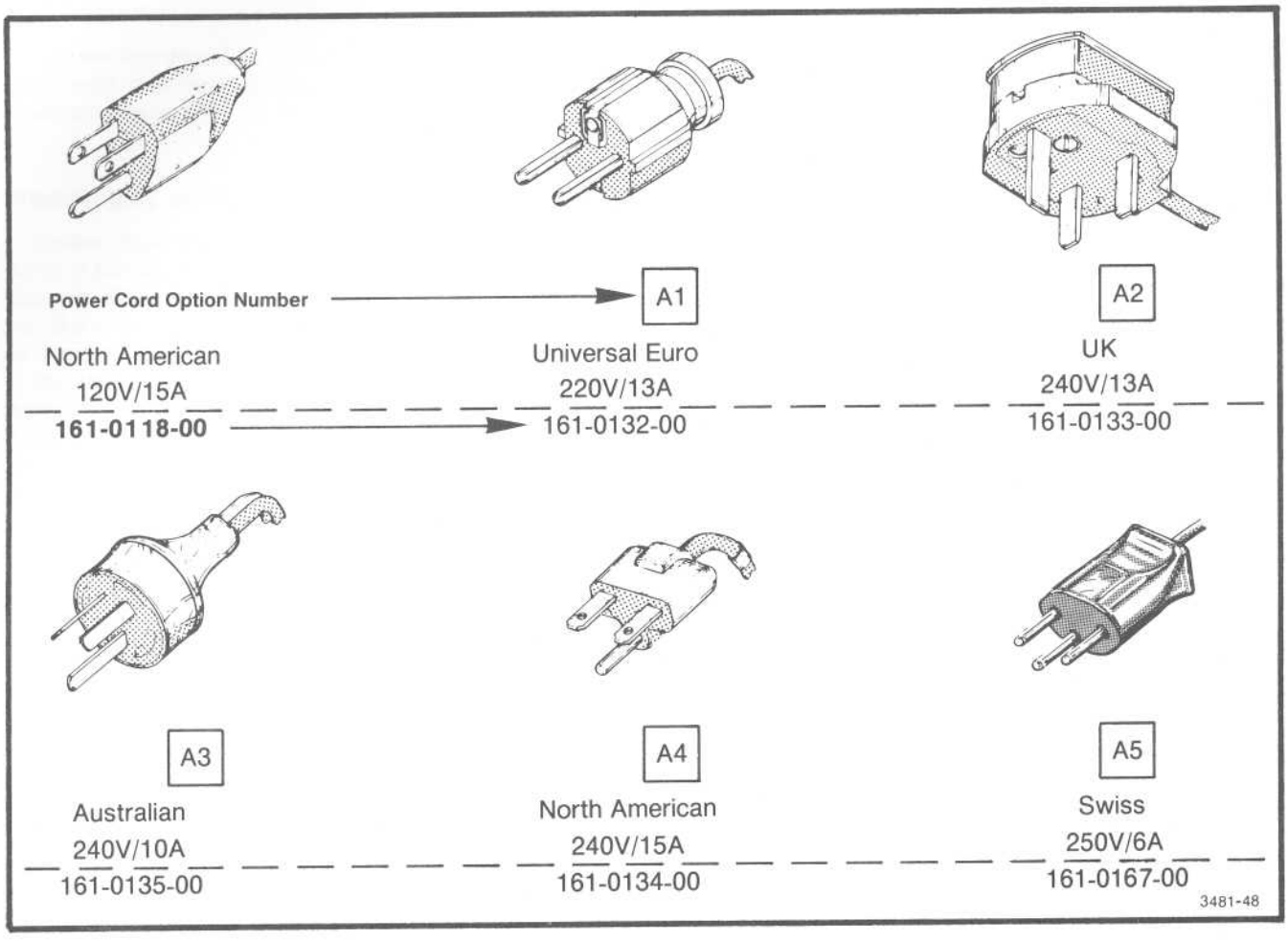


Fig. 1-3. International power cord and plug configuration for the 496/496P.

INSTALLATION AND REPACKAGING

Introduction

This section describes unpacking, installation, power requirements, and repackaging information for the 496/496P Spectrum Analyzer.

Unpackaging and Initial Inspection

Before unpacking the 496/496P from its shipping container or carton, inspect for signs of external damage. If the carton is damaged, notify the carrier as well as Tektronix, Inc. The shipping carton contains the basic instrument and its standard accessories. Optional accessories are shipped in separate containers. Refer to the Accessories page following the Replacable Mechanical Parts list in the 496/496P Service Volume 2 manual for a complete listing.

If the contents of the shipping container are incomplete, if there is mechanical damage or defect, or if the instrument does not meet operational check requirements, contact your local Tektronix Field Office or representative.

The instrument was inspected both mechanically and electrically before shipment. If should be free of mechanical damage and meet or exceed all electrical specifications. Procedures to check functional or operational performance are in the Calibration section. The functional check procedure verifies proper instrument operation and should satisfy the requirements for most receiving or incoming inspections. The electrical performance check follows the functional check.

Preparation for Use

The 496/496P can be installed in any position that allows air flow in the bottom and out the rear of the instrument. Feet on the four corners allow ample clearance even if the instrument is stacked with other instruments. A fan draws air in through the bottom and expels air out the back. Avoid locating the 496/496P where paper, plastic, or like material might block the air intake.

The front panel cover for the 496/496P provides a dust-tight seal. Use the cover to protect the front panel when storing or transporting the instrument. The cover is also used to store accessories and external waveguide mixers. The cover is removed by first pulling up and in on the two release latches then pulling up on the cover. The accessories door is unlatched by pressing the latch to the side and lifting the cover.

The handle of the 496/496P can be positioned at several angles to serve as a tilt stand, or it can be positioned at the top rear of the instrument between the feet and the rear panel so that 496/496P instruments can be stacked. To position the handle, press in at both pivot points and rotate the handle to the desired position.

CAUTION

Removing or replacing the cabinet on the instrument can be hazardous. The cabinet should only be removed by qualified service personnel. See Removing the Cabinet at the beginning of the Calibration Procedure section.

Power Source and Power Requirements

The 496/496P is designed to operate from a single-phase power source that has one of its current-carrying conductors (neutral) at ground (earth) potential. Operating from power sources where both current-carrying conductors are isolated or above ground potential (such as phase-to-phase on a multi-phase system or across the legs of a 110-220 V single-phase, three-wire system) is not recommended, since only the line conductor has over-current (fuse) protection within the unit. Refer to the Safety Summary at the front of this manual.

The ac power connector is a three-wire polarized plug with the ground (earth) lead connected directly to the instrument frame to provide electrical shock protection. If the unit is connectd to any other power source, the unit frame must be connected to an earth ground.

Power and voltage requirements are printed on a back panel plate mounted below the power input jack. The 496/496P can be operated from either 115 Vac or 230 Vac nominal line voltage with a range of 90 to 132 on 180 to 250 Vac, at 48 to 440 Hz. A multipin (harmonica) type connector on the power supply etched circuit board can be positioned to accommodate either voltage range. When the power supply circuitry is changed to accommodate a different power source, the information plate on the back panel must also be changed to reflect the new power requirements. Refer to Changing Power Input Range in Section 1.

Repackaging for Shipment

When the 496/496P is to be shipped to a Tektronix Service Center for service or repair, attach a tag showing: owner and address, name of individual at your firm that can be contacted, complete serial number, and a description of the service required. If the original packaging is unfit for use of not available, repackage the equipment as follows:

1. Obtain a carton of corrugated cardboard having inside dimensions that are at least six inches more than the equipment dimensions, to allow for cushioning. Table 2-1 lists instrument weights and carton strength requirements.

2. Install the front cover on the 496/496P and surround the equipment with polyethylene sheeting to protect the finish.

3. Cushion the equipment on all sides with packing material or urethane foam between the carton and the sides of the equipment.

4. Seal with shipping tape or industrial stapler.

Table 2-1
SHIPPING CARTON TEST STRENGTH

Gross Weight		Carton Test Strength	
Pounds	Kilograms	Pounds	Kilograms
0—10	0—3.73	200	74.6
10—30	3.73—11.19	275	102.5
30—120[a]	11.19—44.76	375	140.0
120—140	44.76—52.22	500	186.5
140—160	52.22—59.68	600	223.8

[a]Applicable to the 496/496P.

If you have any questions, contact your local Tektronix Field Office or representative.

CALIBRATION

INTRODUCTION

Calibration consists of a Performance Check and an Adjustment Procedure. The descriptive detail for these procedures assume the user is knowledgeable in the use of sophisticated test equipment and test procedures. The Performance Check describes procedures to verify that the instrument is performing properly and meets specifications listed in Section 1. All tests can be performed without access to the interior of the instrument. The Adjustment Procedure provides instructional steps required to recalibrate the instrument circuits. After adjustment, the performance should be checked by the procedure described under the Performance Check part. We recommend adjusting only those circuits that do not meet performance criteria.

Since most instruments will have one or more options, procedures for these options are a sub-part of the step and integrated into this section.

The limits, tolerances, and waveform illustrations are aids to calibrate the instrument and are not intended as performance specifications.

HISTORY INFORMATION

The instrument and manual are periodically evaluated and updated. If modifications require changes in the calibration procedure, history information applicable to earlier instruments is included as a deviation within a step or as a sub-part to a step.

EQUIPMENT REQUIRED

Table 3-1 lists the test equipment and calibration fixtures recommended for the Performance Check and Adjustment Procedure. The characteristics specified are the minimum required for the checks. Substitute equipment must meet or exceed these characteristics. Special calibration fixtures that are listed facilitate the procedure. These are available from Tektronix, Inc., and may be ordered through your local Tektronix Field Office or representative.

Sophisticated test equipment and/or procedures are required to accurately measure some high tolerance characteristics. In these cases, a compromise may be made in the procedure. Any compromise is indicated by a footnote. Procedures to check these high tolerance specifications, when a compromise has been made, can be supplied by Tektronix Service Centers.

Table 3-1
EQUIPMENT REQUIRED

Equipment or Test Fixture	Characteristics	Recommendation and Use
	PERFORMANCE CHECK	
Test Oscilloscope	Vertical sensitivity, 50 mV/Div to 5 V/Div	Any TEKTRONIX 7000-Series oscilloscope with plug-in units for real-time display such as: 7A11/7B50A, and P6108 1X Probe (used to monitor signal and voltage levels)
Two Time Mark Generators	Marker output, 1 s to 1 μs; accuracy, 0.001%	TEKTRONIX TG 501 and TM 500-Series Power Module (used to check time/div and span accuracy)
Digital Frequency Counter	10 Hz to 1 GHz, 20 mV rms sensitivity	TEKTRONIX DC 508A Digital Counter (used to measure calibrator frequency)

Table 3-1 (cont)

Equipment or Test Fixture	Characteristics	Recommendation and Use
Function or Sine-Wave Generator	1 Hz to 1 MHz; 0 to 20 V p-p	TEKTRONIX FG 503 Function Generator (used to check external trigger and horizontal input requirements)
Signal Generator(s)	10 Hz to 10 MHz constant output; 250 kHz—110 MHz, leveled output	Hewlett-Packard Model 654 (used to check frequency response)
	Two 500 kHz to 2.0 GHz generators calibrated and leveled. Output, +10 dBm to −100 dBm; spectral purity, >60 dB below fundamental	TEKTRONIX SG 503 Signal Generator Hewlett-Packard Model 8640A/B Option 02 and two 8614A (used to check frequency response; also used as a signal source for IM and display accuracy checks)
Sweep Oscillator	100 kHz to 18 GHz; frequency response, ±1.0 dB	Hewlett-Packard Model 8620C with 86222B Sweep Oscillator (used to check frequency response and flatness)
Power Divider		Hewlett-Packard Model 11667A
Power Meter with Power Sensors	−60 dBm to −20 dBm full scale; 100 kHz to 18 GHz	Hewlett-Packard Model 435B with 8482A and Power Sensors
Vector Voltmeter	Frequency to 100 MHz	Hewlett-Packard Model 8405A (used to check CALibrator OUTput)
or		
Power Meter with Lowpass Filter	Measure −20 dBm within ±0.1 dB (the filter must have rolloff of 40 dB or more at 200 MHz)	Hewlett-Packard Model 435B with 8481A Sensor (used to check CALibrator OUTput). Filter: Texscan or Lark
Comb Generator UHF	Provide comb line to 18 GHz; accuracy, 0.01%	TEKTRONIX Calibration Fixture 067-0885-00 with TM 500 Power Module (used to check frequency readout accuracy)
Spectrum Analyzer	Frequency range, 2.0—3.0 GHz	TEKTRONIX 7L18, 7L13 MOD 139U, or 492/492P (used to adjust 1st and 2nd LO frequency offset)
Attenuator (SMA connectors)	3 dB, 50 Ω; dc to 20 GHz	Weinchel Model 4M. Tektronix Part No. 015-1053-00
Attenuators (bnc connectors; two required)	20 dB, 50 Ω; dc to 2.0 GHz	Tektronix Part No. 011-0059-02
Coaxial Cable (50 Ω, 5 ns SMA connectors)		Tektronix Part No. 015-1006-00
Adapter (N male-to-SMA male)		Tektronix Part No. 015-0369-00
Adapter (N male-to-bnc female)		Tektronix Part No. 103-0045-00
T Connector (bnc)		Tektronix Part No. 103-0030-00

Table 3-1 (cont)

Equipment or Test Fixture	Characteristics	Recommendation and Use
Step Attenuators	Range: 0 – 110 dB in 10 dB and 1 dB steps; accuracy: 0.1 dB; frequency range: dc to 18 GHz	Step attenuator such as Hewlett Packard 8493 and 8496B calibrated by precision standard attenuators; such as Weinchel Model AS-5 attenuator
Coaxial Cables (50 Ω, 2 required)		Tektronix Part No. 012-0482-00

ADJUSTMENTS

All the items listed above plus the following are required for the Adjustment Procedure.

Return Loss Bridge	10 MHz to 1 GHz, 50 Ω	Wiltron VSWR Bridge Model 62BF50
Attenuator (3 dB miniature)	Frequency: to 1.8 GHz; connectors: 5 mm	Weinchel Model 4M Tektronix Part No. 015-1053-00
Autotransformer	Capable of varying line voltage from 90 to 130 Vac	General Radio Variac Type W10MT3
Digital Multimeter	10 μV to 1350 Vdc	TEKTRONIX DM 501A or DM 502A
Dc Block		Tektronix Part No. 015-0221-00
Adapter (Sealectro male-to-male)		Tektronix Part No. 103-0098-00; Sealectro Part No. 51-072-0000
Adapter (bnc female-to-Sealectro male)		Tektronix Part No. 103-0180-00
Three Extension Cables (Sealectro female-to-Sealectro male)*		Tektronix Part No. 175-2902-00
Adapter (bnc-to-Sealectro)		Tektronix Part No. 175-2412-00
Adapter (bnc female to SMA male)		Tektronix Part No. 015-1018-00
Cable (20") Tip plugs to bnc		Tektronix Part No. 175-1178-00
Coaxial cable (8")		Tektronix Part No. 012-0208-00
Screwdriver, tuning		Tektronix Part No. 003-0675-00
Alignment Tool	Square pin adjusting tool for VR calibration	Tektronix Part No. 003-0965-00
Screwdriver, flat 6" with 1/8" tip.		
Screwdriver, Phillips type		No. 1
Allen wrenches (3) 3.32", 5.64", 7.64"		
Service Kit (Extender boards)*		Tektronix Part No. 672-0865-00

*These fixtures are part of the Service Kit 006-3286-00, listed in the Maintenance Section.

PERFORMANCE CHECK PROCEDURE

INTRODUCTION

As stated in the section introduction, the following procedures check is a functional as well as performance check. All performance requirements listed under electrical characteristics in the Specification section are verified. The tests do not include any internal adjustments or checks. The checks should be performed in the sequence given because some tests rely on the satisfactory performance of related circuits. They are also arranged to minimize test equipment setup. If a performance measurement is marginal or below specification, an adjustment procedure to optimize the circuit performance will be found under a similar heading in the Adjustment Procedure of this section. If adjustment fails to return the circuit to specified performance, refer to the Maintenance section for troubleshooting and repair procedures. After adjustment, return to the Performance Check to continue with the calibration process.

INCOMING INSPECTION TEST

The Operators manual contains a functional check that checks all functions of the 496/496P. This check is recommended for incoming inspections because it provides a reliable indication that the instrument is performing properly. This Performance Check procedure checks all instrument specifications and requires sophisticated equipment as well as technical expertise to perform.

PRELIMINARY PREPARATION

a. Perform the initial calibration described under Turn On Procedure in the Operator's manual. For rackmount/benchtop versions, refer to Rackmount/Benchtop section of this manual.

b. Set the front panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN DIV	100 kHz
REF LEVEL	20 dBm
MIN RF ATTEN	0 dB
AUTO RESOLUTION	On
TIME/DIV	AUTO
Vertical Display	10 dB DIV
Video Filter	Off
Digital Storage	VIEW A/VIEW B
BASELINE CLIP	OFF
TRIGGERING	FREE RUN
FINE (push button)	Coarse (not illuminated)
PEAK/AVERAGE	Fully cw

c. Allow the instrument to warm up for at least 30 minutes before proceeding with this check.

1. Check Operation of Front Panel Push Buttons and Controls

The following procedure checks functions activated by front-panel push buttons and that the buttons illuminate when the function is active. Operation of the front-panel controls is also checked.

With the CAL OUT signal applied to the RF INPUT, tune the 100 MHz, 20 dBm signal to center screen. Reduce the FREQ SPAN DIV to 100 kHz keeping the signal centered on screen with the FREQUENCY control. Press or change the following push buttons and controls and note their effect.

INTENSITY. Rotate the control through its range and note crt beam brightness change

READOUT. Inactive state, no crt readout. Active state, crt readout of REF LEVEL, FREQUENCY, FREQ SPAN/DIV, VERT DISPLAY, RF ATTEN, FREQ RANGE, and RESOLUTION BANDWIDTH. The INTENSITY control changes brightness.

GRAT ILLUM. Inactive state, no graticule lights. Active state, graticule lights.

BASELINE CLIP. Inactive, no clipping of the display baseline. Active, display intensity at the baseline is clipped (subdued).

TRIGGERING. Triggering mode is activated by pressing one of four push buttons. Pressing any one of the buttons cancels or deactivates the other mode.

FREE RUN. Active, trace free runs.

INT. Active, trace displayed when signal or noise level at left edge is ≥1.0 division.

LINE. Active, trace triggered at power line frequency.

EXT. Active, trace runs when an external signal ≤1.0 V peak or less is applied to the back panel EXT IN connector.

SINGLE SWEEP. Pressing this button to activate single sweep aborts the recurrent sweep: pressing the button again arms the sweep generator and lights READY, which remains lighted until the sweep completes. The analyzer makes a single sweep of the selected spectrum when the conditions determined by TRIGGERING are met. Single sweep mode is cancelled when any TRIGGERING button is pressed. The effect of SINGLE SWEEP may be more apparent if VIEW A, VIEW B, and B – SAVE A are off.

TIME/DIV. Selects sweep rate and manual scan operation. In MNL position, MANUAL SCAN control should vary the crt beam across the full horizontal axis of the crt graticule.

VERTICAL DISPLAY. Display modes are activated by three push buttons. Pressing any of these buttons cancels the other mode.

10 dB/DIV. Active, display is a calibrated 10 dB/division, 80 dB dynamic range. Calibration is checked later in this procedure.

2 dB/DIV. Active, display is calibrated 2 dB/division, 16 dB dynamic range. Calibration is checked later in this procedure.

LIN. Active, display is linear between the reference level (top of graticule) and zero volts (bottom of graticule). The crt VERT DISPLAY reads out in volts/division.

PULSE STRETCHER. Active, increases the fall time of video signals to make narrow pulses on the display easier to see. With FREQ SPAN/DIV at MAX, TIME/DIV at 5 ms and Digital Storage off, the markers should increase in brightness when PULSE STRETCHER is active.

VIDEO FILTER. Two filters, independently selected to provide WIDE (1/30th) or NARROW (1/300th) of the resolution bandwidth for noise reduction.

DIGITAL STORAGE. Either or both sections of memory can be selected to provide digital storage. When either or both are activated, signal amplitude should remain constant. Vary the PEAK AVERAGE control and note that noise level below the PEAK AVERAGE cursor is averaged.

VIEW A/VIEW B. When SAVE A is off, either VIEW A or VIEW B will display all data (1024 bits) in memory. Both sections of memory are updated each sweep. When SAVE A is activated, VIEW A displays data saved in the A section of memory (512 bits) and VIEW B displays data (512 bits) in the B section of memory. B section is updated each sweep.

SAVE A. Active, contents in A memory are saved and not updated. Verify operation by changing REF LEVEL, and observe that the VIEW A display does not change when VIEW B is inactive.

MAX HOLD. Active, stores maximum signal amplitude at each memory location. Verify operation by changing FREQUENCY or REF LEVEL and note that the maximum level at each location is retained.

B – SAVE A. Active, the difference between updated data in B section of memory and that saved in A is displayed. Verify by saving data in A, then changing the refrence level and pressing B – SAVE A; only the difference can be observed by cancelling VIEW A and VIEW B. The reference (zero difference) level is normally set at graticule center, but can be internally adjusted. See Adjustment Procedure.

PEAK/AVERAGE. When digital storage is activated with VIEW A or VIEW B, this control positions a horizontal line or cursor on the display. Signals above the cursor are peak detected, signals below the cursor are averaged. The cursor should position anywhere within the graticule window.

PHASELOCK. Activated to reduce residual FM when narrow spans are selected. The button lights when active, pressing the button turns phaselock off. When active, the microcomputer automatically selects phaselock for a span division of 50 kHz or below.

AUTO RESOLUTION. When activated, RESOLUTION BANDWIDTH changes so bandwidth is compatible with FREQ SPAN/DIV selection. Check by changing FREQ SPAN/DIV and noting that RESOLUTION BANDWIDTH changes. UNCAL indicator should not light over the FREQ SPAN/DIV range if TIME/DIV selector is in AUTO position.

ZERO SPAN. When activated, converts the 496/496P to time domain operation, with the display calibrated in TIME/DIV instead of FREQ SPAN/DIV. The RESOLUTION BANDWIDTH and FREQUENCY are not altered.

FREQUENCY SPAN/DIV. As this control is rotated clockwise, FREQ SPAN/DIV should change from 0 to MAX in 1-2-5 sequence. Display should indicate this change. The 496/496P has a range from 200 MHz/div to 50 Hz/div.

RESOLUTION BANDWIDTH. As this control is rotated, resolution bandwidth should change in decade steps from 1 MHz to 1 kHz, with a final step at 30 Hz.

ΔF. When activated, center frequency readout initializes to 0 MHz. The frequency difference, to a desired signal or point on the display, can now be determined by tuning that point to center screen and noting the readout. Check by measuring the difference between calibrator markers. If the frequency is tuned below "0", the readout will indicate minus (−). When the FREQ SPAN/DIV is ≤50 kHz, the readout is calibrated in kHz.

DEGAUSS. When pressed, residual magnetism build-up in the local oscillator system is reduced. Switch FREQ SPAN/DIV to 1 MHz and tune the calibrator marker to center screen. Note the signal position, then press the DEGAUSS button. The signal should shift horizontally and then return to a new location. Press again and the signal should return to the same new location. Return FREQ SPAN/DIV to 100 MHz.

CAL. Checked when performing Turn On Procedure.

REFERENCE LEVEL. Continuous control that requests the microcomputer to change the reference level one step for each detent. In the 10 dB/DIV Vertical Display mode, the steps are 10 dB. When FINE is activated, the steps are 1 dB. In the 2 dB/DIV mode, the steps are 1 dB or 0.25 dB for the FINE mode. When FINE is activated in the 2 dB/DIV mode, the ΔA mode is operational. The REF LEVEL goes to 0.00 dB then steps in 0.25 dB increments from an initial 0.00 dB reference level.

Set the MIN RF ATTEN to 0 dB. Set the vertical display to 10 dB/DIV, and rotate the REF LEVEL control counterclockwise to +30 dBm then clockwise to −120 dBm. Note the change in the display. Return the REF LEVEL to −20 dBm and note that 10 dB of RF ATTEN is switched in at −20 dBm.

MIN RF ATTEN. Sets the minimum amount of RF attenuation. Changing RF LEVEL will not decrease RF attenuation below that set by the MIN RF ATTEN selector.

FINE. When activated, REF LEVEL switches in 1 dB increments for 10 dB/DIV display mode, and 0.25 dB for 2 dB/DIV display mode. In the 2 dB/DIV display mode, FINE actuates ΔA mode.

MIN NOISE/MIN DISTORTION. One of two algorithms is selected to control attenuator and IF gain. MIN NOISE (button illuminated) reduces the noise level by reducing attenuation 10 dB and decreasing IF gain 10 dB. MIN DISTORTION reduces IM distortion due to input mixer overload. To observe any change, the RF ATTEN, displayed by the crt readout, must be 10 dB higher than that set by the MIN RF ATTEN selector.

UNCAL. This light comes on when the display is uncalibrated. Set the TIME/DIV to 50 ms, deactive the AUTO RESOLUTION, and set the RESOLUTION BANDWIDTH to 10 kHz. UNCAL should light and remain lit until the FREQ SPAN/DIV is reduced to 200 kHz or the RESOLUTION BANDWIDTH is increased to 1 MHz. Return the TIME/DIV to AUTO and activate the AUTO RESOLUTION. Set the FREQ SPAN/DIV to 100 MHz.

This completes the functional check of the front-panel controls and push buttons.

2. Check Frequency Readout Accuracy Readout accuracy is ±(5 MHz + 20% Span/Div).

NOTE

Due to residual magnetism buildup in the 1st (YIG) oscillator tuning coils, accuracy of the frequency readout should be checked after the tuning coil has been degaussed by pressing the DEGAUSS button. Degauss when the FREQ SPAN/DIV is either 2 MHz or 1 MHz before reducing the FREQ SPAN/DIV to 500 kHz.

a. Test equipment setup is shown in Fig. 3-1. Set the front-panel controls as follows, then apply the CAL OUT to the RF INPUT.

FREQENCY	100 MHz
FREQ SPAN/DIV	20 MHz
REF LEVEL	−20 dBm
MIN RF ATTEN	0 dB
AUTO RESOLUTION	On
TIME/DIV	AUTO
Vertical Display	10 dB/DIV
Video Filter	WIDE
Digital Storage	VIEW A/VIEW B

b. Tune the 100 MHz calibrator line to center screen. Decrease the FREQ SPAN/DIV to 2 MHz or 1 MHz, keeping the 100 MHz signal centered. Press the DEGAUSS button, decrease the FREQ SPAN/DIV to 500 kHz, and center the signal under the frequency dot. Press CAL.

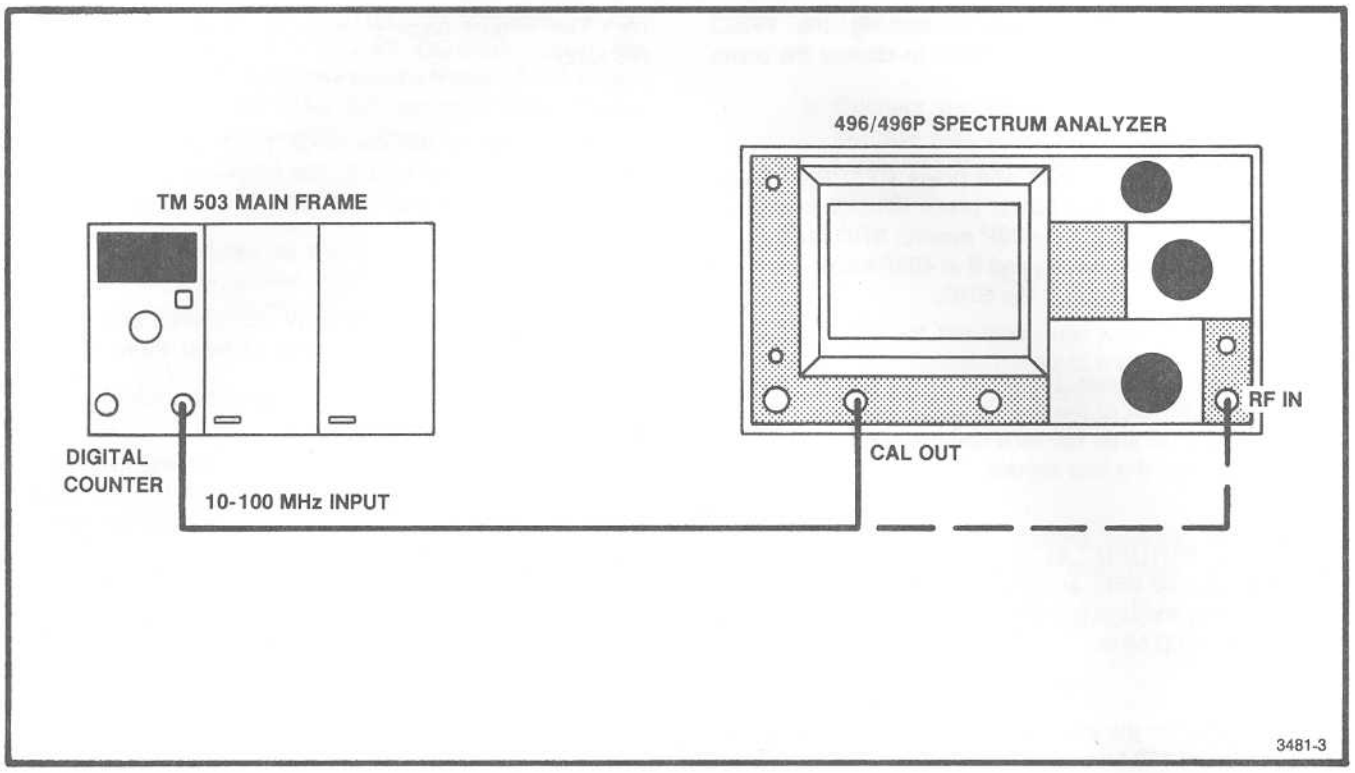


Fig. 3-1. Test equipment setup for checking frequency of the calibrator and the accuracy of the frequency readout.

c. Calibrate the frequency readout by adjusting the frequency control for a readout of 100 MHz. Deactivate the CAL push button.

d. Return the FREQ SPAN/DIV control to 20 MHz and tune the FREQUENCY to the next comb line (200 MHz). Decrease the FREQ SPAN/DIV to 2 MHz, degauss the tuning coils, then decrease the span to 500 kHz/div and center the comb line under the frequency dot. Check the frequency readout accuracy. If a spurious response, tune to the next marker and check. Readout must equal 200 MHz ±(5 MHz +20% Span/Div).

e. Repeat this process checking frequency readout accuracy throughout the band.

f. Leave the comb generator connected for 496P; disconnect the comb generator for the 496.

3. 496P only—TUNE Accuracy Check ±(7% of frequency or 150 kHz), whichever is greater, after a 2-hour warm-up

a. Enter the following program on a 4050-Series controller:

```
100 REMARK TUNE CHECK
110 PRINT @1:"SAVEA OFF;TRIG FRERUN"
120 WBYTE @33,1:
130 INPUT T$
140 PRINT @1:"SIGSWP;SAVEA ON;TUNE";T$;";SIGSWP"
150 INPUT W$
160 GO TO 110
```

b. Connect the 4050-Series controller to the 496P with a GPIB cable (both should already be turned on). Set the 496P GPIB ADDRESS switches for address 1 (switch 1 up, all others in the switch bank down).

c. Change the front-panel controls for:

FREQUENCY	100 MHz
FREQ SPAN/DIV	100 MHz
Video Vilter	Off
PEAK/AVERAGE	Fully ccw

d. Type RUN and press RETURN on the controller. Line 110 of the program immediately sets the sweep and the digital storage so you can change FREQUENCY and other local controls as required for the TUNE check. Line 120 restores local control with the GTL message.

e. Center the marker while decreasing the FREQ SPAN/DIV to 2 MHz. Set REF LEVEL to display the comb marker.

f. Enter 100M (type 100M and press RETURN). If you make an error in this procedure, press BREAK twice and run the program again. If the 496P asserts SRQ (evident by message on controller screen and S in 496P lower readout), enter WBYTE @20: to clear the SRQ.

g. The analyzer tunes 100 MHz, takes a single sweep, and sets up a display of the marker signal you centered and the signal acquired after the tune command executed. Note the error between the two signals.

h. Press RETURN to continue. Change FREQ SPAN/DIV to 100 MHz and FREQUENCY to 1000 MHz. Repeat parts e through g, then repeat the procedure for a frequency of 1700 MHz.

i. Tune error for the above checks should not exceed 3.5 divisions (7% of 100 MHz tune step is 7 MHz).

The foregoing procedure checks performance related to the upper DAC of the 1st LO center frequency control. The remaining procedure checks the lower DAC for the 1st LO.

j. Press RETURN and change the controls as follows:

FREQ SPAN/DIV	200 MHz
FREQUENCY	1 MHz
REF LEVEL	+30 dBm

k. Disconnect the calibrator and connect the output of the time mark generator to the RF INPUT. Set the time mark generator for 2 μs output.

l. Change the FREQUENCY (and REF LEVEL if necessary) while decreasing the FREQ SPAN/DIV to 100 kHz to maintain a centered marker above the 0 Hz spurious response.

m. Type 500K and press RETURN on the controller. Note the difference in the displayed signals, then press RETURN again.

n. Repeat part m seven times. Reset FREQUENCY after noting the error if the accumulated TUNE error is great enough to move the signal off screen. (The FREQUENCY control is active at the point where you note the TUNE error.) The largest error should not exceed 0.75 divisions (75 kHz).

This completes the check of TUNE command performance related to the 1st LO. The following steps check the upper DAC of the pair that control the 2nd LO center frequency.

o. Increase FREQ SPAN/DIV to 1 MHz and change FREQUENCY to center a marker at least three divisions away from the 0 Hz marker.

p. Decrease the span to 2 kHz/div keeping the marker centered and change the time marker output to 10 μs. Change the REF LEVEL as necessary to keep the marker above the noise.

q. Type 100K and press RETURN on the controller. Note the difference in the displayed signals, then press RETURN again.

r. Increase span to 50 kHz/div, change the time marker output to 1 μs, and tune FREQUENCY one marker to the left (−1 MHz). Repeat parts p and q.

s. Increase the span to 50 kHz/div, change the time marker output to 1 μs, and tune FREQUENCY two markers to the right (+2 MHz). Repeat parts p and q.

t. The largest error noted should not exceed 3.5 divisions (7% of 100 kHz tune or 7 kHz).

This completes a check of the 2nd LO upper DAC. A check of the 2nd LO lower DAC follows.

u. Apply 1.0 ms markers, then center one of the markers with the FREQUENCY while reducing FREQ SPAN/DIV to 1 kHz (change REF LEVEL as necessary).

v. Enter 1K at the controller and note the difference in the displayed signals. Press RETURN again. Repeat this step seven times. Reset FREQUENCY after noting the error if it appears the signal will be forced off-screen by the accumulated TUNE error. (The FREQUENCY control is active when the error is noted).The largest error should not exceed 1.0 division.

4. Check Calibrator (frequency 100 MHz ±1.7 kHz, output level −20 dBm ±0.3 dB)

@

a. Check the calibrator frequency by connecting a frequency counter (e.g., TEKTRONIX DC 508A (using the 10–100 MHz input) or Hewlett-Packard Model 5342A Digital Counter) to the 496/496P CAL OUT connector and measure the frequency. Fundamental frequency is 100 MHz ±1.7 kHz.

b. Three procedures for measuring output level are given; vector voltmeter, power meter, and comparison method using an accurate −20 dBm source.

1. Vector Voltmeter Method

a. Terminate the voltmeter probe with a 50 Ω feedthrough termination and then connect the terminated probe to the 496/496P CAL OUT connector (Fig. 3-2).

b. Set the vector voltmeter frequency to 100 MHz.

c. Check—for an rms reading between 21.11 mV and 22.69 mV (−20 dBm is 22.36 mV rms across 50 Ω).

2. Power Meter Measurement

a. Test equipment setup is shown in Fig. 3-2.

b. Connect the power meter sensor through a lowpass filter (≥40 dB at 200 MHz to remove harmonics of the fundamental) to the CAL OUT connector.

NOTE

Insertion loss of the filter with pads, measured at 100 MHz, must be determined to within ±0.05 dB. To ensure a 50 Ω match, use approximately 3 dB minimum-loss matching pads (attenuator) on both sides of the filter.

c. Note the power reading. Reading, plus the loss through the filter and pads, must equal −20 dBm, ±0.3 dB.

3. Signal Substitution Method

NOTE

A power meter is used to verify the output level of the reference signal. Harmonics of the signal source must be greater than 40 dB down.

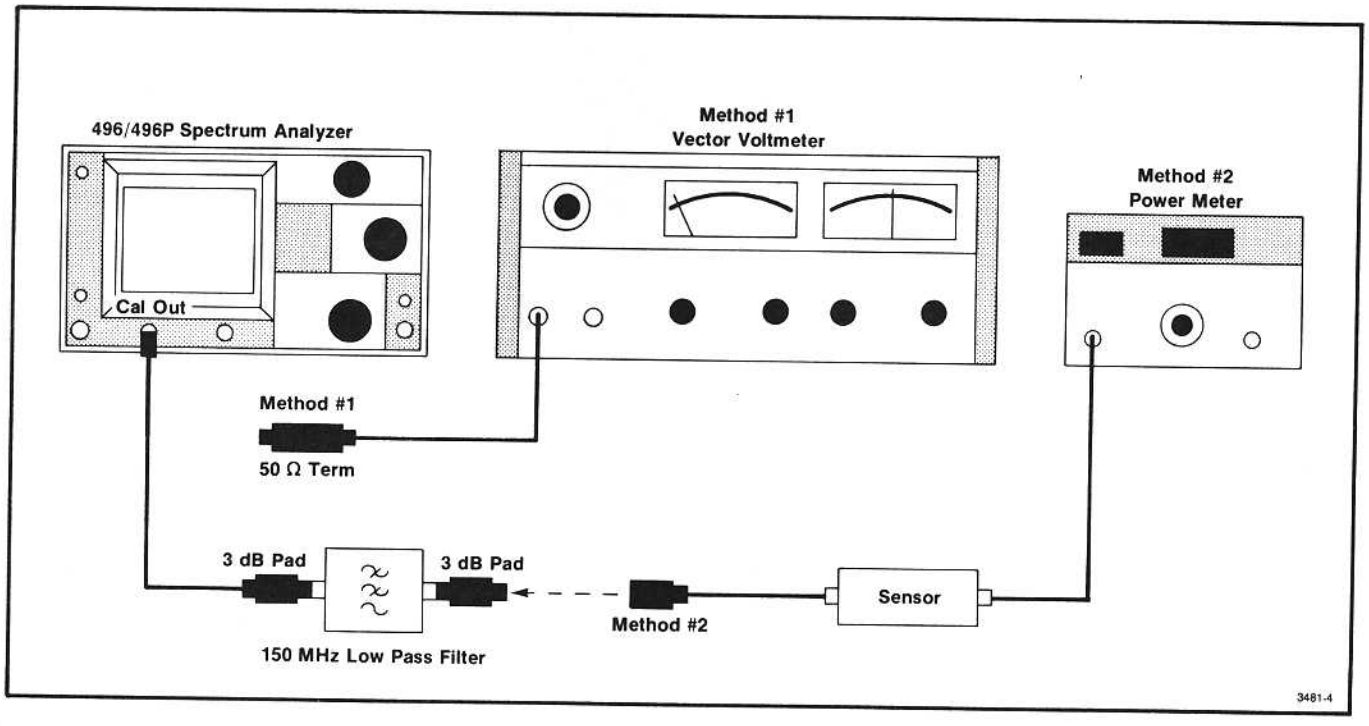


Fig. 3-2. Test equipment setup showing two methods that check calibrator output level.

a. Apply a 100 MHz signal from a signal source (signal generator) through a 3 dB attenuator to the power meter. Adjust the output level for −20.0 dBm reading on the power meter.

b. Set the front-panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	500 kHz
REF LEVEL	−10 dBm
MIN RF ATTEN	0 dB
RESOLUTION BANDWIDTH	1 MHz
TIME/DIV	AUTO
Vertical Display	10 dB/DIV
Video Filter	Off
Digital Storage	VIEW A/VIEW B

c. Disconnect the meter and (using the same instrument cable and attenuator) apply the calibrated reference signal to the 496/496P RF INPUT.

d. Switch to the 2 dB/DIV display mode and tune the reference signal to center screen. Select a REF LEVEL that positions the top of the signal to a graticule line (2nd or 3rd from the top of the screen). Select a SPAN/DIV and RESOLUTION BANDWIDTH to obtain a broad display for more accurate measurement. Store the reference display by activating SAVE A.

e. Remove the reference signal and apply the CAL OUT signal to the RF INPUT.

f. Note the displacement of the CAL signal from the reference. Activate B−SAVE A and note the displacement between the CAL signal and the reference. Displacement must not exceed 0.3 dB (0.75 minor division with a 2 dB/DIV display mode).

NOTE

If greater accuracy is desired, the vertical signal can be amplified through an external amplifier, such as the TEKTRONIX 7A15, to increase the vertical sensitivity. This is done by applying the veritical signal at the rear panel VERT connector of the 496/496P to the external amplifier input and selecting the vertical amplification and Time/Div values that provide the degree of accuracy desired.

5. Check RF Attenuator (within 0.3 dB/10 dB to a maximum of 0.7 dB over the 60 dB range)

NOTE

The attenuator is factory checked to ensure accuracy. Any change in characteristics should be large enough to be readily noticed in operation. The Functional Check in the Operators manual provides a good indication of attenuator performance and would detect component failure. External 10 dB, 20 dB, or a 30 dB step attenuator (calibrated by the user or manufacturer to within 0.05 dB) must be used as a standard to check the RF attenuator in this procedure.

a. Test equipment is shown in Fig. 3-3. Apply a 0 dBm, 1 GHz signal, from a signal generator through 30 dB of calibrated attenuation to the RF INPUT of the 496/496P. Set the front panel controls as follows:

FREQUENCY	1.0 GHz
FREQ SPAN/DIV	200 MHz
REF LEVEL	−30 dBm
MIN RF ATTEN	0 dB
AUTO RESOLUTION	On
TIME/DIV	AUTO
Vertical Display	10 dB/DIV
Video Filter	Off
Digital Storage	VIEW A/VIEW B

b. Tune the signal to center screen as the FREQ SPAN/DIV is reduced to 20 kHz and change the RESOLUTION BANDWIDTH to 100 kHz. Activate the 2 dB/DIV Vertical Display mode and the NARROW Video Filter. Adjust the 2 dB/DIV vertical Display mode and the NARROW Video Filter. Adjust the signal generator output so the signal peak is at some graticule reference level, such as seven divisions. Active SAVE A.

c. Change the REFERENCE LEVEL 10 dB by switching to −20 dBm (this will add 10 dB of RF ATTENuation).

d. Remove 10 dB of external attenuation and compare the difference between the reference level and the new level. Variation plus the calibrated 10 dB external attenuator correction factor must not exceed 0.3 dB. (Activate B−SAVE A to obtain the differential. Deactivate SAVE A and B−SAVE A.)

e. Readjust the signal generator output to establish a new reference level. Repeat the process to check the 20 dB

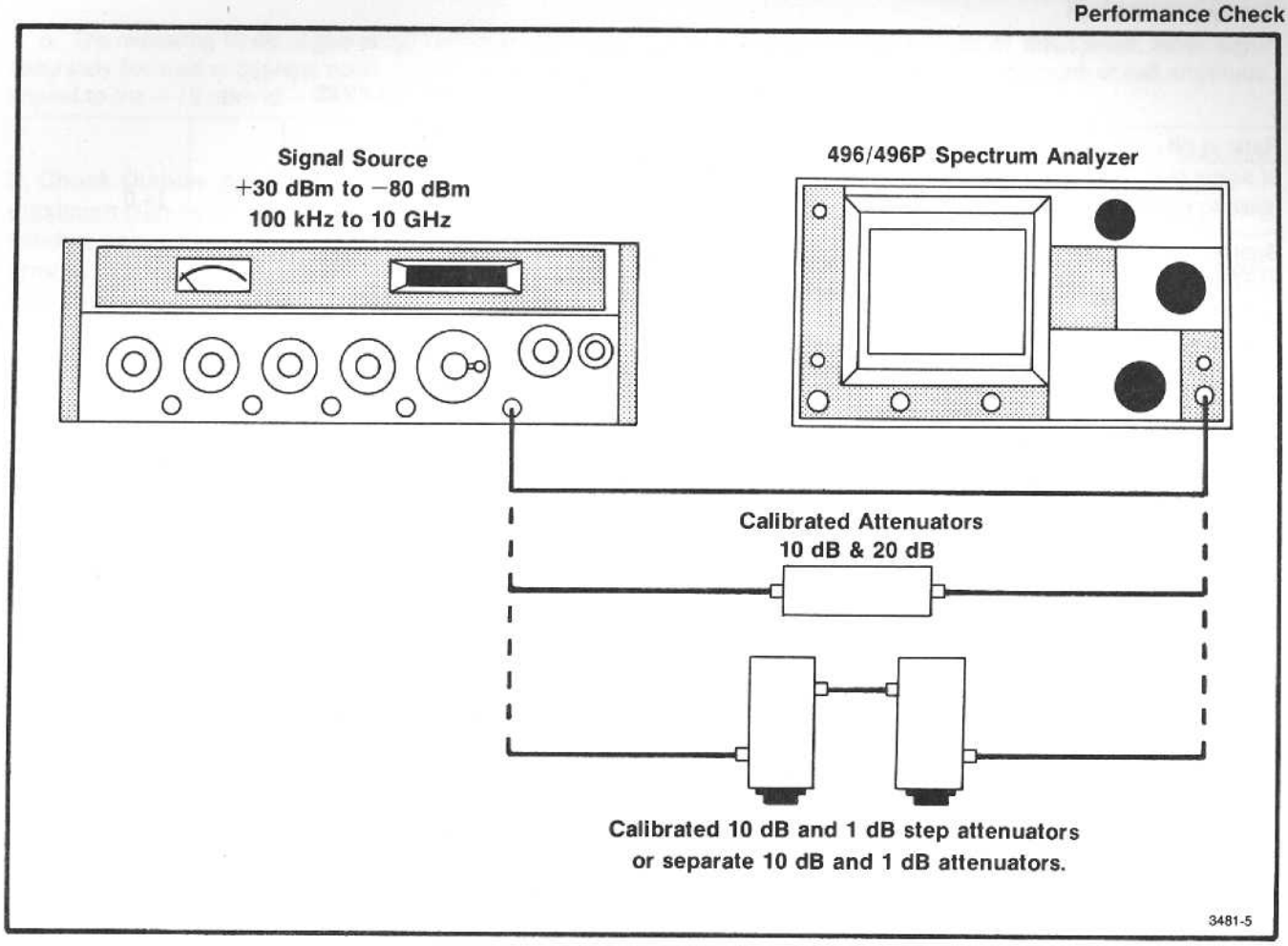


Fig. 3-3. Test equipment setup for verifying attenuator and gain accuracy.

attenuator by switching the REF LEVEL from −30 dBm to −10 dBm for 20 dB ATTEN, then remove 20 dB of external attenuation. Error must not exceed 0.6 dB.

f. Reinstall the 30 dB of external attenuation and set the REF LEVEL to −30 dBm. Re-establish a signal reference level as described above.

g. Check the 30 dB attenuator against the external standard, by switching the REF LEVEL to 0 dBm, for 30 dB RF ATTEN, then remove 30 dB of external attenuation. Error must not exceed 0.7 dB. (Include the calibrated attenuator correction factor.)

h. Since the remaining 60 dB range of the RF ATTENuator is obtained by the combination of these three attenuators, this completes the check of the RF attenuator. Error of any combination must not exceed 0.7 dB.

6. Check IF Gain Accuracy

Gain steps are monotonic (same direction) with the following limits:

Within 0.2 dB/dB to a maximum of 0.5 dB/9 dB, except at the decade transitions of −19 to −20 dBm, −29 to −30 dBm, 39 to −40 dBm, −49 to −50 dBm, −59 to −60 dBm, and −69 to −70 dBm, where an additional 0.5 dB can occur for a total of 1.0 dB per decade. Maximum deviation over the 90 dB range is within ±2 dB.

NOTE

This check requires calibrated attenuators as the standard to check the 1 dB and 10 dB steps. When making signal measurements within 10 dB of the noise floor, a correction factor should be used to correct for the logarithmic addition of noise in the system and analyzer, as shown in Table 3-2.

Table 3-2

CORRECTION FACTOR TO DETERMINE TRUE SIGNAL LEVEL

Ratio in dB of signal plus noise to noise	3.01	4.0	5.0	6.0	7.0	8.0	9.0	10.0	12.0	14.0
Subtract this correction factor for true signal level	3.01	2.20	1.65	1.26	0.97	0.75	0.58	0.46	0.28	0.18

a. Test equipment setup is shown in Fig. 3-3. Apply a −20 dBm, 100 MHz signal from the signal generator through 1 dB and 10 dB step attenuators (set at 0 dB) to the RF INPUT of the 496/496P. Apply the signal generator directly to the 496/496P if individual fixed attenuators are to be used as the standard. Set the front-panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	20 MHz
REF LEVEL	−10 dBm
MIN RF ATTEN	10 dB
AUTO RESOLUTION	On
TIME/DIV	Auto
Vertical Display	10 dB/DIV
Video Filter	WIDE
Digital Storage	VIEW A/VIEW B

b. Tune the signal to center screen, then decrease the FREQ SPAN/DIV to 10 kHz. Now change the RESOLUTION BANDWIDTH to 10 kHz and again center the signal on screen.

c. Change the Vertical Display to 2 dB/DIV. Adjust the signal generator output so the signal amplitude is six divisions with the top of the signal positioned on the 6th graticule line.

d. Activate MIN NOISE and note signal level shift. Shift must not exceed ±0.8 dB, or 2 minor divisions (attenuator plus gain accuracies).

e. Re-position the signal level to the graticule reference line by adjusting the output of the signal generator.

f. Switch the REF LEVEL from −10 dBm to −20 dBm in 1 dB steps, adding 1 dB of external attenuation at each step and note incremental accuracy and the 10 dB gain accuracy. Incremental accuracy must be within 0.2 dB/dB (0.5 minor division). Maximum cumulative error must not exceed 0.5 dB (1.5 minor divisions) except when stepping from the 9 dB to 10 dB increment, where the error could be an additional 0.5 dB for a total of 1.0 dB per decade.

g. Deactivate MIN NOISE. Return the 1 dB step attenuator to 0 dB, decrease the signal generator output to 10 dB or add 10 dB of external attenuation with the 10 dB step attenuator. Readjust the generator output so the signal level is again at the reference line (6 division amplitude).

h. Change the REF LEVEL in 1 dB increments from −20 dBm to −30 dBm adding 1 dB increments of external attenuation with the 1 dB step attenuator and note incremental and 10 dB step accuracies.

i. Return the 1 dB step attenuator to 0 dB, decrease signal level 10 dB by adding 10 dB more of external attenuation or decreasing the signal generator output level then re-establish the signal reference amplitude.

j. Check the −30 dBm to −40 dBm gain accuracies as previously described.

k. Repeat the procedure checking gain accuracies to −70 dBm.

l. Establish a signal reference at −70 dBm, activate NARROW VIDEO FILTER, then check gain accuracy to −80 dBm.

m. Select the 1 kHz resolution bandwidth and decrease the RESOLUTION BANDWIDTH and FREQ SPAN/DIV to 1 kHz. Re-establish a signal reference level as described previously.

n. Check the −80 to −90 dBm gain accuracies by repeating the process previously described.

o. The remaining 10 dB of gain range cannot be checked accurately because of baseline noise. It is, however, directly related to the −70 dBm to −80 dBm check.

7. Check Display Accuracy (±1.0 dB/10 dB to a maximum cumulative error of ±2.0 dB over the 80 dB window and ±0.4 dB/2 dB to a maximum cumulative error of ±1.0 dB over the 16 dB window. LIN mode is 5% of full scale)

a. Test equipment setup is shown in Fig. 3-3. Apply a +10 dBm, 100 MHz signal to the RF INPUT and set the front-panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	10 MHz
REF LEVEL	+10 dBm
MIN RF ATTEN	0 dB
RESOLUTION BANDWIDTH	1 MHz
TIME/DIV	Auto
Vertical Display	10 dB/DIV
Video Filter	NARROW
Digital Storage	VIEW A/VIEW B

b. Tune the FREQUENCY to center the applied signal on screen. Reduce the FREQ SPAN/DIV and RESOLUTION BANDWIDTH to 10 kHz. Carefully adjust the generator output so the signal level is at the top graticule line.

c. Add external attenuation in 10 dB steps for a total of 80 dB and note that the signal steps down screen in 10 dB (±1.0 dB) steps. Maximum cumulative error should not exceed 2.0 dB over the display window.

d. Return the external attenuation to 0 dB and change the Vertical Display to 2 dB/DIV. Set the FREQ SPAN/DIV to 20 kHz and the RESOLUTION BANDWIDTH to 100 kHz. Adjust the signal amplitude to the top graticule line with the generator output control.

e. Repeat the procedure to check the accuracy of the 2 dB steps by adding external attenuation in 2 dB steps for a total of 16 dB. Deviation should not exceed ±0.4 dB/2 dB. Maximum cumulative deviation should not exceed ±1.0 dB over the 16 dB window.

f. Return the external attenuation to 0 dB. Change the Vertical Display to LIN. Adjust the signal generator output for a full screen display.

g. Add 6 dB of external attenuation. Note that the signal amplitude decreases half screen to 4, ±0.4 divisions.

h. Add an additional 6 dB of attenuation. Note signal amplitude decreases to 2, ±0.4 divisions or half amplitude.

i. Add another 6 dB of attenuation. Signal amplitude should decrease to 1.0, ±0.4 divisions.

j. Return the Vertical Display to 10 dB/DIV and disconnect the signal to the RF Input. Turn Video Filter OFF.

8. Check Input 1 dB Compression Level (−18 dBm with MIN RF ATTEN set to 0 dB and MIN NOISE On)

a. Test equipment setup is shown in Fig. 3-4. Apply a 100 MHz 0 dBm signal from the signal generator through 1 dB and 10 dB step attenuators (set at 20 dB) to 496/496P RF INPUT. Apply the signal from the 10 MHz IF port (bnc connector on the rear of the 496/496P) through a second pair of 1 dB and 10 dB step attenuators (set at 0 dB) to the RF input of a second spectrum analyer. Set the front-panel controls of the 496/496P as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	1 MHz
REF LEVEL	−20 dB
MIN RF ATTEN	0 dB
MIN NOISE	On
AUTO RESOLUTION	On
TIME/DIV	AUTO
Vertical Display	10 dB/DIV
Digital Storage	VIEW A/VIEW B

b. Center the displayed 100 MHz signal. Adjust the level of the signal generator for an eight-division display, with the top of the signal touching the top of the screen.

c. Tune the second analyzer to 10 MHz, center the signal, and choose the widest RESOLUTION BANDWIDTH setting (1 MHz or 300 kHz). Select 2 dB/DIV and use the REF LEVEL control for a four-division display, with the top of the signal touching the center graticule line.

d. Decrease the attenuation of the 100 MHz RF signal by 1 dB and increase the attenuation of the 10 MHz IF signal by 1 dB. If both values of attenuation are changed at the same time, there will be no immediate change in the signal level observed on the second analyzer.

e. Continue to decrease the attenuation of the RF signal and increase the attenuation of the IF signal in 1 dB steps. At some point the amplitude of the display in the second analyzer will fall 1 dB below the original center-screen level. Note the setting of the 100 MHz RF attenuators; this is the

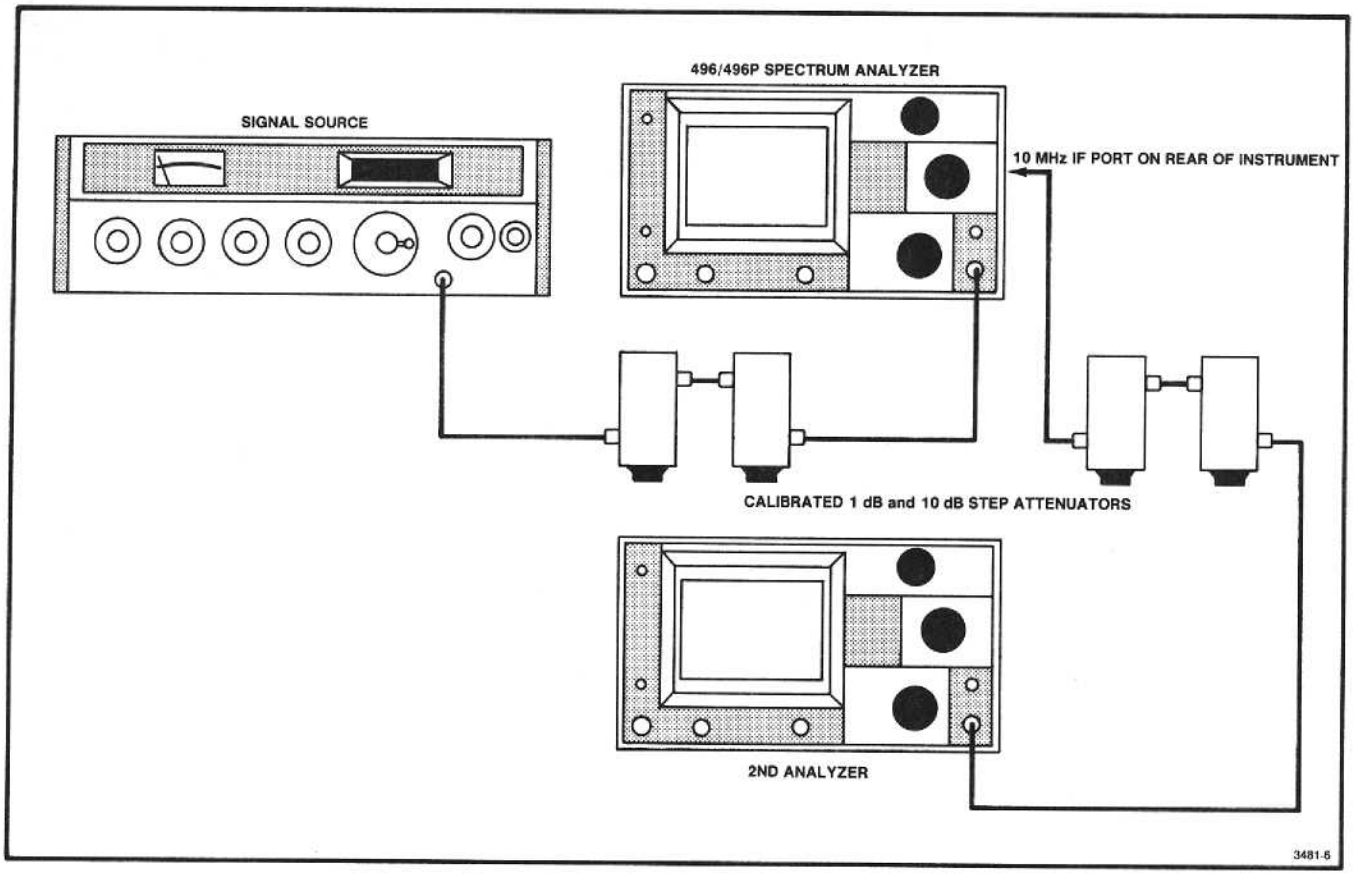


Fig. 3-4. Test equipment setup for checking input 1 dB compression level.

Input 1 dB Compression Level in dBm. (This must be ≥ -18 dBm.)

f. De-activate ZERO SPAN on the 496/496P.

9. Check Gain Variations between Resolution Bandwidths ($\leq$ 0.5 dB)

a. Apply the calibrator signal to the RF INPUT and set the front-panel controls as follows:

FREQUENCY	200 MHz
FREQ SPAN/DIV	20 MHz
REF LEVEL	−20 dBm
MIN RF ATTEN	0 dB
RESOLUTION BANDWIDTH	1 MHz
TIME/DIV	AUTO
Vertical Display	2 dB/DIV
Video Filter	Off
Digital Storage	VIEW A/VIEW B
PEAK/AVERAGE	AVERAGE

NOTE

If digital storage is used, the PEAK/AVERAGE control must be in the AVERAGE mode to measure amplitudes of the 1 MHz, 100 kHz, and 10 kHz resolution bandwidths and in the PEAK mode to measure the amplitude of the 1 kHz and 100 Hz bandwidths.

b. Tune the 200 MHz calibrator marker to center screen and reduce the FREQ SPAN/DIV to 500 kHz. Activate the FINE REFERENCE LEVEL function and adjust the REF LEVEL for a signal amplitude of six divisions.

c. Change the RESOLUTION BANDWIDTH to 100 kHz and the FREQ SPAN/DIV to 100 kHz. Check that the amplitude change is not more than 0.5 dB.

d. Repeat the procedure for 10 kHz resolution bandwidth with a FREQ SPAN/DIV of 10 kHz.

e. Change the PEAK/AVERAGE control to PEAK mode and repeat the procedure for the 1 kHz resolution bandwidth. Reduce the SPAN/DIV to 1 kHz.

f. Repeat the procedure to check amplitude variation for resolution bandwidths of 100 Hz with a FREQ SPAN/DIV of 500 Hz. (Video Filter must be off to maintain a calibrated display at 100 Hz resolution.) Reduce the FREQ SPAN/DIV to 100 Hz.

g. Repeat the procedure again for the 30 Hz resolution bandwidth.

10. Check Frequency Response (±1.5 dB)

Frequency response is the amplitude deviation, over a given frequency range, of a constant level input signal measured at the analyzer center frequency. It includes input attenuation and mixer gain variations. Measurement requires many small incremental checks across the spectrum analyzer frequency range. Because the frequency range of the 496/496P is very wide, measuring the response in small increments is a slow process. A more expeditious method using a sweep oscillator is described in this procedure. Table 3-3 describes the equipment recommended for this procedure.

Table 3-3
RECOMMENDED TEST EQUIPMENT

Equipment	Recommended
Signal Generator 10 kHz—10 MHz	HP654A
Signal Generator 10 MHz—2.4 GHz	HP8620C Sweeper with 86222B RF Plug-In Unit
Power Meter 0 to −10 dBm, 100 kHz—4.2 GHz	HP435B with 8482A Sensor
Power Divider	HP1167A
3 dB Attenuator, SMA Connectors	Weinschel Model 4M
High Performance 50 Ω Cable, SMA Connectors	See Equipment Required list
50 Ω Coaxial Cable, bnc Connectors	See Equipment Required list
Adapter N male-to-SMA male	See Equipment Required list

NOTE

Loss of signal through interconnecting cables becomes significant above 1 GHz; therefore, use short (25 inch or less) semi-rigid cable with precision fittings to interconnect the test equiment. Precision matching terminations and power dividers are used to minimize reflections.

a. Test equipment setup is shown in Fig. 3-5. Set the front-panel controls as follows:

FREQUENCY	5 MHz
FREQ SPAN/DIV	1 MHz
REF LEVEL	0 dBm
MIN RF ATTEN	30 dB
AUTO RESOLTUION	On
TIME/DIV	20 ms
Vertical Display	10 dB/DIV
Digital Storage	VIEW A OFF
	VIEW B ON
	SAVE A ON
PEAK/AVERAGE	ccw

b. Apply the output of a constant level and calibrated 100 kHz to 10 MHz signal generator, to the RF input of the 496/496P. Set the generator frequency to 100 kHz and its output for about −10 dBm.

c. Adjust the REF LEVEL so the amplitude of the 100 kHz signal is about half screen, in the 2 dB/DIV mode. Activate MAX HOLD.

d. Slowly tune the frequency of the signal generator from 100 kHz to 10 MHz, monitoring the output to ensure that it remains constant. Note the frequency response (amplitude deviation above and below the average). Frequency response deviation should not exceed ±1.5 dB. Deactivate MAX HOLD.

e. Replace the 100 kHz to 10 MHz signal source with a 0.01 to 2.4 GHz sweep oscillator and connect the test equipment as shown in Fig. 3-6. The output of the sweep generator is applied through a 3 dB attenuator and high performance coaxial cable to a power divider. Connect one end of the power divider directly to the RF INPUT and the other output to the sensor for the power meter.

f. Change the FREQ SPAN/DIV to MAX. On the sweep generator, select a 1 GHz cw marker and adjust the output for about −6 dBm on the power meter. With the 496/496P Vertical Display in the 2 dB/DIV mode, adjust the REF LEVEL so the signal level is about half screen.

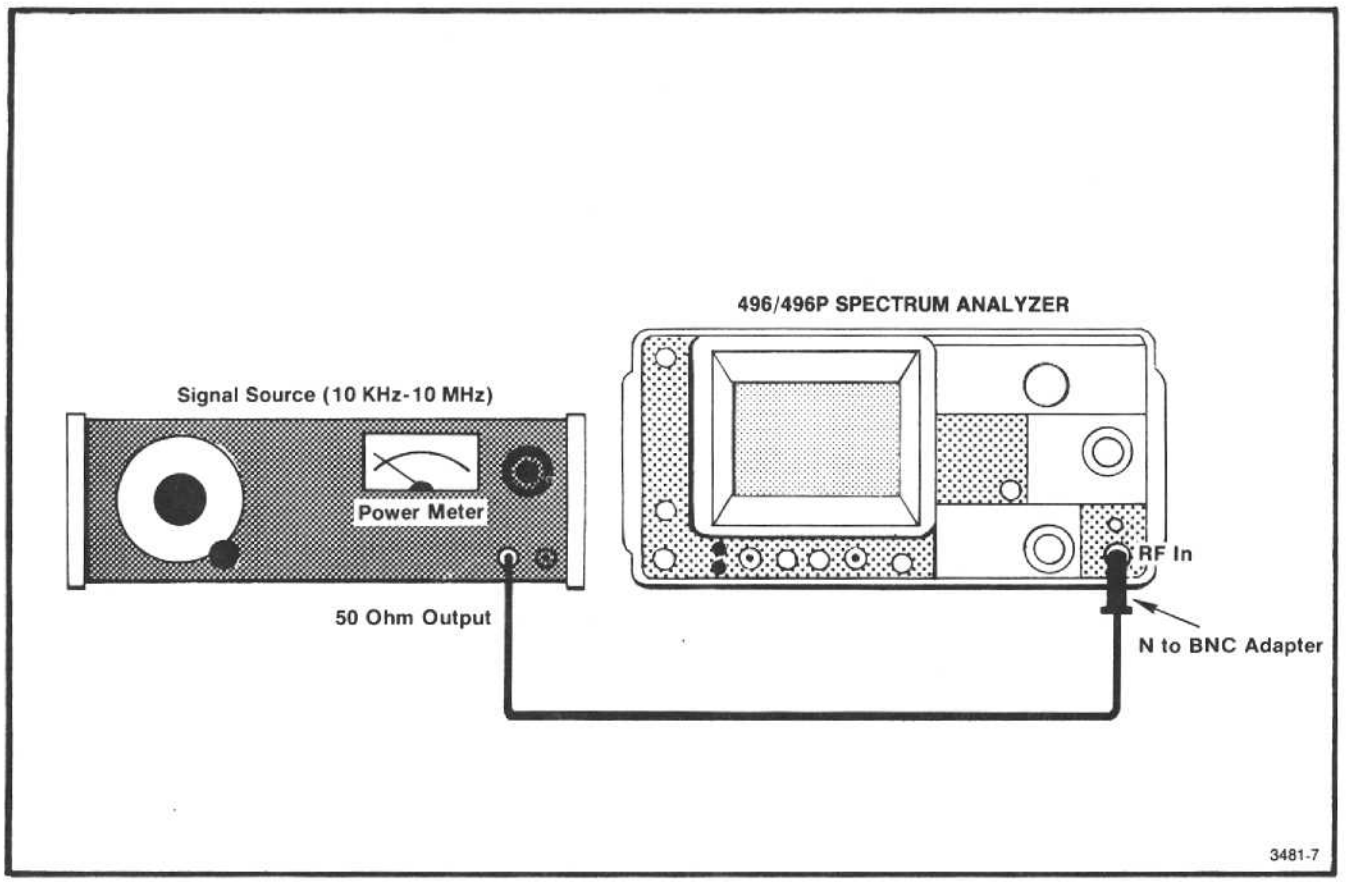


Fig. 3-5. Test equipment setup for checking the 0–10 MHz frequency response.

g. Change the generator sweep mode to automatic internal sweep and set the sweep time to 100 seconds or the slowest available sweep time. Activate MAX HOLD.

h. Check the frequency response as the sweep generator sweeps across the 0.01 to 2.4 GHz span. Deviation must not exceed ±1.5 dB up to 1.8 GHz (upper limit of 496/496P). Refer to Fig. 3-7.

i. Deactivate MAX HOLD and SAVE A, and activate VIEW A. Rotate PEAK/AVERAGE fully cw.

11. Check Frequency Span/Div Accuracy (±5% of the selected span/div)

Span accuracy is checked by noting the displacement of calibrated markers from their respective graticule line over the center eight divisions of the screen. Range is in a 5-10-20 sequence and covers the range from 50 Hz/div to 200.

a. Set the front-panel controls as follows:

FREQUENCY	1 GHz
FREQ SPAN/DIV	200 MHz
REF LEVEL	−30 dBm
MIN RF ATTEN	0 dB
AUTO RESOLUTION	On
TIME/DIV	AUTO
Vertical Display	10 dB/DIV
Video Filter	Off
Digital Storage	VIEW A/VIEW B

b. Connect the CAL OUT to the RF INPUT and adjust the FREQUENCY to align the 100 MHz markers so the 200 MHz/div accuracy can be measured over the center eight divisions of the display (two markers per division). It may be necessary to change the REF LEVEL to obtain adequate markers. Maximum deviation must not exceed 10 MHz/div (0.25 minor divisions).

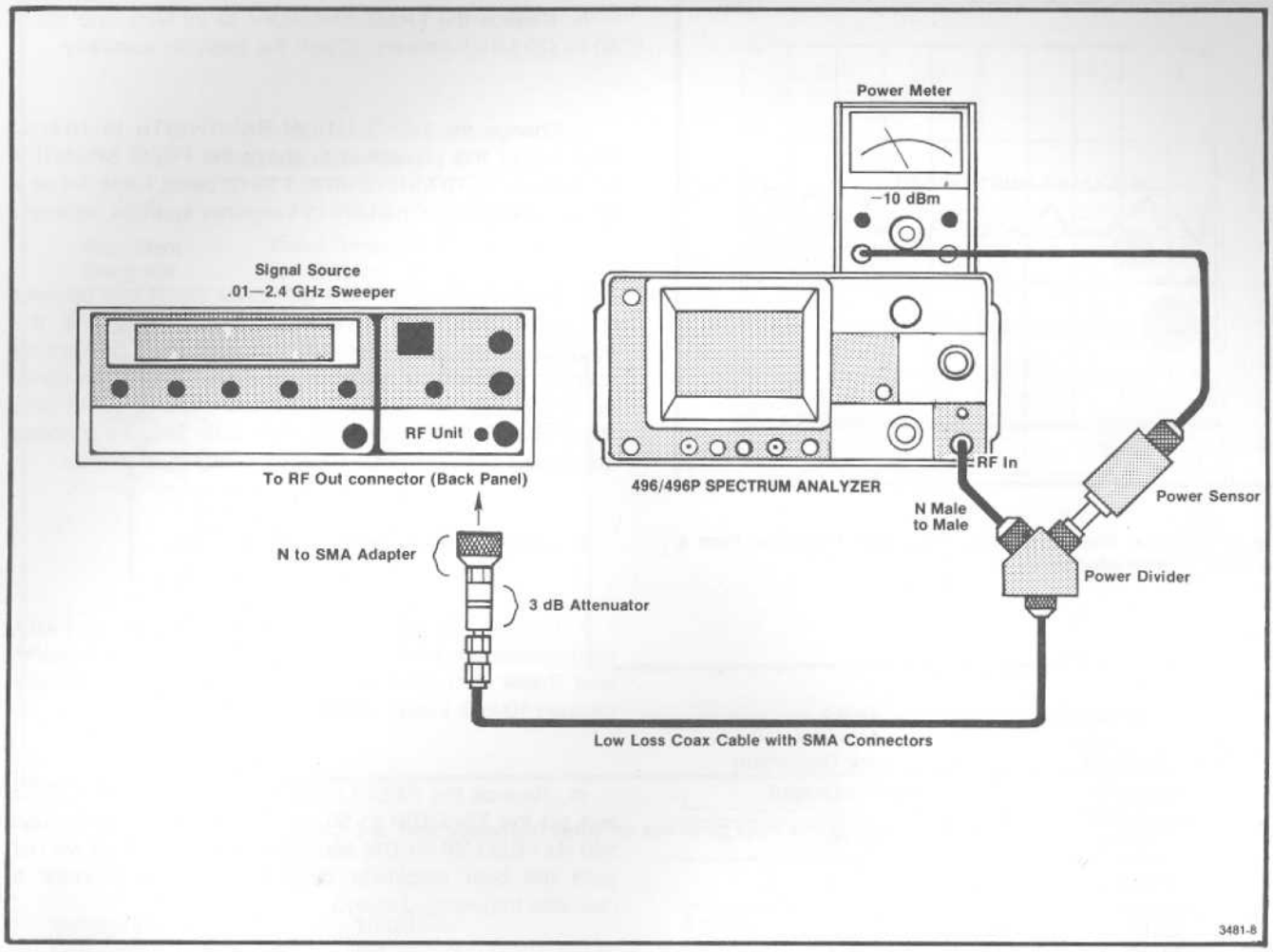


Fig. 3-6. Test equipment setup for measuring the 0.01–1.8 GHz frequency response.

c. Change the FREQ SPAN/DIV to 100 MHz and check the span/div accuracy. Error must not exceed 5% of the span/div or 5 MHz/div.

d. Re-establish a REF LEVEL of +20 dBm and tune the FREQ to 500 MHz. Reduce the SPAN/DIV to 50 MHz and select a RESOLUTION BANDWIDTH of 1 MHz.

e. Remove the CAL OUT from the RF INPUT and connect the Marker Output of the time mark generator to the RF INPUT. Set the FREQ SPAN/DIV to 50 MHz, and apply 20 ns time markers to the 496/496P input.

f. Tune toward the lower frequency end of the band until 50 MHz markers are displayed over the center eight divisions (10 MHz markers will appear between each 50 MHz marker).

g. Check the accuracy of the 50 MHz/div span.

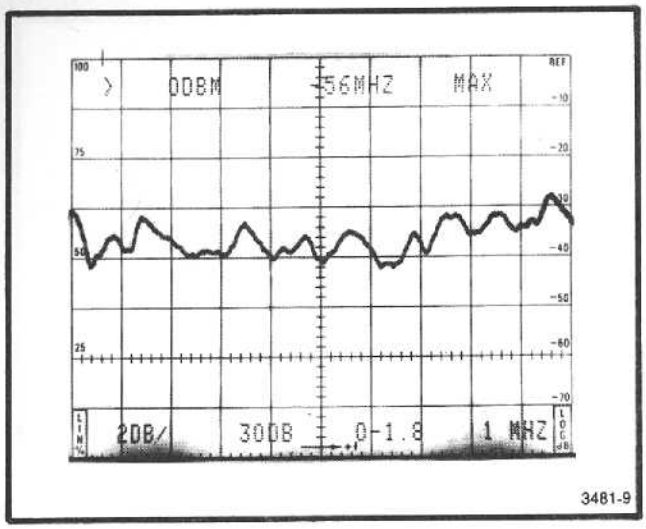


Fig. 3-7. Typical display showing frequency response from a sweeping signal source.

Table 3-4

SPAN/DIV vs TIME MARKERS

FREQUENCY SPAN/DIV	Time Mark Generator Marker Output
20 MHz	50 ns
10 MHz	.1 μs
5 MHz	2 μs
2 MHz	.5 μs
1 MHz	1 μs
500 kHz	2 μs
200 kHz	5 μs
100 kHz	10 μs
50 kHz	20 μs
20 kHz	50 μs
10 kHz	.1 ms
5 kHz	.2 ms
2 kHz	.5 ms
1 kHz	1 ms
500 Hz	2 ms
200 Hz	5 ms
100 Hz	10 ms
50 Hz	20 ms

h. Reduce the FREQ SPAN/DIV to 20 MHz and apply 50 ns (20 MHz) markers. Check the span/div accuracy.

i. Change the RESOLUTION BANDWIDTH to 10 kHz, then repeat this procedure to check the FREQ SPAN/DIV accuracy from 10 MHz down to 1 MHz, using Table 3-4 as a guide to relate time markers to frequency span/div settings.

j. Remove the time mark generator signal and connect the comb generator to the RF INPUT. Modulate the 500 MHz comb generator with 2 μs (500 kHz) markers by applying the Marker Output to the Pulse Input of the comb generator. Change the REF LEVEL to −20 dBm and tune the FREQUENCY toward 500 MHz until 500 kHz markers are displayed over the center eight divisions of display.

k. Check the 500 kHz/div span accuracy.

l. Reduce the RESOLUTION BANDWIDTH to 1 kHz, then reduce the FREQ SPAN/DIV setting and time marks (see Table 3-4) to check the accuracy for the 50 kHz through 10 kHz FREQ SPAN/DIV selections.

m. Reduce the RESOLUTION BANDWIDTH to 100 Hz and set the TIME/DIV to 50 ms. Check the 5 kHz through 500 Hz FREQ SPAN/DIV accuracy. (This procedure will not yield the best amplitude display but it will produce a readable frequency display.)

n. Reduce the RESOLUTION BANDWIDTH to 30 Hz and set the TIME/DIV to 100 ms. Check the 200 to 50 Hz FREQ SPAN/DIV accuracy.

12. Check Time/Div Accuracy (accuracy within 5% of time selected)

a. Test equipment setup is the same as that required for step 11.

b. Apply the Marker Output from the time mark generator directly to the RF INPUT and the Trigger output to the 496/496P EXT TRIG connector on the back panel. Set the controls as follows:

FREQUENCY	≈1 MHz
FREQ SPAN/DIV	100 kHz
REF LEVEL	−20 dBm
MIN RF ATTEN	20 dB
RESOLUTION BANDWIDTH	10 kHz
TIME/DIV	50 ms

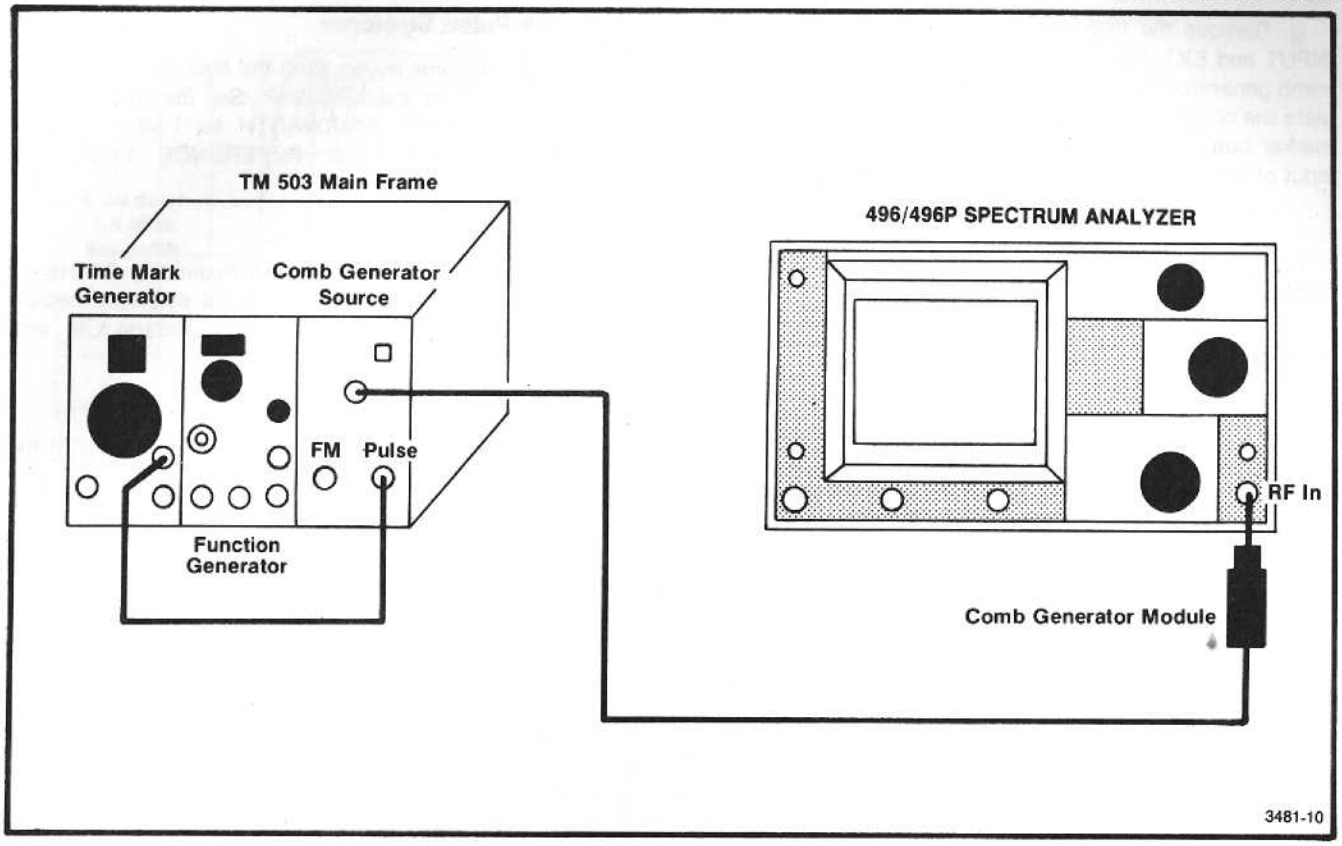


Fig. 3-8. Test equipment setup for checking span and timing accuracy.

Vertical Display	10 dB/DIV
Video Filter	Off
Digital Storage	VIEW A/VIEW B
Triggering	EXT

c. Apply 50 ms time markers. Tune the FREQUENCY toward 0 Hz as the FREQ SPAN/DIV is reduced to zero, so time markers are displayed on the time domain display (see Fig. 3-9). Adjust FREQUENCY if necessary.

d. Use the horizontal position control to align a marker on the 1st graticule line; then check the displacement of markers from their respective positions over the center eight divisions. Individual marker displacement must not exceed 5% or 2 minor divisions.

e. Check the accuracy of the 50 ms to 2 ms TIME/DIV settings by applying appropriate markers for each setting and note the displacement as described in part d of this step.

f. Deactivate the Digital Storage. Change the RESOLUTION BANDWIDTH to 1 MHz and adjust FREQUENCY for a satisfactory display of the time markers. Check the accuracy of the 1 ms and 20 μs TIME/DIV selections.

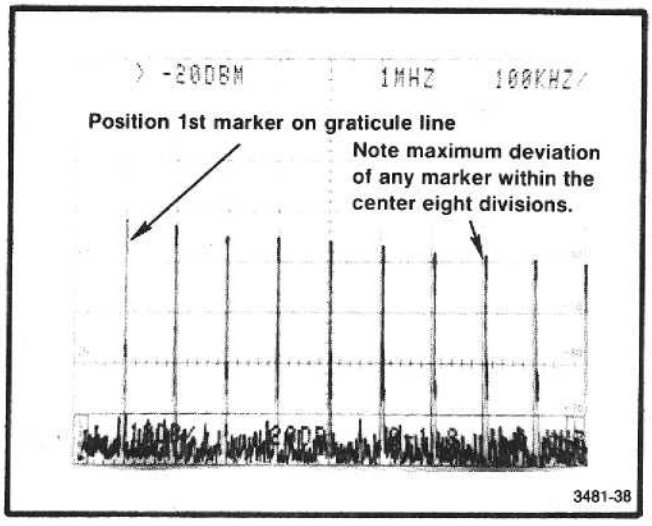


Fig. 3-9. Display to illustrate how timing accuracy is checked.

g. Remove the time mark generator output to the RF INPUT and EXT TRIG input of the 496/496P. Connect the comb generator 500 MHz signal to the RF INPUT and modulate the comb generator with .1 s markers by applying the marker output from the time mark generator to the Pulse input of the comb generator.

h. Set the TIME/DIV to .1 s and active INT Triggering. Change the FREQ SPAN/DIV to 50 MHz and adjust the FREQUENCY to center the 500 MHz comb signal. Activate VIEW A, VIEW B.

i. Change the REF LEVEL to −30 dBm, then reduce the RESOLUTION BANDWIDTH to 1 kHz and the FREQ SPAN/DIV to 100 kHz while adjusting the FREQUENCY to optimize time markers on the display. Reduce the FREQ SPAN/DIV to zero.

j. Check the accuracy of the .1 s to 5 s sweep rates by applying appropriate markers to modulate the comb generator signal as the TIME/DIV selector is changed over this range.

13. Check Delta Frequency Readout Accuracy (±5% of readout frequency)

a. Apply 2 μs time marks from the time mark generator to the RF INPUT of the 496/496P. Set the front-panel controls as follows:

FREQUENCY	1 MHz
FREQ SPAN/DIV	100 kHz
REF LEVEL	+20 dBm
MIN RF ATTEN	0 dB
RESOLUTION BANDWIDTH	10 kHz
TIME/DIV	AUTO
Vertical Display	10 dB/DIV
Video Filter	Off
Digital Storage	VIEW A/VIEW B

b. Tune one of the marks to center screen. Change the FREQ SPAN/DIV to 50 kHz and tune the FREQUENCY control counterclockwise until the display stops moving.

c. Tune the closest marker to a graticule line. Press ΔF and tune to the next higher marker; note the frequency on the Delta F readout. Turn off ΔF.

d. Repeat the previous part 5 times.

e. The deviation from 500 kHz should not exceed ±25 kHz (±5% of 500 kHz) on any of the six measurements.

14. Check Pulse Stretcher

a. Apply 1 ms time marks from the time mark generator to the RF INPUT of the 496/496P. Set the TIME/DIV to 500 μs, RESOLUTION BANDWIDTH to 1 MHz, Vertical Display to 2 dB/DIV, and REFERENCE LEVEL to −10 dBm.

b. Tune the FREQUENCY to approximately 0 MHz so the amplitude of the markers is near full screen. If necessary, change REF LEVEL. Set Digital Storage Off, and SPAN/DIV to ZERO.

c. Activate PULSE STRETCHER and check that it extends the fall time of the markers.

15. Check Resolution Bandwidth and Shape Factor (bandwidth within 20% of that selected, shape factor 7.5:1 or less; 15:1 or less for 30 Hz bandwidth)

a. Apply the CAL OUT signal to the RF INPUT. Set the front-panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	500 kHz
REF LEVEL	−20 dBm
MIN RF ATTEN	0 dB
RESOLUTION BANDWIDTH	1 MHz
TIME/DIV	AUTO
Vertical Display	2 dB/DIV
Video Filter	Off
Digital Storage	VIEW A/VIEW B
MIN NOISE	On

b. Adjust the FREQUENCY to center the calibrator signal on screen and measure the −6 dB bandwidth (see Fig. 3-10A). Bandwidth must equal 1 MHz ±200 kHz.

c. Change the Vertical Display mode to 10 dB/DIV.

d. Estimate the −60 dB bandwidth (see Fig. 3-10B). Calculate the shape factor (60/6 dB bandwidth ratio). Shape factor should equal 7.5:1 or less.

e. Switch the RESOLUTION BANDWIDTH to 100 kHz and the FREQ SPAN/DIV to 100 kHz. Check the bandwidth and shape factor of the 100 kHz filter by repeating the foregoing procedure.

f. Check the resolution bandwidth and shape factor for the remaining RESOLUTION BANDWIDTH selections. Decrease the FREQ SPAN/DIV as necessary to check each

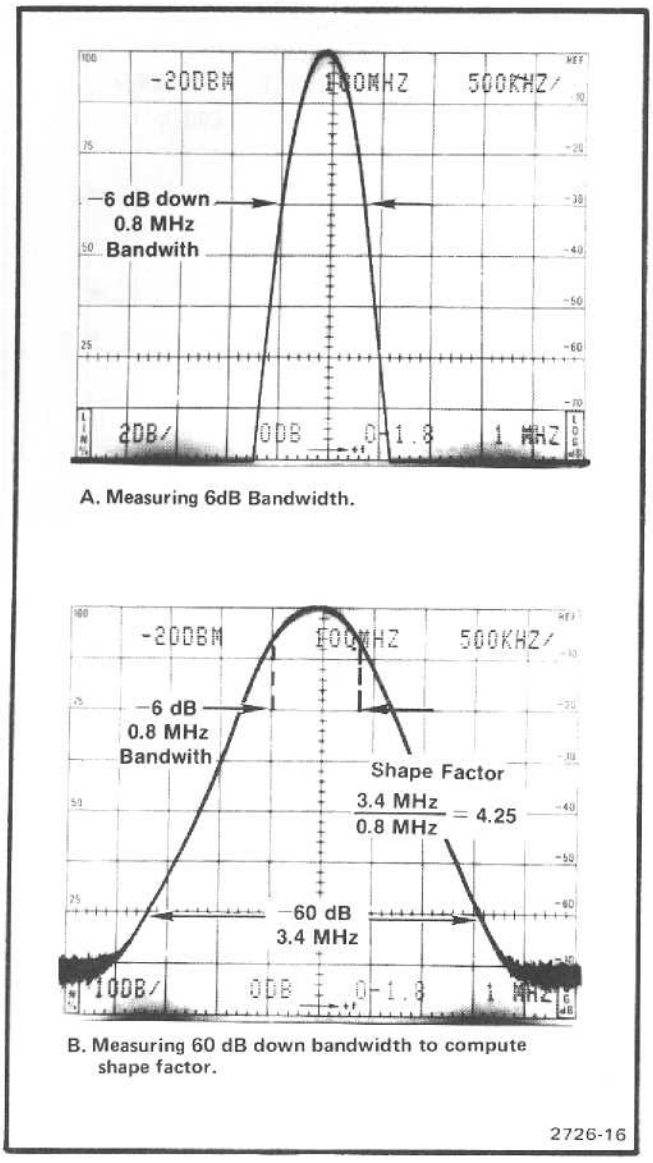


Fig. 3-10. Measuring resolution bandwidth and shape factor.

selection. Bandwidth must be within 20% of the bandwidth selected and the shape factor 7.5:1 or less; except for 30 Hz RESOLUTION BANDWIDTH, where the shape factor must be 15:1 or less.

g. Deactivate MIN NOISE.

16. Check Equivalent Input Noise Sensitivity

NOTE

Sensitivity is specified according to the input or average noise level. The 496/496P calibrator is the reference used to calibrate the display.

a. Set the front-panel controls as follows:

FREQUENCY	≈500 MHz
FREQ SPAN/DIV	10 kHz
REF LEVEL	−20 dBm
MIN RF ATTEN	0 dB
RESOLUTION BANDWIDTH	1 MHz
TIME/DIV	0.5 s
Vertical Display	10 dB/DIV
Video Filter	WIDE
Digital Storage	VIEW A/VIEW B
PEAK/AVERAGE cursor	Top of screen (control fully cw)

b. Calibrate the reference level and display range as per Operating Instructions; then disconnect the calibrator signal from the RF INPUT. Change the REF LEVEL to −30 dBm.

c. Check the noise level below the −30 dBm reference level. Noise level must be −85 dBm or better.

d. Check the noise level for 100 kHz resolution bandwidths. Compare this level with the characteristic in the following listing.

Average Noise Level dBm (max)

(Frequency Range; 100 kHz–1.8 GHz) Resolution Bandwidth

1 MHz – 85
100 kHz – 95
10 kHz – 105
1 kHz – 115
100 Hz – 123
30 Hz – 126

e. Change the REF LEVEL to −60 dBm and reduce TIME/DIV to 2 s.

f. Check the average noise level for 1 kHz, 100 Hz, and 30 Hz resolution bandwidths against the listing in part d.

g. Turn Video Filter Off.

17. Check Frequency Drift (Phaselock On: within 3.3 kHz over 10 minutes after 30 minute warm up, within 330 Hz over 10 minutes after 1 hour warm up. Phaselock Off: within 33 kHz over 10 minutes after 1 hour warm up)

NOTE

This measurement and residual FM are dependent on oscillator stability. The instrument must therefore have a 30 minute warm-up period and a settling time of 10 minutes after retuning more than 50 kHz.

a. Set the front-panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	10 MHz
REF LEVEL	−20 dBm
MIN RF ATTEN	0 dB
MIN NOISE	Off
AUTO RESOLUTION	On
TIME/DIV	AUTO
Vertical Display	10 dB/DIV
Digital Storage	VIEW A/VIEW B

b. Connect the CAL OUT signal to the RF INPUT. Tune the calibrator mark to center screen. Reduce the FREQ SPAN/DIV to 1 MHz and press DEGAUSS to remove any residual magnetism as the signal is centered.

c. Adjust the REF LEVEL for a signal amplitude of 7 divisions. Decrease the FREQ SPAN/DIV to 1 kHz keeping the signal centered as necessary with the FREQUENCY control. Confirm that the PHASELOCK light is on.

d. Activate VIEW A, VIEW B, and MAX HOLD.

e. Check the signal stability or drift over the specified time period. Drift will appear as the width of the response less the resolution bandwidth (see Fig. 3-11) after the specified time period.

f. Deactivate MAX HOLD.

g. Repeat this procedure after 1 hour of operation. When part c is repeated decrease the FREQ SPAN/DIV to 100 Hz. Check that the drift does not exceed 330 Hz over 10 minutes.

h. Repeat the procedure again. When performing part c, increase the FREQ SPAN/DIV to 10 kHz and cancel PHASELOCK. Check that the drift does not exceed 33 kHz over 10 minutes.

18. Check Residual FM (within 1 kHz peak to peak over 20 milliseconds without phaselock, within 10 Hz peak to peak over 20 milliseconds with phaselock)

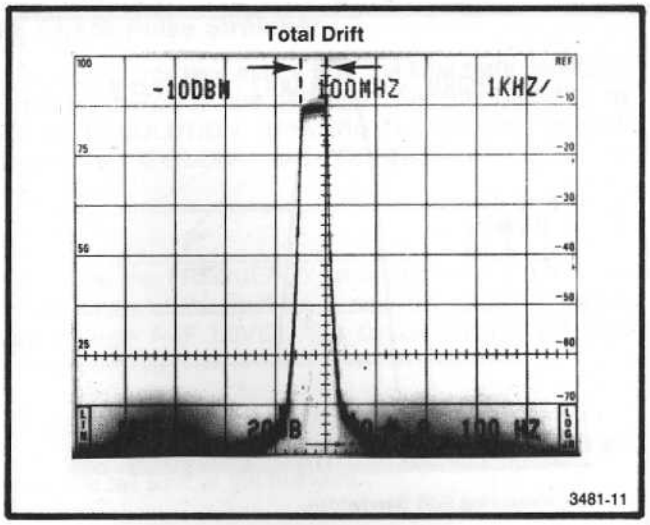


Fig. 3-11. Digital stored display showing drift.

a. Set the front-panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	10 MHz
REF LEVEL	−20 dBm
MIN RF ATTEN	0 dB
MIN NOISE	Off
AUTO RESOLUTION	On
TIME/DIV	AUTO

b. Center the calibrator signal with the FREQUENCY control and decrease the FREQ SPAN/DIV to 10 kHz. Cancel PHASELOCK and recenter the calibrator signal with the FREQUENCY control.

c. Set the RESOLUTION BANDWIDTH to 10 kHz and the Vertical Display to LIN. Activate FINE and adjust REF LEVEL for a full screen display.

d. Position the calibrator signal with the FREQUENCY control so the slope (horizontal versus vertical excursion) can be measured as illustrated in Fig. 3-12A. SINGLE SWEEP is a useful way of freezing the display for measurement. Press FREE RUN to cancel SINGLE SWEEP.

e. Press ZERO SPAN (time domain operation), rotate TIME/DIV to 20 ms, and adjust FREQUENCY to position the display near center screen as shown in Fig. 3-12B. Note the peak-to-peak deviation of the display within any given horizontal division. Scale the vertical deflections according to the slope calculated in the previous step. Residual FM must not exceed 1 kHz for 20 ms. Cancel ZERO SPAN.

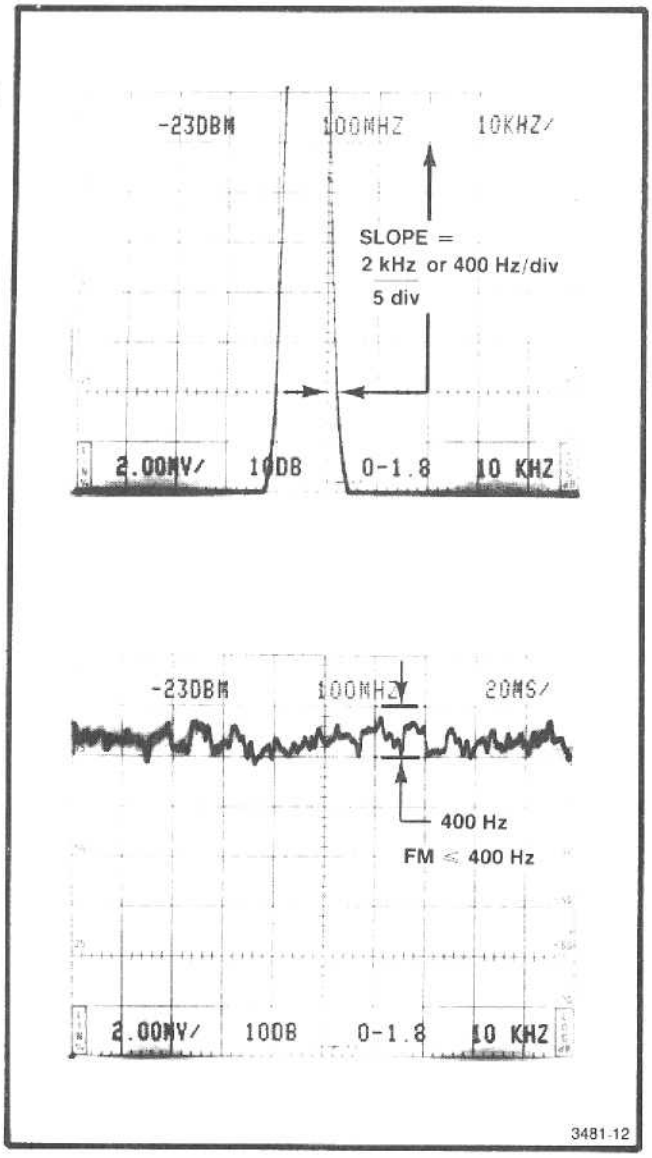


Fig. 3-12. Measuring residual (incidental) FM.

f. Switch TIME/DIV to AUTO and activate PHASELOCK. Increase FREQ SPAN/DIV to bring the signal on screen, then reduce the span to 100 Hz/div and the RESOLUTION BANDWIDTH to 100 Hz. Keep the signal centered with the FREQUENCY control.

g. Calculate the slope as described in part d.

h. Press ZERO SPAN, rotate TIME/DIV to 20 ms, and adjust FREQUENCY to position the display near center screen. Note the peak-to-peak deviation within any given horizontal division. Scale the vertical deflections according to the previously calculated slope. Residual FM must not exceed 10 Hz for 20 ms. Cancel ZERO SPAN.

19. Check Intermodulation Distortion (Min Distortion Mode: Third-order IM distortion is −70 dBc below any two on-screen signals within any frequency span)

a. Set the front panel controls as follows:

FREQUENCY	Within 2 MHz of test frequencies
FREQ SPAN/DIV	5 MHz
REF LEVEL	−30 dBm
MIN RF ATTEN	0 dB
MIN NOISE	Off
RESOLUTION BANDWIDTH	100 kHz
TIME/DIV	AUTO
Vertical Display	10 dB/DIV
Digital Storage	VIEW A/VIEW B

b. Apply two signals from two 50 Ω sources, separated about 2 MHz. Apply the signals through 20 dB attenuators (for isolation), a bnc T connector, and bnc-to-n adapter, to the 496/496P RF INPUT (test equipment setup is shown in Fig. 3-13).

c. Adjust the output of the signal generators for two −30 dBm, or full screen signals, on the 496/496P display. Decrease the signal frequency separation to 1 MHz and the FREQ SPAN/DIV to 500 kHz. Set the RESOLUTION BANDWIDTH to 10 kHz.

d. Check third order intermodulation products (see Fig. 3-14). Ensure that third order products are −70 dB or more down from the input signal level.

NOTE

Intermodulation products may not appear unless the input signal level is off screen. Use the VIDEO FILTER and very slow sweep rates to help resolve these sidebands.

e. Decrease signal separation and FREQ SPAN/DIV settings and check again for sidebands. Check IM distortion at other portions of the frequency range. IM distortion should be down at least 70 dBc.

20. Check Harmonic Distortion (−60 dBc for a full screen signal in MIN DISTORTION mode)

a. Set the front-panel controls as follows:

FREQUENCY	Same as generator
FREQ SPAN/DIV	5 MHz
REF LEVEL	−30 dBm

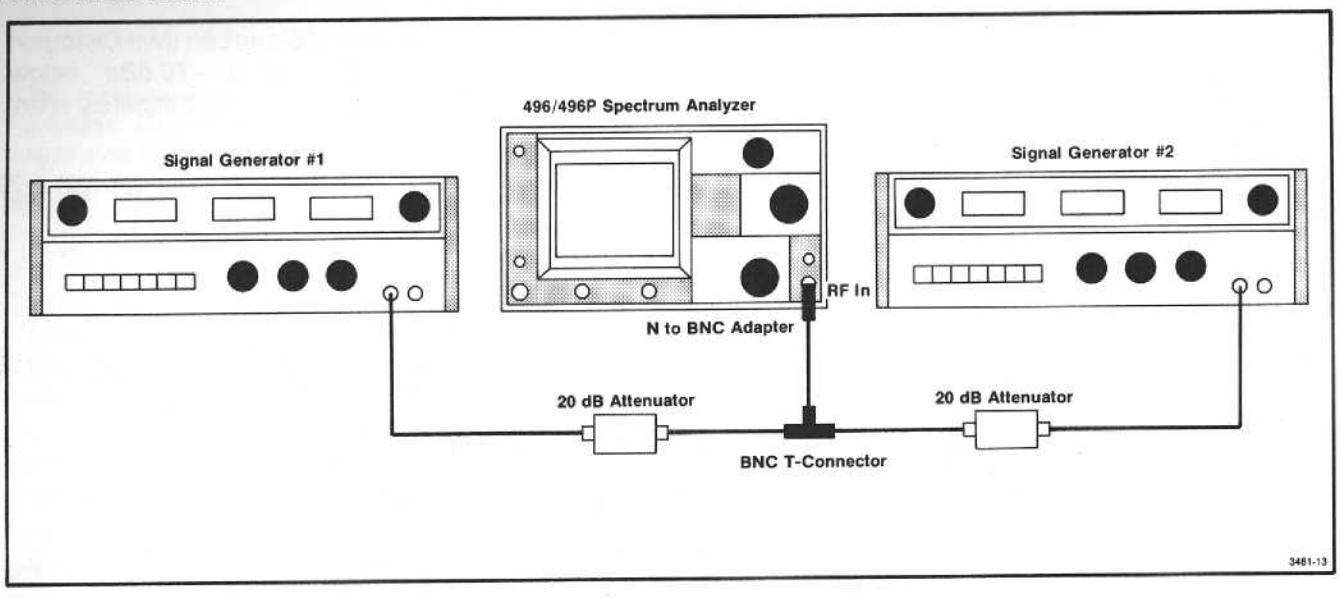


Fig. 3-13. Test equipment setup for measuring intermodulation distortion.

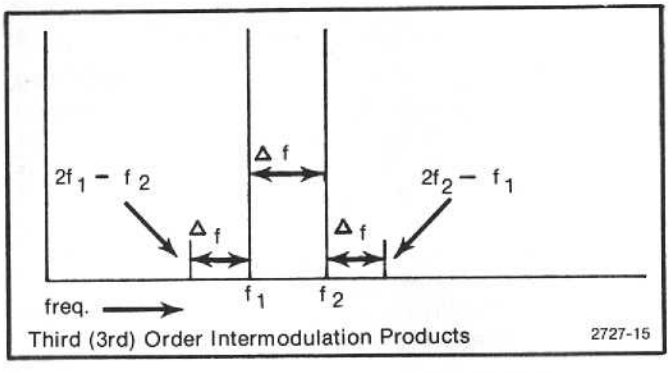


Fig. 3-14. Intermodulation products.

MIN RF ATTEN	0 dB
AUTO RESOLUTION	On
TIME/DIV	AUTO
Vertical Display	10 dB/DIV
Video Filter	WIDE
Digital Storage	VIEW A/VIEW B

b. Apply the output of the signal generator, through a lowpass or bandpass filter (with a minimum of 40 dB rolloff to attenuate multiples of the generator frequency), to the 496/496P RF INPUT (see Fig. 3-15). Frequency of the signal generator depends on the frequency characteristics of the filter. Ensure that the REF LEVEL is in the MIN DISTORTION mode.

c. Tune the 496/496P FREQUENCY to the applied signal frequency. Adjust the generator output for a full screen (−30 dBm) signal.

d. Activate ΔF. Adjust the FREQUENCY so the 2nd multiple of the input frequency is centered. Increase the REF LEVEL to −50 dBm, decrease the FREQ SPAN/DIV to 500 kHz and the RESOLUTION BANDWIDTH to 10 kHz.

e. Check the display for harmonic spurii (spurious responses) of the input signal. Harmonic spurii must be down 60 dB or more from the −30 dBm carrier (−40 dB below top of screen).

f. Increase the FREQUENCY to the 3rd harmonic. Check for harmonic spurii. Again responses must be down 40 dB from the top of the screen (60 dBc).

g. Increase the REF LEVEL to −70 dBm, decrease the FREQ SPAN/DIV to 1 kHz and the RESOLUTION BANDWIDTH to 30 Hz. Deactivate the Video WIDE Filter. Check that harmonic spurii are 100 dB or more down from the −30 dBm carrier level.

21. Check Phaselock Noise Sidebands (At least 75 dBc at 30 times Resolution Bandwidth offset from the Center Frequency; at least 70 dBc for 100 Hz or 30 Hz Resolution Bandwidth)

a. Set the front-panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	10 MHz
REF LEVEL	−20 dBm
AUTO RESOLUTION	On
TIME/DIV	AUTO

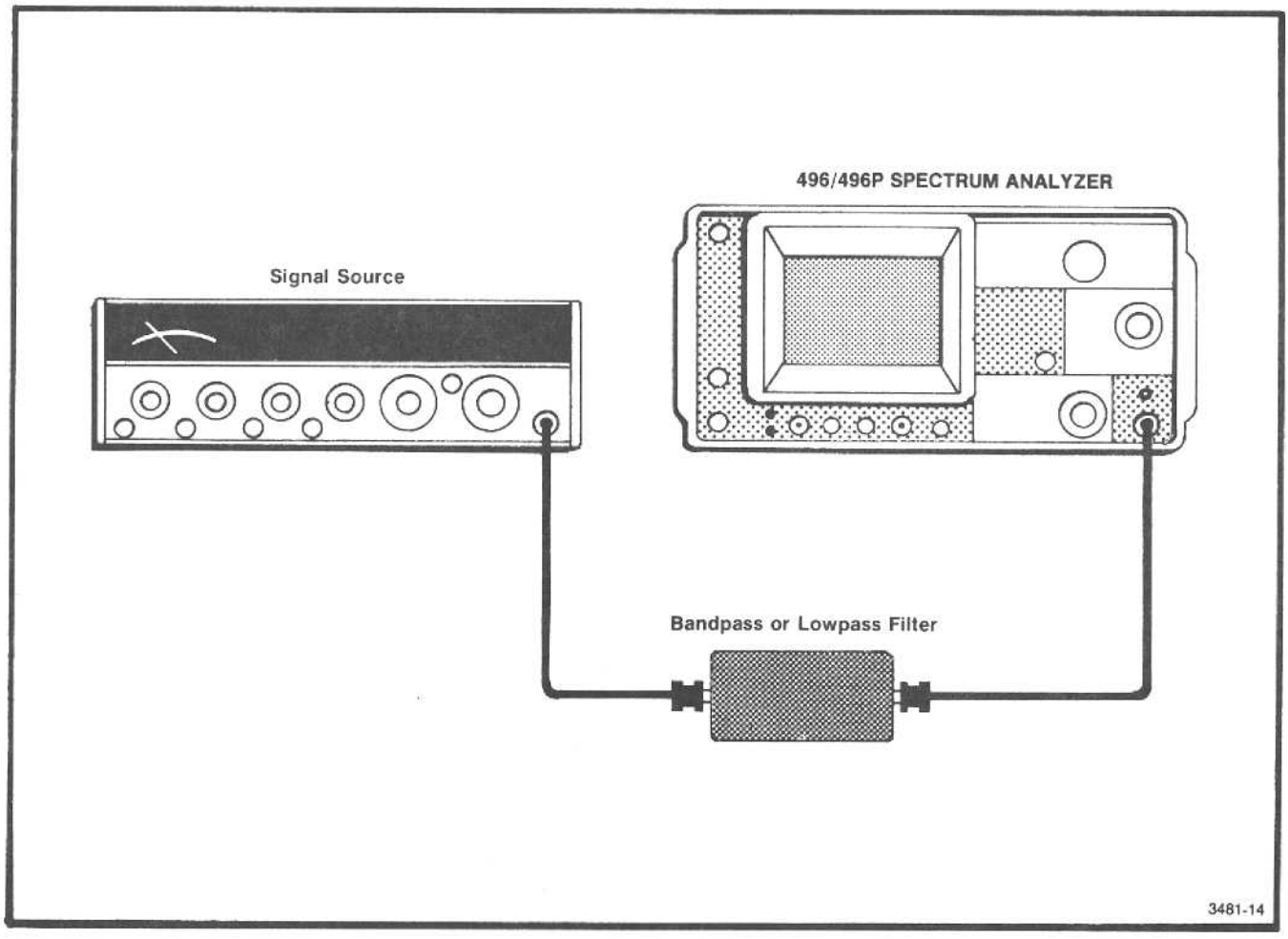


Fig. 3-15. Test equipment setup to check harmonic distortion.

Vertical Display	10 dB/DIV
Digital Storage	VIEW A/VIEW B

b. Apply the CAL OUT to the RF INPUT. Center the marker with the FREQUENCY control. Adjust the REF LEVEL input for a full screen display.

c. Keep the calibrator marker centered as the FREQ SPAN/DIV is reduced to 20 kHz and the RESOLUTION BANDWIDTH is reduced to 1 kHz. Confirm that the PHASELOCK is on.

d. Increase REF LEVEL 20 dB to position the signal peak 20 dB above the reference line. Check the amplitude of noise sidebands 30 kHz away from the calibrator signal (Fig. 3-16). Phaselock sidebands should be 75 dB or more down from the signal level or 55 dB below the top of the screen.

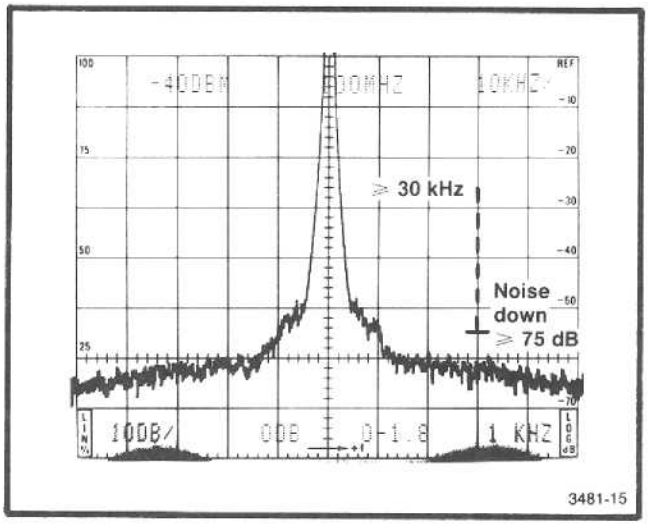


Fig. 3-16. Typical display of phaselock noise.

e. Keep the calibrator marker centered as the FREQ SPAN/DIV is reduced to 2 kHz and the RESOLUTION BANDWIDTH is reduced to 100 Hz.

f. Check the average amplitude of noise sidebands 3 kHz away from the calibrator signal. Phaselock sidebands should be 70 dB or more down from the signal level or 50 dB below the top of the screen.

22. Check Spurious Response Residual (≤ −100 dBm)

a. Remove all signals to the RF INPUT and set the front-panel controls as follows:

FREQUENCY	Multiples of 100 MHz
FREQ SPAN/DIV	10 MHz
REF LEVEL	−50 dBm
MIN RF ATTEN	0 dB
RESOLUTION BANDWIDTH	10 kHz
TIME/DIV	AUTO
Vertical Display	10 dB/DIV
Video Filter	Off
Digital Storage	VIEW A/VIEW B

b. Set the frequency range in 100 MHz increments. Note the amplitude of any spurious response. Spurii amplitude must not exceed −100 dBm. (By activating ΔF after each increment, it is easier to determine 100 MHz increments.)

23. Check Zero Frequency Feedthrough Amplitude (≤20 dBm)

a. Set the front panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	10 MHz
REF LEVEL	−20 dBm
MIN RF ATTEN	0 dB
MIN NOISE	On
AUTO RESOLUTION	On
TIME/DIV	AUTO
Vertical Display	10 dB/DIV
Digital Storage	VIEW A/VIEW B

b. Apply the CAL OUT signal to the RF INPUT. Check that the calibrator signal is at the top of the screen; press 2 dB/DIV and recheck the calibrator signal. If the calibrator signal is not at the top of the screen, perform the initial calibration described under the Turn On Procedure in the Operators manual.

c. Reset the Vertical Display to 10 dB/DIV. Tune the analyzer to the zero frequency spur and press 2 dB/DIV. The zero frequency spur should be −20 dBm or less (spur should not reach the top of the screen). Reset the Vertical Display to 10 dB/DIV.

24. Check Digital Storage

a. Set the front-panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	10 MHz
REF LEVEL	−12 dBm
MIN RF ATTEN	20 dB
RESOLUTION BANDWIDTH	1 MHz
TIME/DIV	AUTO
Vertical Display	2 dB/DIV
Video Filter	Off
Digital Storage	VIEW A

b. With the calibrator signal applied to the RF INPUT, tune the signal to center screen while reducing the FREQ SPAN/DIV to 200 kHz. Change the Vertical Display to 2 dB/DIV, then active SAVE A.

c. Change the REF LEVEL to −10 dBm. Activate VIEW B. Display B should be 2 dB below display A.

d. Activate B–SAVE A. Check that B–SAVE A display is the algebraic difference between display B and display A (see Fig. 3-17).

e. Deactivate SAVE A and B–SAVE A.

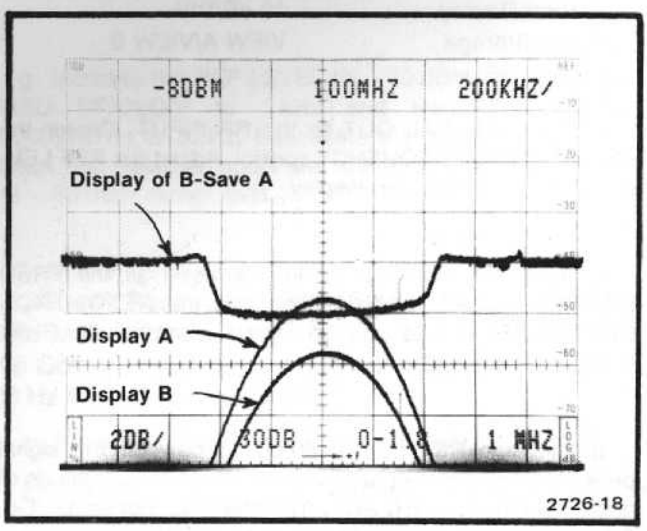


Fig. 3-17. Multiple exposure to illustrate how the differential between two signals can be measured.

25. Check Triggering Operation and Sensitivity (internal trigger sensitivity ≥2 divisions, external trigger ≥1.0 V, 15 Hz to 1 MHz)

a. Apply the output of a signal generator, modulated by a sine-wave generator, to the RF INPUT of the 496/496P. Monitor the output of the sine-wave generator with a test oscilloscope (see Fig. 3-18).

b. Set the front-panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	10 kHz
REF LEVEL	−30 dBm
MIN RF ATTEN	0 dB
RESOLUTION BANDWIDTH	1 MHz
TIME/DIV	20 ms
Vertical Display	LIN
Video Filter	Off
Digital Storage	VIEW A/VIEW B

c. Set the signal generator for a −30 dBm, 100 MHz signal and tune the 496/496P FREQUENCY to center the signal on screen.

d. Decrease the output of the signal generator so the display is half screen, then modulate the signal with a 1 kHz sine wave.

e. Press ZERO SPAN.

f. Adjust the sine-wave generator output for a modulation amplitude of two divisions, then switch TRIGGERING to INT.

g. Check the internal trigger operation through the 15 Hz to 1 MHz frequency range.

NOTE

Because of deflection amplifier response, the display amplitude will decrease at the high frequency end.

The triggering signal can also be applied through a bnc-to-pin-jack cable, to pins 1 and 2 (see Fig. 3-25) of the rear-panel ACCESSORIES connector (pin 2 is Video in; pin 1 Ext Video select).

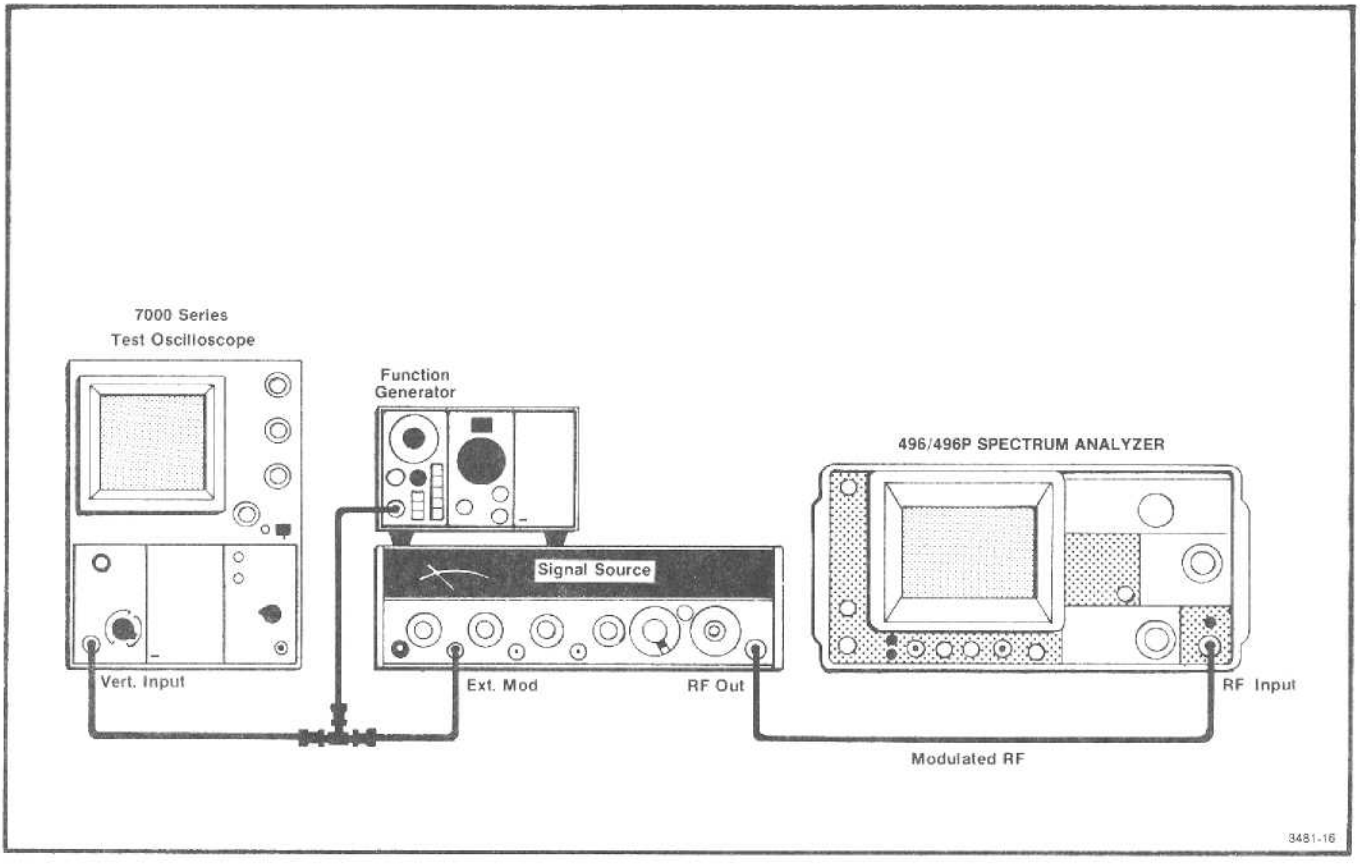


Fig. 3-18. Test equipment setup for checking triggering requirements.

h. Disconnect the test equipment. Apply, through a bnc T connector and coaxial cable, the sine-wave generator output to the EXT IN HORIZ/TRIG connector on the back panel of the 496/496P (see Fig. 3-19). Monitor the input signal amplitude with a test oscilloscope.

i. Set the sine-wave generator frequency to 1 kHz. Adjust its output level for 2 V peak-to-peak (1.0 V peak) as indicated on the test oscilloscope (see Fig. 3-20).

j. Change the 496/496P TIME/DIV to .2 s. Activate the EXT Triggering.

k. Check that sweep runs as the generator frequency is varied from 15 Hz to 1 MHz.

l. Return the TRIGGERING to FREE RUN and the input signal level to 0 V.

26. Check Vertical Output (provides 0.5 V ±5% of signal per division of display above and below the centerline)

a. Connect the VERT OUTPUT to the input of a dc-coupled test oscilloscope with a sensitivity of 1 V/DIV and sweep rate of 10 ms.

b. Set the 496/496P controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	100 kHz
REF LEVEL	−20 dBm
MIN RF ATTEN	0 dB
RESOLUTION BANDWIDTH	100 kHz
TIME/DIV	AUTO
Vertical Display	2 dB/DIV
Video Filter	Off
Digital Storage	Off

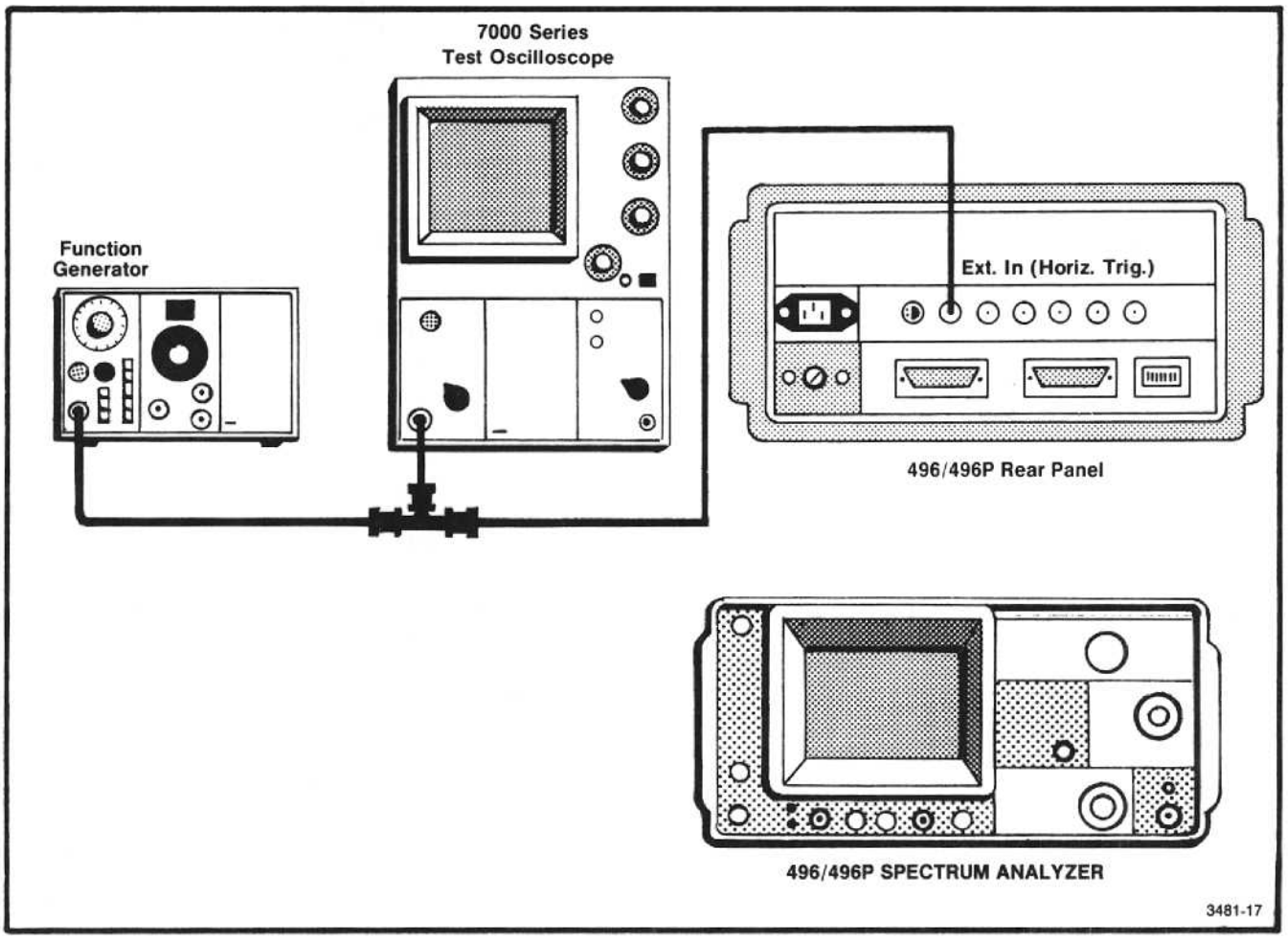
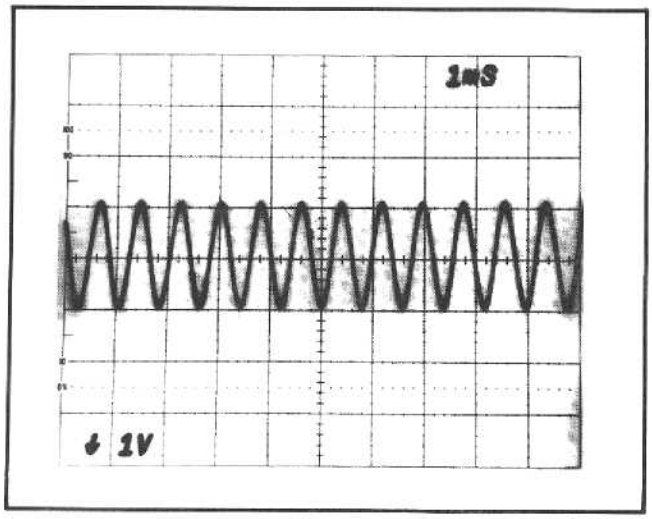


Fig. 3-19. Test equipment setup to check external triggering and horizontal input characteristics.



3783-21

Fig. 3-20. Test oscilloscope display of a sinewave input signal to EXT TRIG connector (input 0.5 V peak at 1.0 V peak to peak).

c. Apply the CAL OUT signal to the RF INPUT and tune the 100 MHz signal to center screen.

d. Activate the FINE step REF LEVEL function and adjust the REF LEVEL for an eight division display.

e. Check the vertical signal output level on the test oscilloscope. Output level should equal plus and minus 2 V for a total of 4 V ± 0.2 V (see Fig. 3-21).

27. Check Horizontal Signal Output (0.5 V, ±5% either side of center screen with a full range of −2.5 V to + 2.5 V, ±10%)

a. Connect a dc-coupled test oscilloscope to the HORIZ OUTPUT connector. Set the 496/496P TIME/DIV to MNL position.

b. Adjust the crt beam five divisions either side of center screen with the MANUAL SCAN control. The output range should equal −2.5 V to +2.5 V, ±10%.

c. Return the TIME/DIV to AUTO; disconnect and remove the test equipment.

28. Check LO Emission Out of the RF INPUT (no more than −70 dBm to 18 GHz, referenced to input mixer)

Two methods or procedures can be used to check EMI.

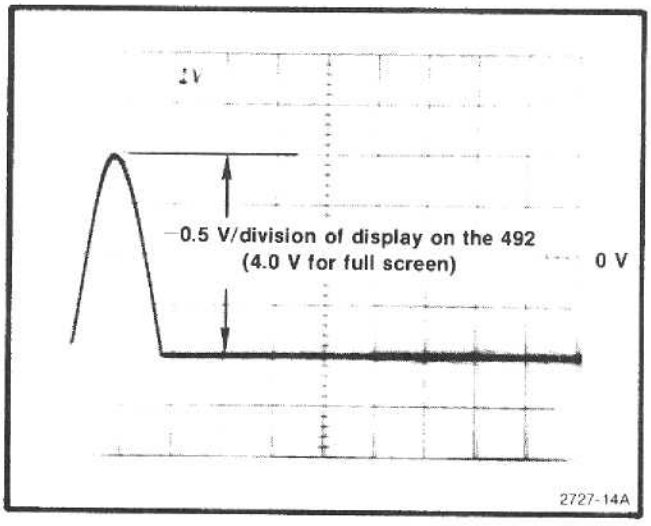
1. Connect a sensitive power meter (see equipment list) to the RF INPUT and directly measure the emitted signal level. Set MIN RF ATTEN at 0 dB and REF LEVEL at −20 dBm.

2. Use a high-frequency spectrum analyzer with loop coupling probe to sniff or check around the front-panel output ports for EMI radiation.

29. 496P GPIB Verification Program

This verification program for TEKTRONIX 4050-Series Computer Terminal checks functional operation of the GPIB interface in a 496P Spectrum Analyzer. All interface lines are verified as well as all interface messages, except those for parallel poll. In addition, the instruments' interface is checked for operation on other primary addresses, as well as the talk-only and listen-only modes.

The program is written in TEKTRONIX 4050 BASIC, and is divided into individual tests, each for a specific interface line, message, or function. The tests start on even 1000 line numbers to allow easy modification of the program.



2727-14A

Fig. 3-21. Display of a full screen signal at the Vertical Output Connector.

The following describes the function of each test in the program.

Lines 1—5000:	Interfaces to user definable keys for recovery from a failed test.
Lines 5000—6000:	Inputs the primary address of the 496P under test (1 should be used).
Lines 6000—7000:	ID query response test. The instrument must be able to talk and listen, to send out its ID? response and manipulate all eight of the DIO lines for the test to be successful.
Lines 7000—8000:	Local lock-out test. Tests correct operation of the interface message that should disable all programmable front panel controls.
Lines 8000—9000:	Go to LOCAL test. Tests correct operation of the interface message that should enable all front panel controls.
Lines 9000—10000:	Group Execute Trigger test. Checks that a GET message does cause the 496P to abort the present sweep and re-arm the trigger, causing a sweep to start and end, sending out an End-of-Sweep SRQ. Thus, the SRQ line, as well as the GET message, is verified.
Lines 10000—11000:	Selected Device Clear Test. This test verifies that an SDC message does indeed reset the 496P's GPIB output buffer clearing out it's ID? response.
Lines 11000—12000:	Device clear test. This test is identical to the selected device clear test, except the universal command DCL is used instead.
Lines 12000—13000:	Addressed as listener, talker test. This test checks to see that the 496P microprocessor correctly recognized that the GPIA chip has been addressed to listen or talk, and sends the appropriate character to the crt readout (L or T).
Lines 13000—14000:	Serial Poll test. This checks correct operation of the serial poll enable (SPE) and serial poll disable (SPD) interface messages. The status byte is read, and if anything other than ordinary operation is indicated, the instrument fails the test.
Lines 14000—15000:	GPIB rear panel switch test. All five primary address switches are checked for correct operation. Three subroutines are called in the process of testing one address switch. The first two send a formatted messge to the 4050 display, and the third performs the address switch test.
Lines 15000—16000:	Line feed or EOI switch test. Checks for correct selection of line feed as a termination when selected by this switch by sending an ID? terminated only by a line feed.
Lines 16000—17000:	Talk-only mode test. When selected, this mode should cause the instrument to send a SET? response and (optionally) a CURVE? response whenever the RESET-TO-LOCAL button is pressed. The string received from the instrument is thus examined for existence of a portion of the correct SET? response after the RESET-TO-LOCAL button is pressed.
Lines 17000—18000:	Listen-only mode test. When selected, this mode will cause the instrument to respond to any message on the bus, since it is always addressed to listen. The command "REF 0" is sent to the bus without addressing the instrument, then the listen-only mode is deselected and the instrument interrogated to see if it did respond to the REF command while in the listen-only mode.
Lines 18000—19000:	Interface clean (and Remote Enable) test. This IFC line on the GPIB will unaddress the instrument's interface. This fact is verified by noting that the "L" is not present in the crt readout, indicating that the IFC line worked; also the REN line will be unasserted when the end statement is executed (except for some early 4052 and 4054's). Thus, a front panel in the local mode is evidence that the REN line was successfully unasserted. (Evidence it was asserted is that the instrument was able to execute commands sent to it by previous tests.)
Lines 19000—end:	Utility routines. "Rear panel interface switch test text routine" puts headers on the interface switch test display. The "rear panel test text routine" tells the operator what to do after changing the address switches. "Test address switch" acquires an ID? response from the instrument on its new address during the address switch test. The "SRQ handler" will handle any 49X SRQ's that occur, although none, except the power-up SRQ, would be expected. (The end of sweep SRQ during the GET test is handled by another SRQ handler.) "Delay Generator" generates delays for other tests. The "Failure Decision Handler" allows the program to be restarted with the user definable keys if any test fails.

```
1 GO TO 5000
4 B2=1
5 RETURN
20 B2=5
21 RETURN
5000 REM *** 49XP GPIB VERIFICATION PROGRAM ***
5030 INIT
5040 ON SRQ THEN 19280
5050 DIM V$(400),W$(400)
5060 I7=0
5070 PAGE
5080 PRINT "JJJENTER 49XP'S PRIMARY ADDRESS (DEFAULT = 1) ";
5090 INPUT T$
5100 IF T$<>"" THEN 5130
5110 A1=1
5120 GO TO 5180
5130 A1=VAL(T$)
5140 IF A1>0 AND A1<31 THEN 5180
5150 PRINT "JJGERROR!! ";A1;" IS NOT A VALID ADDRESS";
5160 PRINT " ONLY 0 THRU 30 ARE VALID ADDRESSESKK"
5170 GO TO 5080
5180 PAGE
5190 REM
5200 REM
5210 REM
5220 REM
5230 REM
6000 REM ***"ID" QUERY RESPONSE ***
6010 PRINT "*** "ID" QUERY RESPONSE ***"
6020 PRINT @A1:"INI;ID?;SIG"
6030 INPUT @A1:T$
6040 V$=SEG(T$,1,9)
6050 IF V$="ID TEK/49" THEN 6080
6060 PRINT "JJJ*** "ID" QUERY RESPONSE *** FAIL ***G"
6070 GO TO 19530
6080 WBYTE @32+A1:64,128,-127
6090 PRINT @A1:"WFM ENC:BIN;CUR?"
6100 PRINT @37,0:37,255,255
6110 INPUT %A1:T$
6120 WBYTE @64+A1:
6130 RBYTE R,R,R,T6
6140 WBYTE @95:
6150 IF R=>128 AND T6<128 THEN 7000
6160 PRINT "JJJ*** DIO8 TEST *** FAIL ***G"
6170 GO TO 19530
6180 REM
6190 REM
6200 REM
6210 REM
6220 REM
7000 REM *** LOCAL LOCK-OUT.....LLO ***
7010 PRINT "*** LOCAL LOCK-OUT.....LLO ***"
7020 WBYTE @32+A1,17:
7030 PRINT @A1:"SET?"
7040 INPUT @A1:V$
7050 PRINT "II49XP IN LOCAL LOCK-OUT MODE (LLO)"
7060 PRINT "IIATTEMPT TO USE 49XP CONTROLS"
7070 PRINT " IIPRESS RETURN <CR> WHEN DONE ";
7080 INPUT T$
7090 PRINT @A1:"SET?"
```

```
7100 INPUT @A1:W$
7110 IF W$<>V$ THEN 7130
7120 GO TO 8000
7130 PRINT "J*** LOCAL LOCK-OUT.....LLO *** FAIL ***G"
7140 GO TO 19530
7150 REM
7160 REM
7170 REM
7180 REM
7190 REM
8000 REM *** GO TO LOCAL.....GTL ***
8010 PRINT @A1:"INI;TIM?"
8020 INPUT @A1:R
8030 PRINT @A1:"TIM INC"
8040 PRINT "*** GO TO LOCAL.....GTL ***"
8050 WBYTE @32+A1,1:
8060 PRINT @A1:"TIM?"
8070 INPUT @A1:T6
8080 IF R<>T6 THEN 8100
8090 GO TO 9000
8100 PRINT "J**** GO TO LOCAL.....GTL *** FAIL ***G"
8110 GO TO 19530
8120 REM
8130 REM
8140 REM
8150 REM
8160 REM
9000 REM *** GROUP EXECUTE TRIGGER.....GET ***
9010 PRINT "*** GROUP EXECUTE TRIGGER...GET ***"
9020 ON SRQ THEN 9120
9030 I7=0
9040 PRINT @A1:"INIT;TIM 100M;SIG;EOS ON"
9050 WBYTE @32+A1,8:
9060 T6=3
9070 GOSUB 19390
9080 PRINT @A1:"EOS OFF"
9090 IF I7<>1 THEN 9150
9100 ON SRQ THEN 19280
9110 GO TO 10000
9120 WBYTE @20:
9130 I7=1
9140 RETURN
9150 PRINT "GROUP EXECUTE TRIGGER...GET *** FAIL ***G"
9160 GO TO 19530
9170 REM
9180 REM
9190 REM
9200 REM
9210 REM
10000 REM *** SELECTED DEVICE CLEAR...SDC ***
10010 PRINT "*** SELECTED DEVICE CLEAR...SDC ***"
10020 PRINT @A1:"ID?"
10030 WBYTE @32+A1,4:
10040 WBYTE @64+A1:
10050 RBYTE R
10060 IF ABS(R)<>255 THEN 10080
10070 GO TO 11000
10080 PRINT "*** SELECTED DEVICE CLEAR.....SDC *** FAIL ***G"
10090 GO TO 19530
10100 REM
```

```
10110 REM
10120 REM
10130 REM
10140 REM
11000 REM *** DEVICE CLEAR.....DCL ***
11010 PRINT "*** DEVICE CLEAR.....DCL ***"
11020 PRINT @A1:"ID?"
11030 WBYTE @20:
11040 WBYTE @64+A1:
11050 RBYTE R
11060 IF ABS(R)<>255 THEN 11080
11070 GO TO 12000
11080 PRINT "*** DEVICE CLEAR.....DCL *** FAIL ***G"
11090 GO TO 19530
11100 REM
11110 REM
11120 REM
11130 REM
11140 REM
12000 REM ** ADDRESSED AS LISTENER, TALKER ***
12010 PRINT "*** 49XP ADDRESSED AS LISTENER..***"
12020 WBYTE @32+A1:76,79,82,68,79,-63
12030 T6=1
12040 GOSUB 19390
12050 INPUT @A1:V$
12060 T$=SEG(V$,16,1)
12070 IF T$="L" THEN 12100
12080 PRINT "J*** 49XP ADDRESSED AS LISTENER *** FAIL ***G"
12090 GO TO 19530
12100 PRINT "*** 49XP ADDRESSED AS TALKER....***"
12110 PRINT @A1:"INI;TIM 50M;SIG;SIG;WAI;LORDO?"
12120 INPUT @A1:V$
12130 T$=SEG(V$,16,1)
12140 IF T$="T" THEN 13000
12150 PRINT "*** 49XP ADDRESSED AS TALKER *** FAIL ***"
12160 GO TO 19530
12170 REM
12180 REM
12190 REM
12200 REM
12210 REM
13000 REM *** SERIAL POLL ***
13010 PRINT "*** SERIAL POLL.....SPD/SPE ***"
13020 WBYTE @95,63,24,64+A1:
13030 RBYTE R
13040 WBYTE @95,25:
13050 IF R=0 OR R=16 THEN 13080
13060 PRINT "J*** SERIAL POLL *** FAIL ***G"
13070 GO TO 19530
13080 T6=3
13090 GOSUB 19390
13100 REM
13110 REM
13120 REM
13130 REM
13140 REM
14000 REM *** GPIB INTERFACE REAR PANEL SWITCH TEST ***
14010 PAGE
14020 A1=2
14030 GOSUB 19000
```

@

```
14040 PRINT " 0 I 0 I 0 I 0 0 0 1 0"
14050 GOSUB 19070
14060 GOSUB 19190
14070 PAGE
14080 A1=4
14090 GOSUB 19000
14100 PRINT " 0 I 0 I 0 I 0 0 1 0 0"
14110 GOSUB 19070
14120 GOSUB 19190
14130 PAGE
14140 A1=8
14150 GOSUB 19000
14160 PRINT " 0 I 0 I 0 I 0 1 0 0 0"
14170 GOSUB 19070
14180 GOSUB 19190
14190 PAGE
14200 A1=16
14210 GOSUB 19000
14220 PRINT " 0 I 0 I 0 I 1 0 0 0 0"
14230 GOSUB 19070
14240 GOSUB 19190
14250 REM
14260 REM
14270 REM
14280 REM
14290 REM
15000 REM *** "LF" OR "EOI" SWITCH ***
15010 PAGE
15020 A1=1
15030 GOSUB 19000
15040 PRINT " 0 I 0 I 1 I 0 0 0 0 1"
15050 GOSUB 19070
15060 PRINT "JJTESTING "LF" OR "EOI" SWITCH"
15070 GOSUB 19190
15080 WBYTE @32+A1:73,68,63,10
15090 INPUT @A1:T$
15100 T$=SEG(T$,1,9)
15110 IF T$="ID TEK/49" THEN 15140
15120 PRINT "J"LF" OR "EOI" SWITCH *** FAIL ***G"
15130 GO TO 19530
15140 T6=2
15150 GOSUB 19390
15160 REM
15170 REM
15180 REM
15190 REM
15200 REM
16000 REM *** TALK ONLY MODE ***
16010 PAGE
16020 GOSUB 19000
16030 PRINT " 0 I 1 I 0 I 0 0 0 0 1"
16040 GOSUB 19070
16050 PRINT "JJJTESTING TALK ONLY"
16060 INPUT @A1:V$
16070 I7=POS(V$,"FINE OFF",1)
16080 IF I7<>0 THEN 17000
16090 PRINT "JJJTALK ONLY MODE *** FAIL ***G"
16100 GO TO 19530
16110 REM
16120 REM
```

```
16130 REM
16140 REM
16150 REM
17000 REM *** LISTEN ONLY MODE ***
17010 PAGE
17020 GOSUB 19000
17030 PRINT " 1 I 0 I 0 I 0 0 0 0 1"
17040 GOSUB 19070
17050 PRINT "JJJTESTING LISTEN ONLY"
17060 PRINT @A1:"INI"
17070 T6=0.5
17080 GOSUB 19390
17090 WBYTE 82,69,70,32,-48
17100 PAGE
17110 GOSUB 19000
17120 PRINT " 0 I 0 I 0 I 0 0 0 0 1"
17130 GOSUB 19070
17140 PRINT @A1:"REF?"
17150 INPUT @A1:V$
17160 IF V$<>"REFLVL +0.0" THEN 17180
17170 GO TO 18000
17180 PRINT "JJJLISTEN ONLY MODE *** FAIL ***G"
17190 GO TO 19530
17200 REM
17210 REM
17220 REM
17230 REM
17240 REM
18000 REM *** INTERFACE CLEAR AND REMOTE ENABLE TEST.....IFC & REN ***
18010 PAGE
18020 PRINT "JJJTESTING IFC(INTERFACE CLEAR), AND REN(REMOTE ENABLE)"
18030 WBYTE @32+A1:
18040 T6=3
18050 GOSUB 19390
18060 PRINT "JJCHECK THE 49XP CRT, FOR AN "L" BETWEEN THE VERTICAL"
18070 PRINT "DISPLAY AND THE MIN RF ATTEN READOUTS."
18080 PRINT "JPRESS RETURN TO CONTINUE.";
18090 INPUT P$
18100 INIT
18110 PRINT "JIF AN "L" IS STILL PRESENT, THE IFC LINE IS FAULTY,"
18120 PRINT "IF THE "L" VANISHED, IFC TESTED OK."
18130.PRINT "JJCHECK ALSO THE 49XP FRONT PANEL FOR PROPER LOCAL CONTROL"
18140 PRI "IF THE FRONT PANEL IS LOCKED OUT, THE REN LINE IS FAULTY, IF"
18150 PRINT "NOT, REN TESTED OK"
18160 PRINT "JJJGPIB VERIFICATION COMPLETEG"
18170 END
18180 REM
18190 REM
18200 REM
19000 REM *** REAR PANEL INTERFACE SWITCH TEST TEXT ROUTINE ***
19010 PRINT "SET GPIB ADDRESS SWITCHES TO:"
19020 PRINT "JJLISTENITALKILF ORI ADDRESS"
19030 PRINT " ONLYIONLYIEOII16 8 4 2 1"
19040 PRINT "------I----I-----I----------"
19050 RETURN
19060 REM
19070 REM *** REAR PANEL TEST TEXT ROUTINE ***
19080 PRINT "JJAFTER CHANGING THE SWITCHES, ";
19090 PRINT "PRESS THE REMOTE/LOCAL BUTTON ONCEJJ"
19100 PRINT "I(NOTE: IF YOU GET A GPIB INTERFACE ERROR MESSAGE,"
```

```
19110 PRINT "I          IT MEANS THAT THE SWITCH(ES) WEREN'T "
19120 PRINT "I          READ CORRECTLY. TO RE-TEST, TYPE"
19130 PRINT "I          "RUN" FOLLOWED BY THE LINE NUMBER IN THE"
19140 PRINT "I          ERROR MESSAGE) "
19150 PRINT "JJIPRESS RETURN <CR> WHEN DONE ";
19160 INPUT T$
19170 RETURN
19180 REM
19190 REM *** TEST ADDRESS SWITCH ***
19200 PRINT @A1:"ID?"
19210 INPUT @A1:T$
19220 T$=SEG(T$,1,9)
19230 IF T$="ID TEK/49" THEN 19260
19240 PRINT "ADDRESS SWITCH TEST FAIL"
19250 GO TO 19530
19260 RETURN
19270 REM
19280 REM *** SRQ HANDLER ***
19290 T6=3
19300 GOSUB 19390
19310 POLL Z1,Z1;A1
19320 PRINT @A1:"ERR?"
19330 INPUT @A1:S$
19340 PRINT "GGAN INTERRUPT OCCURED ON THE BUS, THE 49XP RETURNS ";S$
19350 PRINT "JPRESS RETURN <CR> TO CONTINUE ";
19360 INPUT T$
19370 RETURN
19380 REM
19390 REM *** DELAY GENERATOR ***
19410 REM *** T6 GIVEN IN SEC (GLOBAL) *** I9 SCRATCH ***
19420 IF T6<0 THEN 19510
19430 IF RND(0)>0.5 THEN 19490
19440 REM *** 4051 ***
19450 T6=T6*220
19460 FOR I9=1 TO T6
19470 NEXT I9
19480 GO TO 19510
19490 REM *** 4052
19500 CALL "WAIT",T6
19510 T6=0
19520 RETURN
19530 REM **** FAILURE DECISION HANDLER ****
19540 PRINT "JJISELECT A UDK:"
19550 PRINT "I (1) RE-START"
19560 PRINT "I (5) END"
19570 SET KEY
19580 B2=0
19590 IF B2<>1 AND B2<>5 THEN 19590
19600 IF B2=5 THEN 19630
19610 PAGE
19620 GO TO 6000
19630 END
```

This concludes the Performance Check part of the Calibration Procedure.

ADJUSTMENT PROCEDURE

If the 496/496P operation is out of tolerance for a particular specification, determine the cause, repair if necessary, then use the appropriate adjustment procedure to return the instrument operation to specification. After any adjustment, repeat that part of the Performance Check to verify operation.

Allow instrument to warm up for at least two hours in ambient air of +20°C to +30°C before performing an adjustment.

Waveform illustrations used in these instructions may be idealized. They are not intended to be representative of specification tolerances.

Adjustment steps that interact are noted, and reference is made within the procedure to the affected circuit or steps.

CAUTION

STATIC DISCHARGE CAN DAMAGE MANY SEMICONDUCTOR COMPONENTS USED IN THIS INSTRUMENT.

Many semiconductor components, especially MOS types, can be damaged by static discharge. Damage may not be catastrophic, therefore, not immediately apparent. It usually appears as a 'weakening' of the semiconductor characteristics. Devices that are particularly susceptible are: MOS, CMOS, JFETs, and high impedance operational amplifiers. Damage can be significantly reduced by observing the following precautions.

1. Handle static-sensitive components or circuit assemblies at or on a static-free surface. Work station areas should contain a static-free bench cover or work plane such as conductive polyethylene sheeting and a grounding wrist strap. The work plane should be connected to earth ground.

2. All test equipment, accessories, and soldering tools should be connected to earth ground.

3. Minimize handling by keeping the components in their original containers until ready for use. Minimize the removal and installation of semiconductors from their circuit boards.

4. Hold the IC devices by their body rather than the terminals.

5. Use containers made of conductive material or filled with conductive material for storage and transportation. Avoid using ordinary plastic containers. Any static sensitive part or assembly (circuit board) that is to be returned to Tektronix, Inc., should be packaged in its original container or one with anti-static packaging material.

Table 3-5
ADJUSTMENT STEPS FOR CALIBRATING THE 496/496P

Preparation

To prepare the rackmount or benchtop version for adjustment, refer to the Rackmount/Benchtop Versions section of this manual (Section 6).

Remove the cabinet of the 496/496P as follows:

1) set the 496/496P on its face or front panel;

2) loosen the four screws through the back rubber feet;

3) pull the cover up and off of the 496/496P;

4) place the instrument on the bench and reconnect the power cord.

1. Check and Adjust Low Voltage Power Supply

This high efficiency power supply uses an internal oscillator. The frequency of the oscillator is adjusted for 66 kHz. This adjustment is normally required only after replacing oscillator components; therefore, Part 1 of this step should only be performed after repair. Part 2 is the normal adjustment and check procedure.

WARNING

The 496/496P uses a high efficiency power supply. The potential of the primary ground for this supply is different than chassis or earth ground. An isolation transformer, with a turns ratio of 1:1 and a 500 VA minimum rating, should be used between the power source and the 496/496P power input receptacle. The transformer must have a three-wire input and output connector with ground through the input and output. Stancor GIS1000 is a suitable transformer. A jumper should also be connected between the primary ground side to chassis ground (emitter of Q2061 and the ground terminal of the input filter FL301).

If the power supply is separated from the instrument and operated on the bench, hazardous potentials will exist within the supply for several seconds after power is disconnected. This is due to the slow discharge of capacitors C6101 and C6111. A relaxation oscillator lights DS 5112 (next to C6111) when the potential exceeds 80 volts.

Part 1
Adjusting the Power Supply Oscillator Frequency

a. Remove the Power Supply module as described in the Maintenance section. Remove the Power Supply module cover and disconnect P3045.

b. Apply power to the module by plugging the power cord into the power input plug and connect it to a suitable power source (115 V ac or 230 V ac, depending on the position of P1091 on J1091).

c. Use a plastic or insulated tuning tool or equivalent, to insert between the two power switches to engage these switches.

d. Connect a test oscilloscope probe with a deflection sensitivity of 5 V/div and sweep rate of 10 μs/div to TP6053 (Fig. 3-22). Note the output waveform of the oscillator U6059. Amplitude should be approximately 10 V.

e. Adjust R6061 (Oscillator Freq Adj) for a waveform period of 15 μs (66 kHz).

f. Reinstall the power supply module cover, then install the module on the 496/496P.

Part 2
Check and Adjust Low Voltages

a. Connect a Variac (line voltage regulator) in line with the 496/496P power input and set the Variac for 117 Vac.

b. Connect a digital voltmeter (DVM) to +15 V test point (Fig. 3-22B) on the Z-Axis board to monitor the +15 V supply.

c. Remove the power supply cover screw located below the 10 MHz IF OUTPUT jack on the rear panel (see Fig. 3-22A). This will provide access to the +15 V adjustment, R6028.

d. Insert a narrow bit screwdriver through the screw hole and engage adjustment R6028. Adjust for +15 V on the DVM.

e. Vary the input voltage range from 90 to 132 Vac and note that the +15 V supply remains regulated.

f. Check the other supply voltages at test points indicated in Fig. 3-22B against tolerances listed in Table 3-6.

Table 3-6
POWER SUPPLY VOLTAGE TOLERANCES

Supply	Tolerance
+9 V	+9 V to +10 V
−5 V	−4.95 V to −5.05 V
−15 V	−14.90 V to 15.05 V
+5 V	+4.85 V to +5.10 V
+17 V	+16.8 V to +18.6 V
+100 V	+95 V to +105 V
+300 V	+280 V to +310 V

g. Remove the line voltage regulator (Variac) and reconnect the 496/496P directly to the power source.

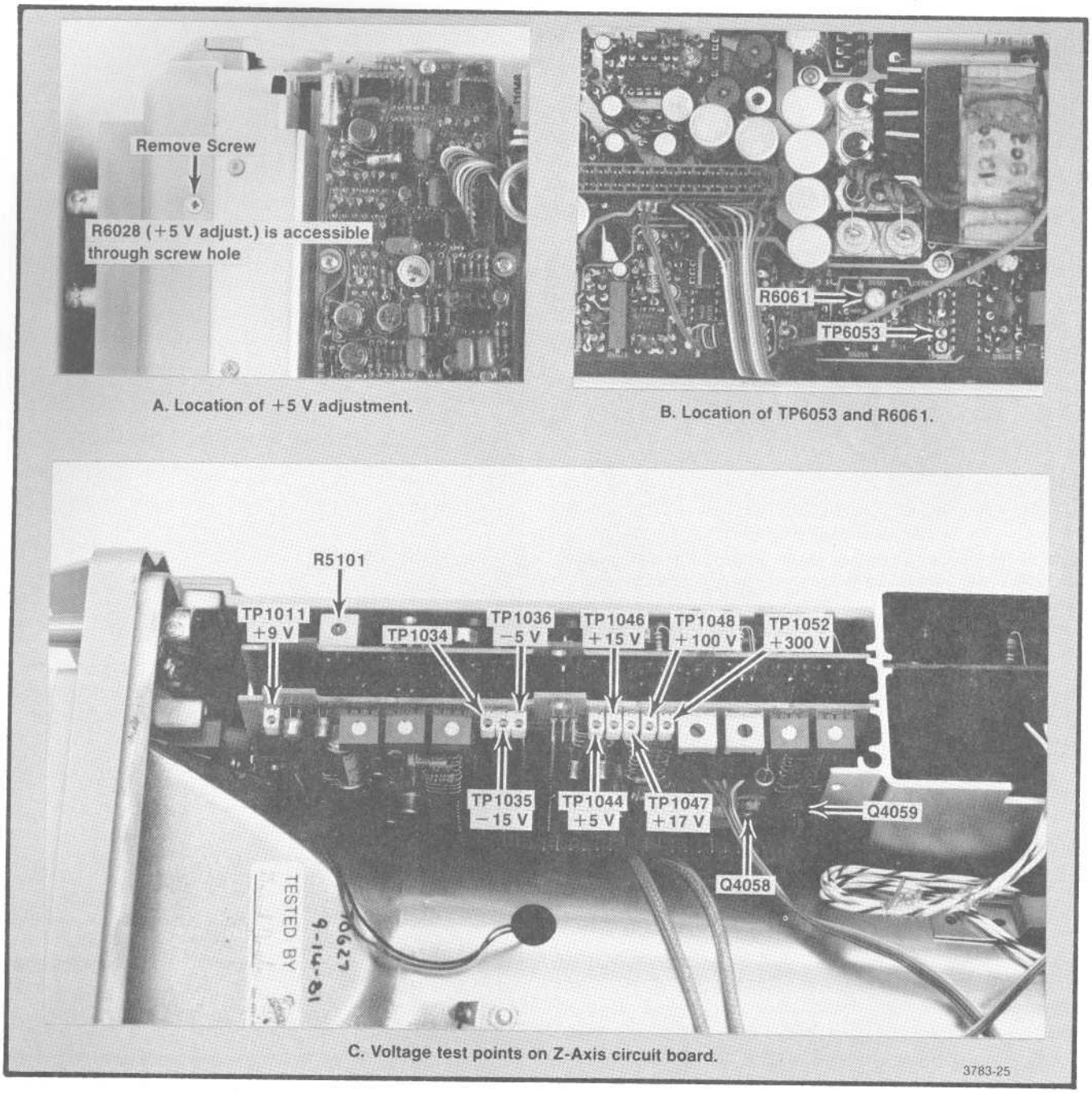


Fig. 3-22. Low voltage power supply adjustments and test point locations.

2. CRT DISPLAY (Z-Axis and High Voltage Circuits)

NOTE

Instruments prior to serial number B010218 do not have Crt Bias adjustment R2040. If your instrument does not have R2040, proceed to part b of this step. Auto Focus Tracking R1067 and Auto Focus Gain R1063 no longer affect the display. They are set mid range and not described in this procedure.

a. Switch POWER off and preset the INTENSITY control fully counterclockwise, MANUAL SCAN to midrange, and TIME/DIV to MNL. Set the Intensity Limit R1027 on the Z-Axis board (Fig. 3-23) fully counterclockwise and Crt Bias R2040 on the High Voltage board (Fig. 3-24) fully clockwise.

b. Switch POWER on and after the power-up state has stabilized change the Vertical Display mode to 2 dB/DIV, deactivate READOUT, and if the instrument has Option 02 turn Digital Storage off.

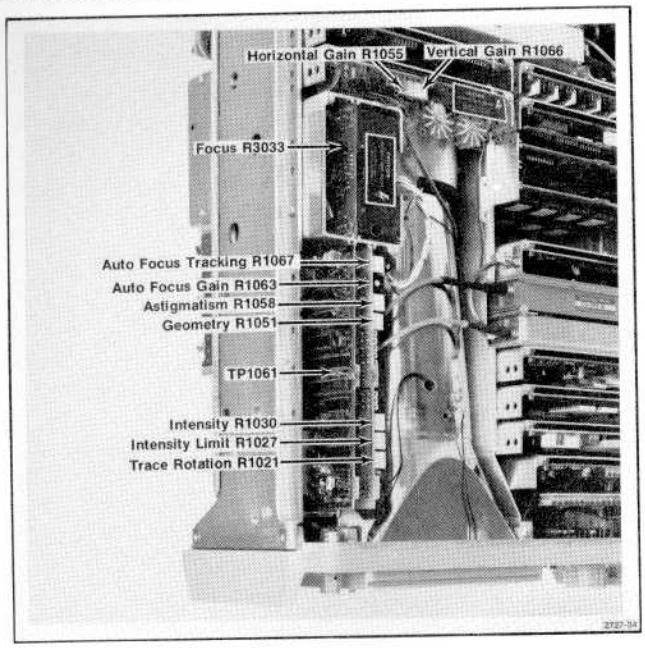


Fig. 3-23. Adjustments and test points on the deflection amplifier, High Voltage module, and Z Axis/RF Interface board.

c. Adjust Crt Bias as follows:

1) Using a voltmeter on the 20 volt range, measure and record the collector voltage of Q4058 or Q4059 (Fig. 3-22) on the Z-Axis board.

2) Turn INTENSITY clockwise until a crt beam dot appears on the screen.

3) Focus the dot by adjusting R3033 on the High Voltage board (Fig. 3-23).

4) Set the INTENSITY control for a collector voltage which is about 5.5 volts higher than the voltage noted in part 1.

5) Use the non-metallic screwdriver to adjust Crt Bias R2040 counterclockwise until the crt beam is visible, then turn the adjustment clockwise until the dot just extinguishes, with the screen shaded. (If no dot appears with the adjustment fully counterclockwise, this will be the bias setting.)

6) Turn the INTENSITY control clockwise until a dot is visible. Defocus the dot with the focus adjustment, then adjust Astigmatism R1058 (Fig. 3-23) for a round dot. Re-focus the crt beam dot.

7) Turn the INTENSITY control counterclockwise until the dot just disappears and again measure the collector voltage of Q4058 or Q4059. Voltage should equal or exceed the voltage measured in part 4. If the voltage is less, repeat the procedure for setting Crt Bias.

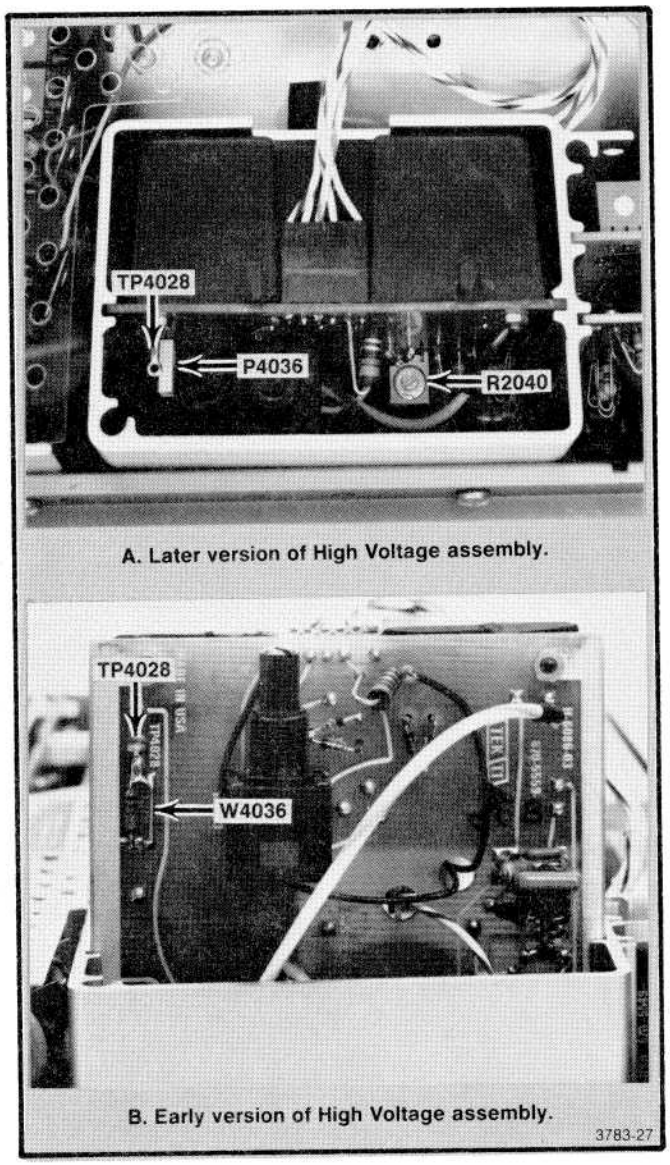


Fig. 3-24. Location of wire strap (W4036) on high voltage circuit board.

d. Adjust the crt cathode current as follows:

1) Switch POWER off then remove P4036 (Fig. 3-24) on the High Voltage board. Turn the INTENSITY control fully clockwise, the MANUAL SCAN fully counterclockwise and ensure that the TIME/DIV is in MNL position. Set the Intensity Limit R1027 on the Z-Axis board (Fig. 3-23) fully clockwise.

2) Connect the voltmeter between TP4028 (Fig. 3-24) and the ground lug on the crt shield.

3) Turn POWER on. After the instrument initializes, activate the 2 dB/DIV display mode and switch READOUT and Digital Storage off.

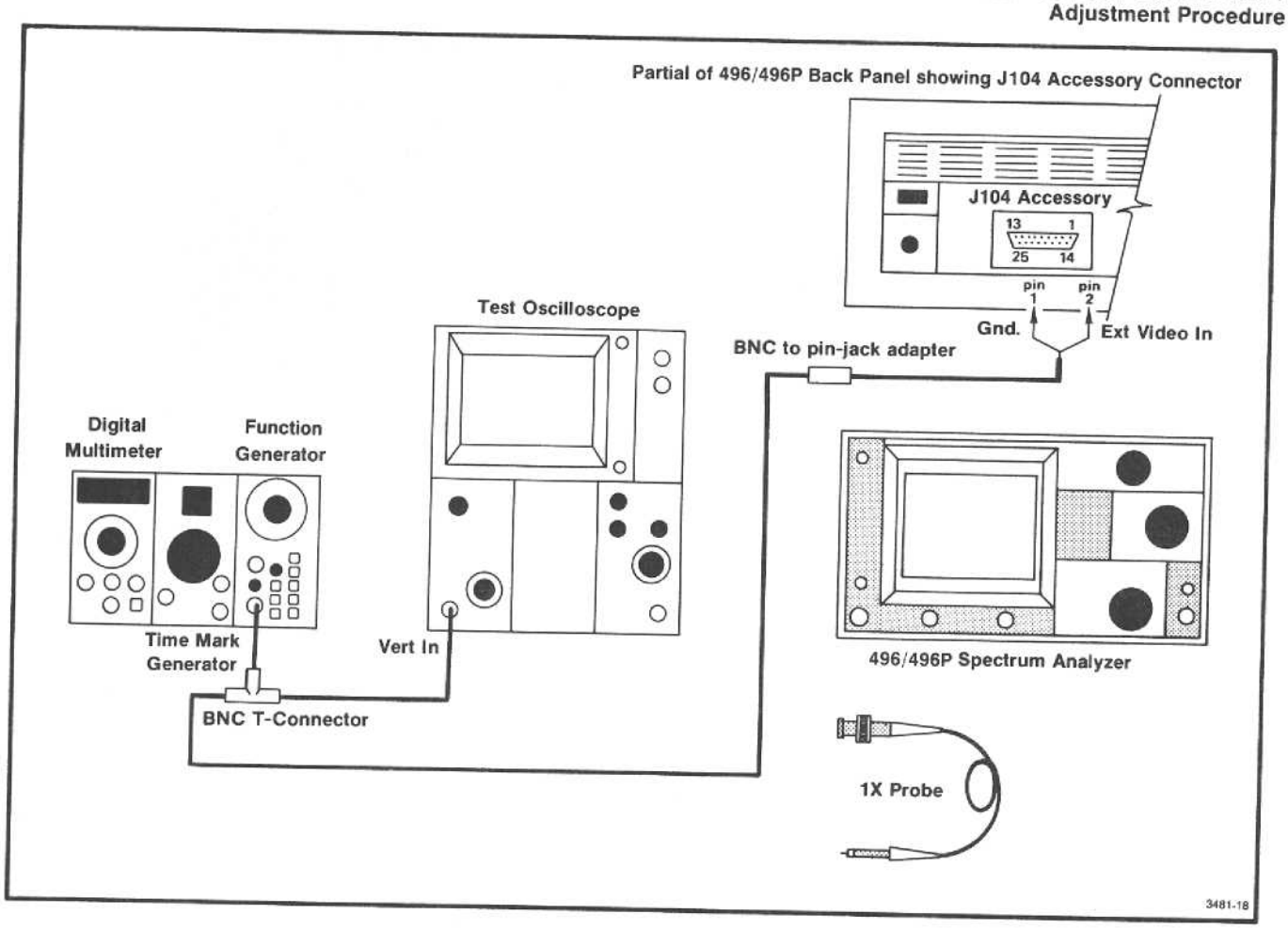


Fig. 3-25. Test equipment setup for calibrating the Deflection Amplifier.

4) Adjust Intensity Limit R1027 (Fig. 3-23) for a voltage reading of 0.9 volt at TP4028.

5) Switch POWER off and re-install the jumper P4036, on the High Voltage board. Turn POWER on.

e. Apply the CAL OUT signal to the RF INPUT and set the front panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	10 MHz
RESOLUTION BANDWIDTH	MAX
TIME/DIV	AUTO
REF LEVEL	−20 dBm
VIDEO FILTER	NARROW
MIN RF ATTEN dB	0
Vertical Display	10 dB
Digital Storage	off

f. Reduce the FREQ SPAN/DIV toward 0 Hz while keeping the calibrator signal centered on screen with the FREQUENCY control. Adjust the REF LEVEL so the trace is approximately mid-screen; then adjust the Trace Rotation R1021 (Fig. 3-23) so the trace is aligned with the graticule lines.

g. Change the REF LEVEL so the trace is approximately 15 to 20 dB below the top of the screen. Now, while alternately switching between 2 dB/DIV and 10 dB/DIV, adjust Geometry R1051 (Fig. 3-23) for the straightest trace at the top and bottom of the screen.

If the instrument has Digital Storage, turn the storage on and use the PEAK/AVERAGE cursor, positioned at the top and bottom of the screen, as a reference line to set geometry.

h. Change the REF LEVEL to position the trace within the graticule area with the Vertical Display mode in 2 dB/DIV. Activate Digital Storage if the instrument has Option 02.

i. Adjust INTENSITY so the trace is just visible.

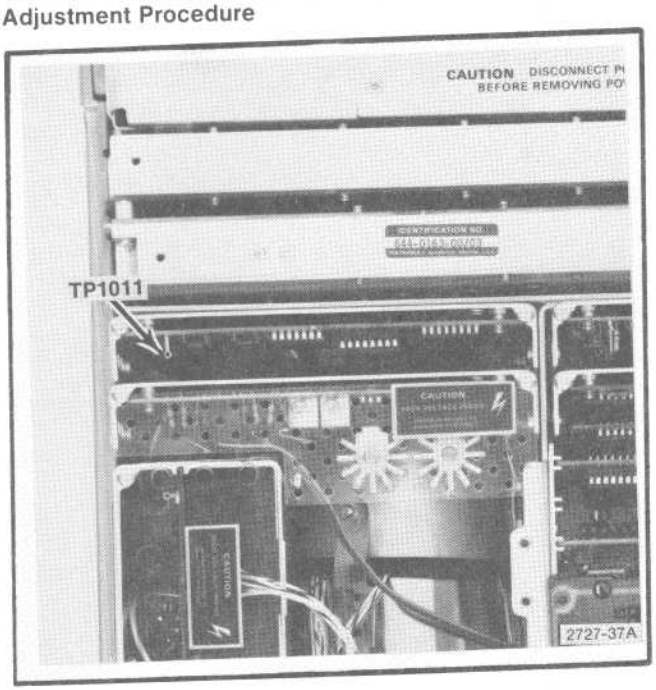


Fig. 3-26. Location of TP1011 on Crt Readout.

j. Adjust Δ Intensity R1030 (Fig. 3-23) so the brightness of the readout characters is the same (just discernible) as the trace.

k. Rotate the INTENSITY control and note that the brightness of the trace and readout characters tracks.

3. Deflection Amplifier (gain and frequency response)

a. Test equipment setup is shown in Fig. 3-25. Set the TIME/DIV to 5 ms, Vertical Display to 2 dB/DIV, and switch Digital Storage off. Position the trace on the bottom graticule line.

b. Apply a 5 kHz, 0 to +4 V signal, from the sine-wave generator, through a bnc-to-pin-jack adapter, to the Ext Video input (pin 2) and Video Select (pin 1) of the ACCESSORIES jack (see Fig. 3-25).

c. Adjust Vert Gain, R1066 (Fig. 3-23), for a full screen display (0 to +4 V). Remove the 5 kHz signal from pin 2 of the ACCESSORIES jack.

d. Set TIME/DIV to MNL, and Vertical Display to 2 dB/DIV.

e. Connect a digital voltmeter (DVM) to TP1061 (Fig. 3-23) and adjust MANUAL SCAN for 0.0 V at TP1061. Adjust horizontal Position control to center MANUAL SCAN dot.

f. Adjust MANUAL SCAN for a reading of +5 V at TP1061. Now adjust Horiz Gain, R1055 (Fig. 3-23), to position the crt beam to the right graticule edge (10th graticule line).

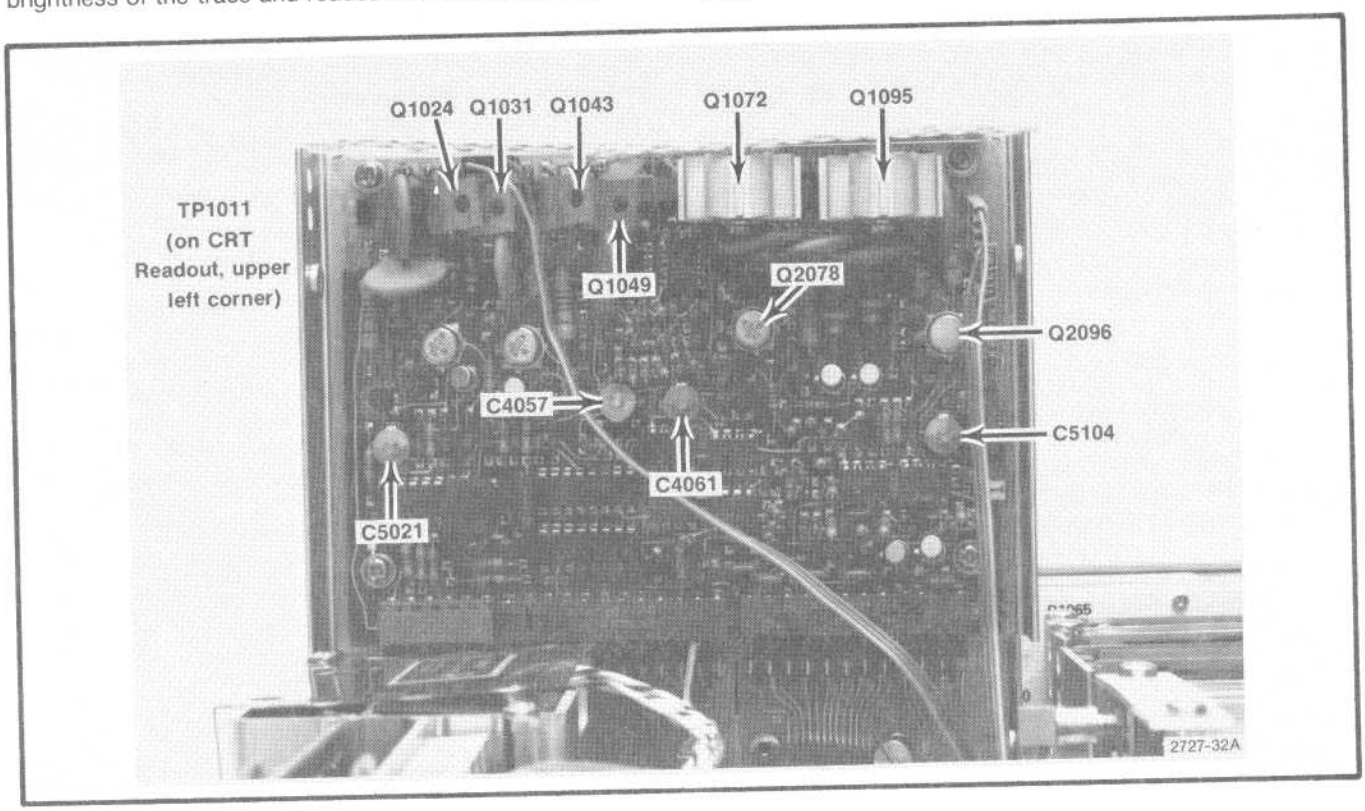


Fig. 3-27. Test points and adjustments on the Deflection Amplifier board for gain and frequency response calibration.

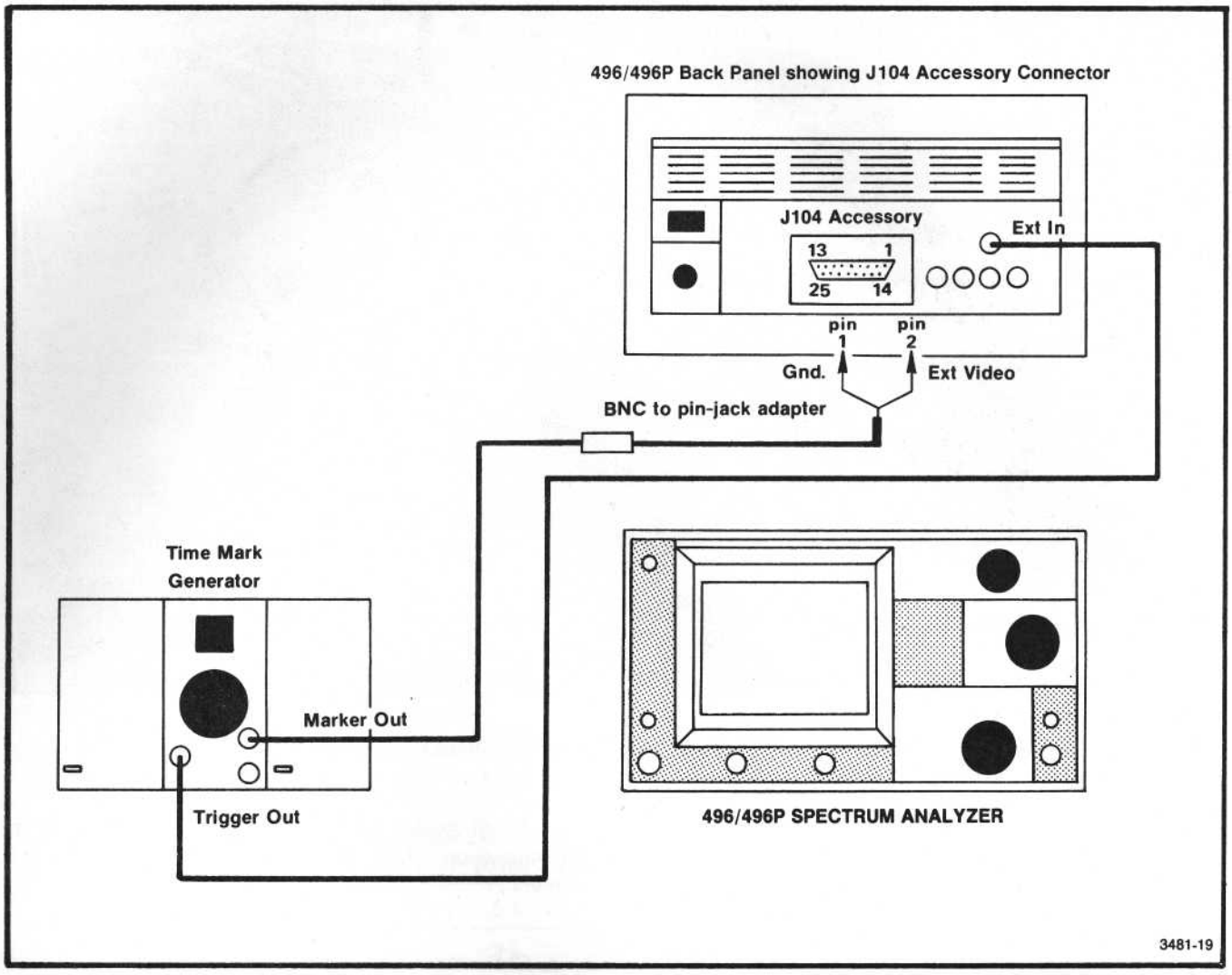


Fig. 3-28. Test equipment setup for calibrating sweep timing.

g. Adjust MANUAL SCAN so crt beam moves to the left edge of the graticule and check that the voltage at TP1061 is now approximately −5.0 V.

h. Turn the POWER off and disconnect the DVM. Remove and install the Deflection Amplifier board on an extender.

i. Change the test oscilloscope to Ext Trigger. Apply the Readout Off signal at TP1011 (Fig. 3-26), in the upper left corner of the crt readout board, to the test oscilloscope Ext Trigger input. Adjust the controls for a triggered sweep. Turn the 496/496P sweep off by activating SINGLE SWEEP, deactivate Digital Storage and ensure READOUT is on.

j. Connect the test oscilloscope probe to the collectors of Q1031 and Q1024. Adjust C5021 (Fig. 3-27) for the best frequency response (no overshoot or rolloff).

k. Connect the probe to the collectors of Q1043 and Q1049. Adjust C4057 (Fig. 3-27) for the best response.

l. Connect the probe to the collectors of Q1072, Q2078 (Fig. 3-27), and adjust C4061 for the best response.

m. Connect the probe to the collectors of Q1095, Q2096 (Fig. 3-27), and adjust C5104 for best response.

n. Remove the probe and Ext Trigger connection to TP1011.

o. Check the appearance of "Z" in GHz of the frequency readout. If necessary, adjust C5104 and C4061 (vertical output) for the straightest top on the Z.

p. Set the Vertical Display to LIN and adjust REF LEVEL for 100 μV/. Set TIME/DIV to MNL and adjust MANUAL SCAN fully clockwise.

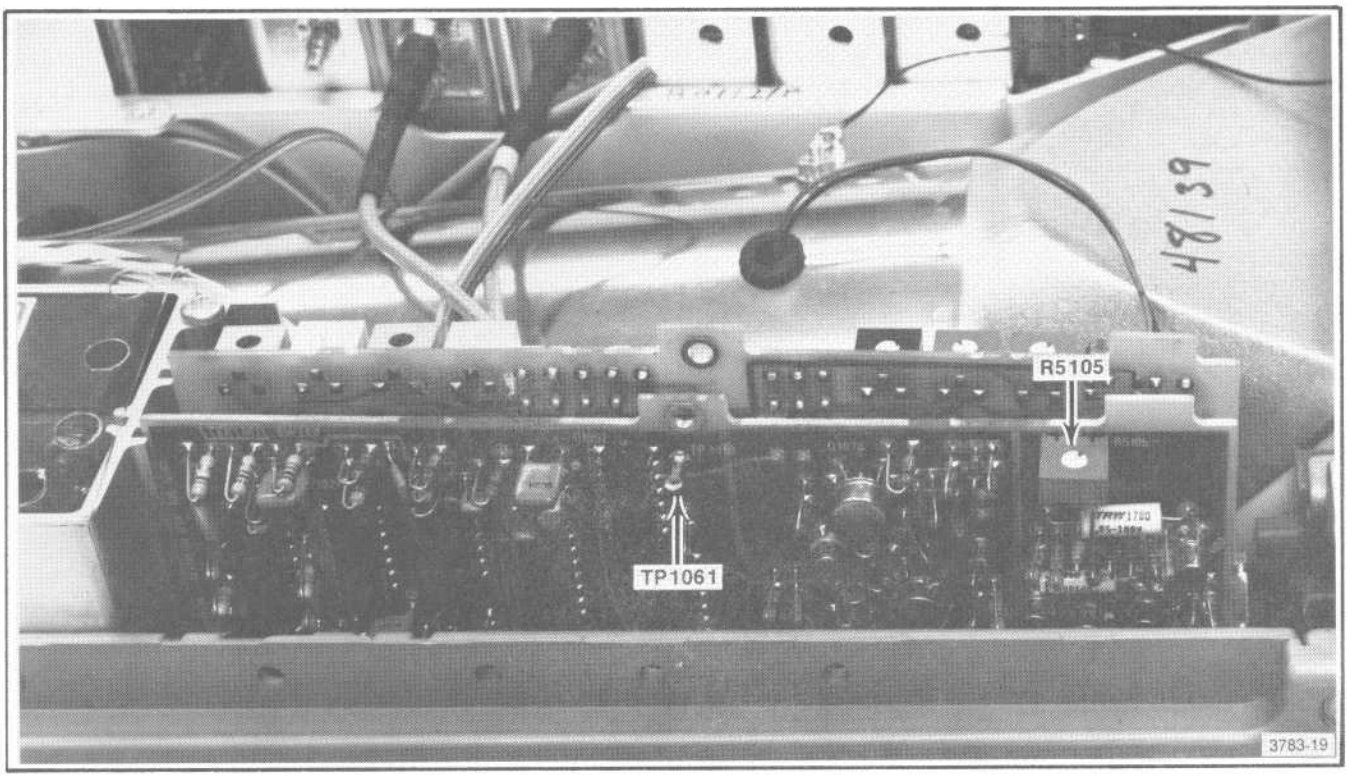


Fig. 3-29. Location of timing adjustment R5105 and TP1061 on sweep board.

q. Adjust C5021 and C4057 for best REF LEVEL readout (straightest letters and numerals).

4. Adjust Sweep Timing

a. Test equipment setup is shown in Fig. 3-28. Select EXT Triggering, TIME/DIV of 10 ms, and a FREQ SPAN/DIV of 10 MHz or less.

b. Apply 10 ms time marks from the time-mark generator to the EXT Video In (pins 2 and 1 of the ACCESSORIES jack, see Fig. 3-28) and the Trigger Output of the time-mark generator to the EXT TRIG input on the back panel of the 496/496P. This should provide a display of 10 ms markers.

c. Adjust Sweep Timing, R5105 (see Fig. 3-29), for 1 marker/division. (Use POSITION adjustments to align markers.)

d. Check the remaining TIME/DIV selections for ±5% or less error over the center eight divisions.

e. Set the TIME/DIV to AUTO, FREQ SPAN/DIV to MAX, and activate AUTO RESOLUTION.

f. Check the Time/Div versus Resolution Bandwidth as per Table 3-7 for the different FREQ SPAN/DIV settings.

g. Return Triggering to FREE RUN and remove the time-mark generator markers to the 496/496P. Reposition the trace if moved in part c.

Table 3-7

RESOLUTION AND SWEEP RATE AS A FUNCTION OF SPAN IN THE AUTO MODE

FREQ SPAN/DIV	RESOLUTION	TIME/DIV
MAX	1 MHz	20 ms
200 MHz	1 MHz	10 ms
100 MHz	1 MHz	10 ms
50 MHz	1 MHz	10 ms
20 MHz	1 MHz	10 ms
10 MHz	1 MHz	10 ms
5 MHz	100 kHz	10 ms
2 MHz	100 kHz	10 ms
1 MHz	100 kHz	10 ms
500 kHz	100 kHz	10 ms
200 kHz	10 kHz	10 ms
100 kHz	10 kHz	10 ms
50 kHz	10 kHz	10 ms
20 kHz	10 kHz	10 ms
10 kHz	1 kHz	50 ms
5 kHz	1 kHz	20 ms
2 kHz	1 kHz	10 ms
1 kHz	100 Hz	.5 s
500 Hz	100 Hz	.2 s
200 Hz	100 Hz	.1 s
100 Hz	30 Hz	.5 s
50 Hz	30 Hz	.5 s

5. Calibrate the 1st LO System and Center Frequency Control

An alternate procedure for the 496P is provided using program control. Before proceeding with this step, check sweep timing and amplitude accuracy.

a. Adjust Coarse Tuning Range

1. Test equipment setup is shown in Fig. 3-30. Set the front-panel controls as follows:

FREQUENCY	0 MHz
FREQ SPAN/DIV	200 MHz
REF LEVEL	−20 dBm
MIN RF ATTEN	0 dB
AUTO RESOLUTION	AUTO
TIME/DIV	MNL
Vertical Display	10 dB/DIV
Video Filter	Off
Digital Storage	Off
MANUAL SCAN	Midrange

2. Connect the digital voltmeter (DVM) set to the 200 V range between TP1058 of the 1st LO Driver and chassis ground (Fig. 3-31), so the voltage at the test point can be monitored. Adjust FREQUENCY for a readout of −56 MHz as the FREQ SPAN/DIV is reduced to 5 MHz. Note the DVM reading.

3. Tune the FREQUENCY for a readout of 1871 MHz (switch FREQ SPAN/DIV to 200 MHz to facilitate tuning, then reduce to 5 MHz and press DEGAUSS for the final adjustment).

4. Note the DVM setting.

5. If the differential between −56 MHz and 1871 MHz is not 20.00 V, adjust Coarse Tune Range R1032, on the Center Frequency Control board (Fig. 3-31) until the voltage difference between the two frequency points is 20.00 V.

b. Calibrate 10 V Supply

1. Connect the DVM to TP1059, on the 1st LO Driver (Fig. 3-31A).

2. Adjust R1034 (Fig. 3-31A) for −10.00 V.

c. Adjust Sweep Offset

1. Connect a shorting strap from TP1035, on the Span Attenuator board, to chassis ground (Fig. 3-31). Monitor the voltage on TP1073 (Fig. 3-31) with the DVM.

2. Adjust Sweep Offset R1063 for 0.00 V.

3. Remove shorting strap and switch EXTERNAL MIXER off.

d. Calibrate Frequency Span to Center Frequency Readout (This is followed by an alternate procedure for 496P only instruments.)

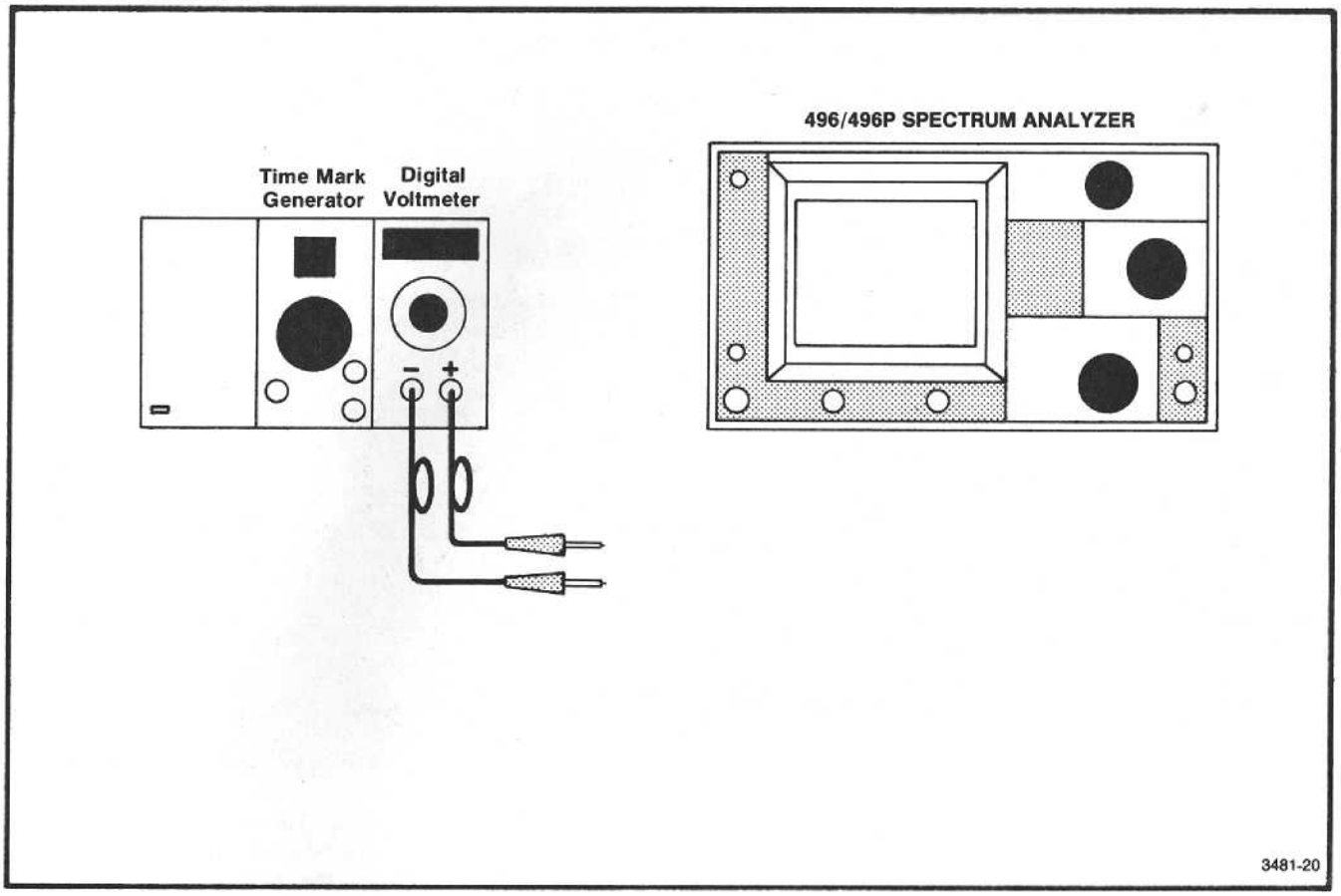


Fig. 3-30. Test equipment setup for calibrating sweep ramp for the 1st LO Driver.

1. Apply the Calibrator output to the RF INPUT. Set the FREQ SPAN/DIV to 100 MHz, activate FREQUENCY CAL, then set the readout calibration at the center of the CAL range (range is about ±15 MHz). Deactivate the FREQUENCY CAL function.

2. Initialize the front panel control settings by switching POWER off, then on. Set the FREQ SPAN/DIV to 200 MHz, TIME/DIV to AUTO, and REFERENCE LEVEL to −30 dBm (MIN RF ATTEN at 0 dB).

3. Adjust the FREQUENCY to tune the 9th marker of the Calibrator signal to the center of the screen, then reduce the FREQ SPAN/DIV to 2 MHz, activate DEGAUSS, and set the FREQUENCY readout to 900 MHz.

4. Adjust the 1st LO Offset R1032 (Fig. 3-31) on the 1st LO Driver board to center the 900 MHz marker.

5. Tune the FREQUENCY for a readout of 100 MHz (switch the SPAN/DIV to a higher setting to facilitate tuning, then back to 2 MHz). Degauss by pressing DEGAUSS.

6. Adjust 1st LO Sensitivity R1031 (Fig. 3-31) on the 1st LO Driver board to center the 100 MHz marker.

7. Repeat these steps to correct for any interaction.

ALTERNATE PROCEDURE FOR 496P INSTRUMENTS

Instructions for the 4050 program are given in parentheses.

1. Send
   "INIT;REF −20;SPAN 2M;SIG"
   "FREQ 100M;DEG;SIG;WAIT;FREQ 900M;DEG;SIG;WAIT; REP 1200"

   This will give an adjustment sequence for about two minutes. If necessary, re-send the command to complete the adjustment.

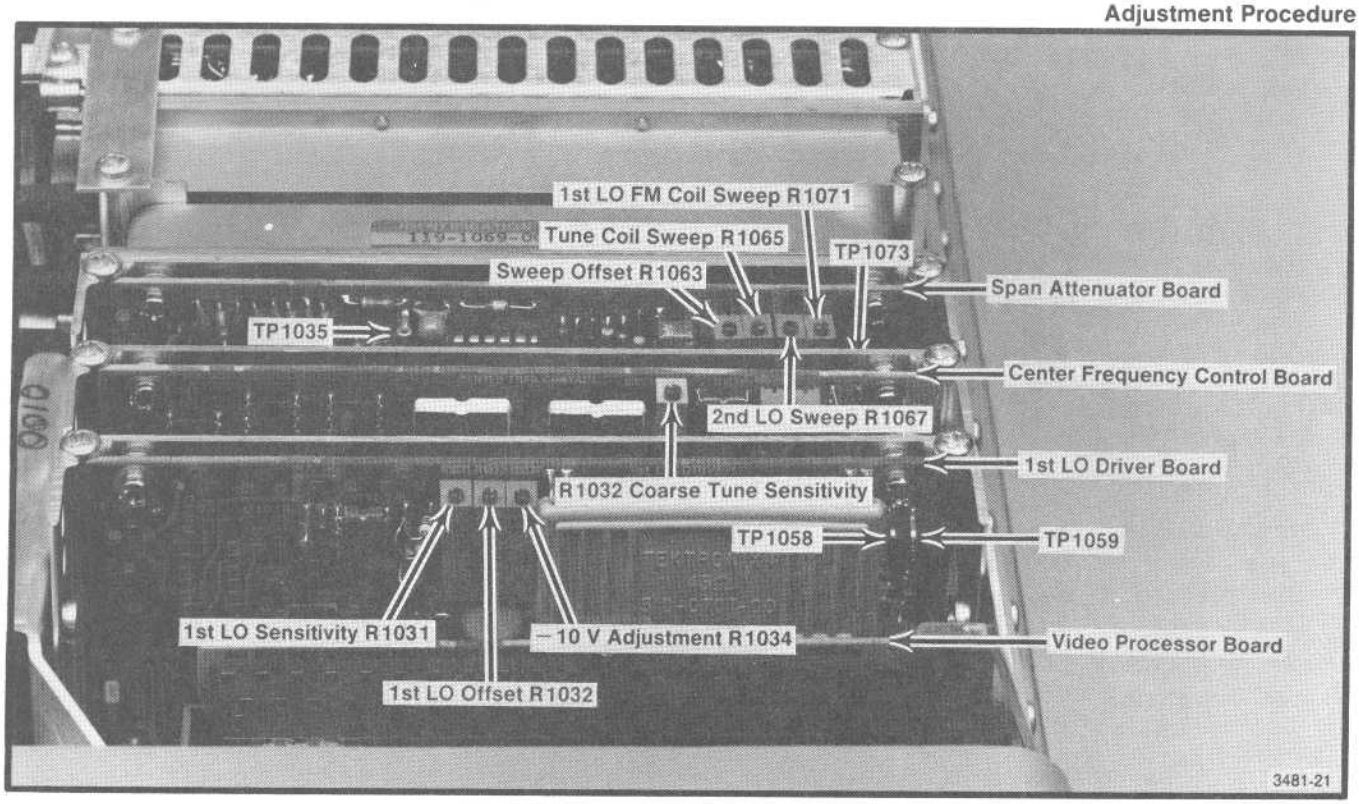


Fig. 3-31. 1st LO balance and span adjustments and test points.

(Press USER key 3 to start the sequence and press the BREAK key to stop.)

2. If the adjustments are fairly close, two signals will appear on screen on alternate sweeps; a large and a small signal. The small signal is 900 MHz, the large is 100 MHz. Proceed with the following adjustments:

a. Adjust the 1st LO Offset R1032 on the 1st LO Driver board, to bring the two signals to the same horizontal position. If one or no signals appear on screen, adjust R1031 until a signal comes on screen. Then adjust R1032 (1st LO Offset) until the second signal appears while alternately adjusting the 1st LO Sense R1031 to keep the first signal on screen;

b. Adjust 1st LO Sense R1031, on the 1st LO Driver board, to align the two signals with the vertical centerline of the graticule.

e. Adjust 1st LO and 2nd LO Sweep (Applicable to all 496 and 496P instruments)

1. With the Calibrator output applied to the RF INPUT, set the FREQ SPAN/DIV to 100 MHz and tune the FREQUENCY to about 500 MHz.

2. Adjust Tune Coil Swp R1065 (Fig. 3-31) on the Span Attenuator board so the 100 MHz harmonics of the Calibrator are spaced at one division intervals over the center eight divisions of the graticule. Adjust the FREQUENCY as necessary to align the markers.

3. Remove the Calibrator signal.

4. Set the FREQ SPAN/DIV to 2 MHz, REF LEVEL to +10 dBm, FREQUENCY about 15 MHz, then apply 0.5 μs markers from a time-mark generator to the RF INPUT.

5. Adjust the 1st LO FM Coil Swp R1071 (Fig. 3-31) for 1 marker/division over the center eight divisions of the display.

6. Change the FREQ SPAN/DIV to 20 kHz, RESOLUTION BANDWIDTH to 1 kHz and apply 50 μs markers from the time-mark generator.

7. Adjust the 2nd LO Swp R1067 (Fig. 3-31) on the Span Attenuator board for 1 marker/division. Adjust FREQUENCY control as necessary to align markers.

NOTE

Increase the value of R4076 (on the Shaper and Bias board) to 15.0 kΩ, 1% if the LO sweeps too far, and decrease the value to 10.0 kΩ, 1% if the LO does not sweep far enough.

8. Disconnect and remove the time-mark generator connection to the RF INPUT.

6. Check/Adjust 2nd LO Tuning Range (An alternate procedure is provided for the programmable 496P over the GPIB bus.)

a. Test equipment setup is shown in Fig. 3-32. Switch POWER off, remove the Center Frequency Control board, and install the board on an extender; then switch POWER on. Set the FREQUENCY to 5 MHz, FREQ SPAN/DIV to 100 kHz, REF LEVEL to 0 dBm and MIN RF ATTEN to 30 dB.

b. Apply 2 μs time markers to the RF INPUT and tune one of the marker signals to center screen.

c. Change the FREQ SPAN/DIV to 50 kHz; then tune the FREQUENCY control counterclockwise until the display stops moving.

d. Tune a marker to a graticule line, press ΔF, then rotate FREQUENCY until the readout indicates 3000 kHz. Count the markers as they pass across the screen.

e. When properly adjusted, the tune range will cover 6 markers (3000 kHz total range).

f. Adjust Fine Tune Range, R4040, on the Center Frequency board (Fig. 3-33), to correct for one half the error, and repeat the steps until the range is correct.

g. Switch POWER off, remove the extender board, and reinstall the Center Frequency Control board in the 496. Switch POWER on.

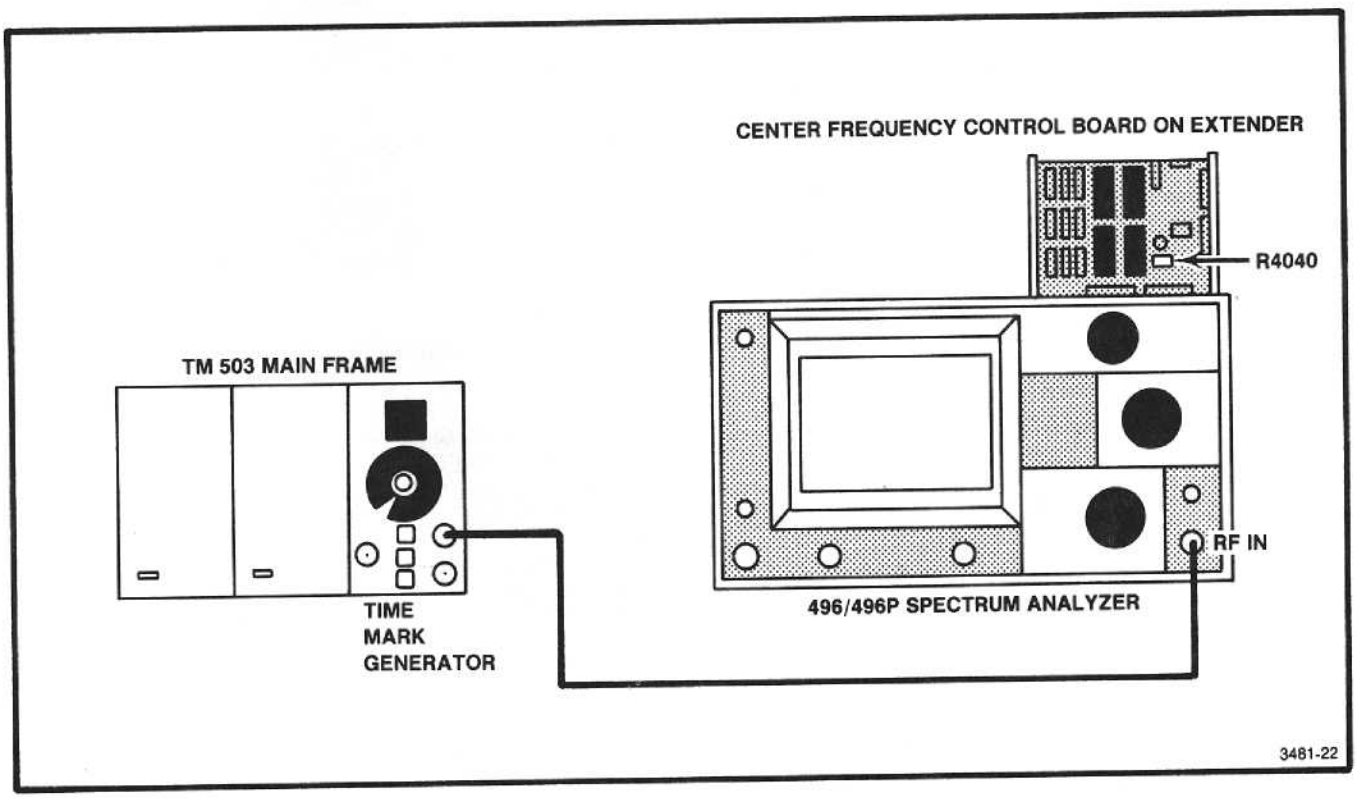


Fig. 3-32. Test equipment setup for check and adjustment of 2nd LO Tuning Range.

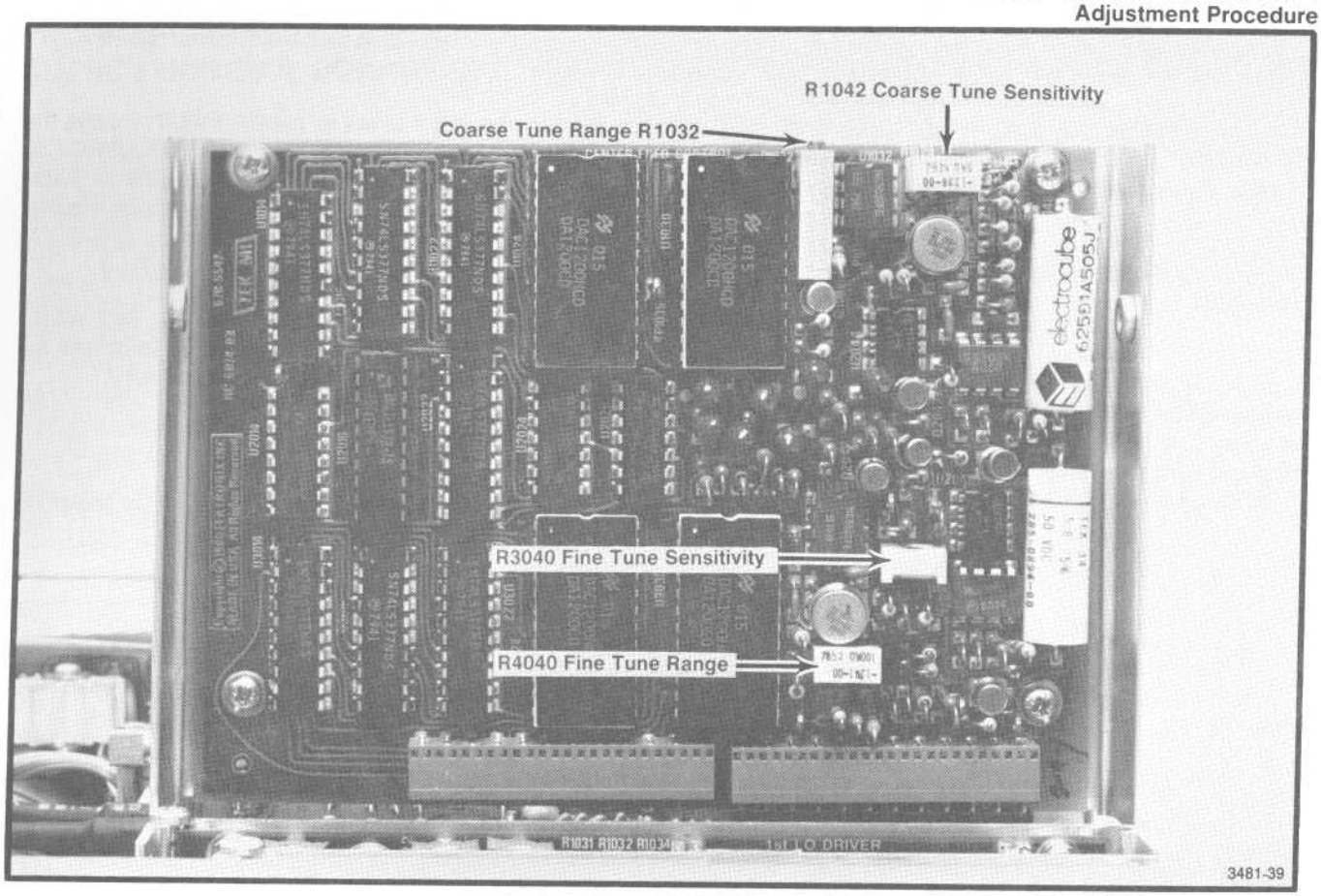


Fig. 3-33. Center Frequency Control adjustment locations.

ALTERNATE PROCEDURE FOR 496P

NOTE

Instructions in parentheses refer to the 4050-Series program as listed at the end of step 7 (Adjust 1st Converter Bias). At the end of any programmed procedure press the RETURN TO LOCAL button.

a. Adjust the 1st LO Tune Sensitivity as follows:

1) set the MIN RF ATTEN to 30 dB and apply 1 μs markers to the RF INPUT from the time mark generator. Set the FREQ SPAN/DIV to 500 kHz and adjust FREQUENCY to center the 10 MHz marker on screen;

2) send: 'FREQ 10M;SPAN 100k' to the 496P over the GPIB bus;

3) adjust the FREQUENCY control to center the marker on screen, then send: 'TUNE 5M; SIG; WAIT;TUNE −5M;SIG;WAIT;REP 1200'. This will repeat the adjustment sequence for about two minutes. Send the instruction again if necessary to complete the adjustment.

(Press USER DEFINABLE KEY #4 to start the sequence and press BREAK to stop the sequence.)

b. Adjust the Coarse Tune Sensitivity R1042 until the harmonics of alternate sweep are at the same horizontal position in the display as the regular sweep. It is not important where they are in the display, just so they are at the same horizontal location.

c. Adjust the 2nd LO Oscillator Range as follows:

1) tune the FREQUENCY to 10 MHz, set SPAN/DIV to 100 kHz, and center one of the 1 μs markers on screen. Reduce SPAN/DIV to 50 kHz.

2) tune down 1 marker. Reduce SPAN/DIV to 10 kHz.

3) send: "TUNE 2M;WAIT;TUNE −2M; SIG; WAIT; REP 1200". This will repeat the adjustment sequence for about two minutes. Repeat the command if necessary.

(Press USER DEFINABLE KEY #5 to start the sequence and BREAK to stop the sequence.)

d. Adjust Fine Tune Range R4040 until the harmonic signal in alternate sweep is at the same horizontal location on the display as the initial sweep. It is not important where in the display the two signals are as long as they are positioned together.

NOTE

Increase the value of R3077 (on the Shaper and Bias board) to 9.09 kΩ, 1%, if identify is too narrow and decrease it to 6.98 kΩ, 1%, when identify is too wide.

e. Adjust the 2nd LO Tune Sensitivity as follows:

1) apply 1.0 ms markers to the RF INPUT, change the FREQ SPAN/DIV to 1 MHz, and tune FREQUENCY to about 0 MHz. Decrease the FREQ SPAN/DIV to 5 kHz and tune the zero spur to the left side of the display. Decrease the FREQ SPAN/DIV to 100 Hz;

2) send: "TUNE 1K;SIG;WAIT;TUNE −1K; SIG; WAIT; REP 150". This will repeat the adjustment sequence for five minutes. Repeat the command if necessary.

(Press USER DEFINABLE KEY #6 to start the sequence and press BREAK to stop the sequence.)

3) adjust Fine Tune Sensitivity R3040 until the harmonics displayed in alternate sweep have the same horizontal location as the even sweep.

PROGRAM TO FACILITATE CALIBRATING THE 1st LO DRIVER AND THE CENTER FREQUENCY CONTROL BOARDS OF THE 496P, USING TEKTRONIX 4050-SERIES COMPUTER TERMINAL

```
1     ON SRQ THEN 700
2     GO TO 700
4     ON SRQ THEN 100
5     GO TO 210
8     ON SRQ THEN 100
9     GO TO 230
12    ON SRQ THEN 100
13    GO TO 300
16    ON SRQ THEN 100
17    GO TO 400
20    ON SRQ THEN 100
21    GO TO 500
24    ON SRQ THEN 100
25    GO TO 600
100   REM *** ERROR HANDLING ROUTINE ***
110   POLL Z8,Z9;A9
120   PRINT@A9:"ERR?"
130   INPUT@A9:Z$
140   PRINT Z$
150   RETURN
200   REM *** ADJUST COARSE TUNE RANGE R1032 CEN FRE CONTROL BRD ***
210   PRINT@A9:"FRE -56M"
220   RETURN
230   PRINT@A9:"FRE 1871M"
240   RETURN
300   REM *** ADJUST 1ST LO SENSE (GAIN) AND OFFSET ***
310   PRINT@A9:"FRE 100M;DEG;SIG;WAI"
320   PRINT@A9:"FRE 1.8G;DEG;SIG;WAI"
330   GO TO 310
400   REM *** ADJUST COARSE TUNE SENSITIVITY R1042 CEN FRE CON BRD ***
410   PRINT@A9:"TUN 5M;SIG;WAI"
420   PRINT@A9:"TUN -5M;SIG;WAI"
430   GO TO 410
500   REM *** ADJUST FINE TUNE RANGE R4040 CEN FRE CON BRD ***
510   PRINT@A9:"TUN 2M;SIG;WAI"
520   PRINT@A9:"TUN -2M;SIG;WAI"
530   GO TO 510
600   REM *** ADJUST FINE TUNE SENSITIVITY R3040 CEN FRE CON BRD ***
610   PRINT@A9:"TUN 1K;SIG;WAI"
620   PRINT@A9:"TUN -1K;SIG;WAI"
630   GO TO 610
700   REM *** START UP PROCEDURE ***
710   PAGE
720   PRINT "ENTER THE 496P'S GPIB PRIMARY ADDRESS";
730   INPUT@A9
740   POLL Z8,Z9;A9
750   RETURN
```

@

7. Log Amplifier Calibration

CAUTION

Use only an insulated screwdriver or tuning tool, such as Tektronix Part No. 003-0675-00, to make these adjustments.

a. Test equipment setup is shown in Fig. 3-34. Set the front-panel controls as follows:

FREQUENCY	200 MHz
FREQ SPAN/DIV	200 MHz
REF LEVEL	−70 dBm
MIN RF ATTEN	0 dB
AUTO RESOLUTION	On
TIME/DIV	AUTO
Vertical Display	10 dB/DIV
Video Filter	Off
Digital Storage	VIEW A/VIEW B
CAL (LOG and AMPL)	Centered

b. Remove P621 and apply a 10 MHz signal of 0 dBm from the signal generator, through 10 dB and 1 dB step attenuators, to the input of the Log Amplifier at J621 (Fig. 3-35). Set the step attenuators for 50 dB of attenuation.

c. Position the display at a graticule reference line with the variable output of the signal generator; then switch the REF LEVEL from −70 dBm to −120 dBm, and adjust the front panel LOG CAL so each 10 dB step equals one division.

d. Set the REF LEVEL to −20 dBm and the attenuators for 0 dB.

e. Increase the step attenuators in 10 dB steps. Adjust Log Gain, R4020 (Fig. 3-35), so each 10 dB of change produces a division of change on the display.

f. Return the step attenuator to 0 dB. Display should be full screen (0 dBm); if not, readjust the signal generator output for 0 dBm.

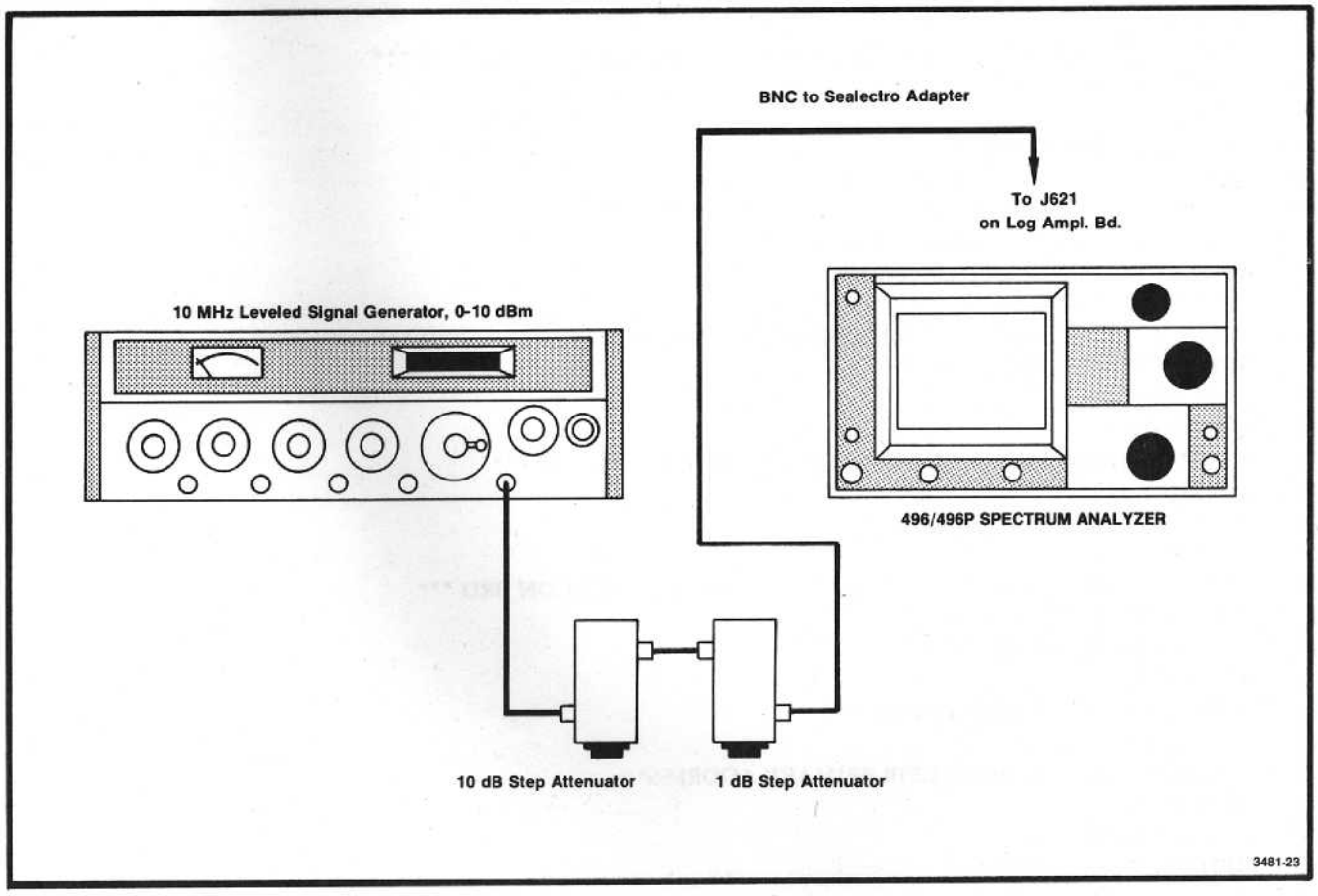


Fig. 3-34. Equipment setup for calibrating Log Amplifier.

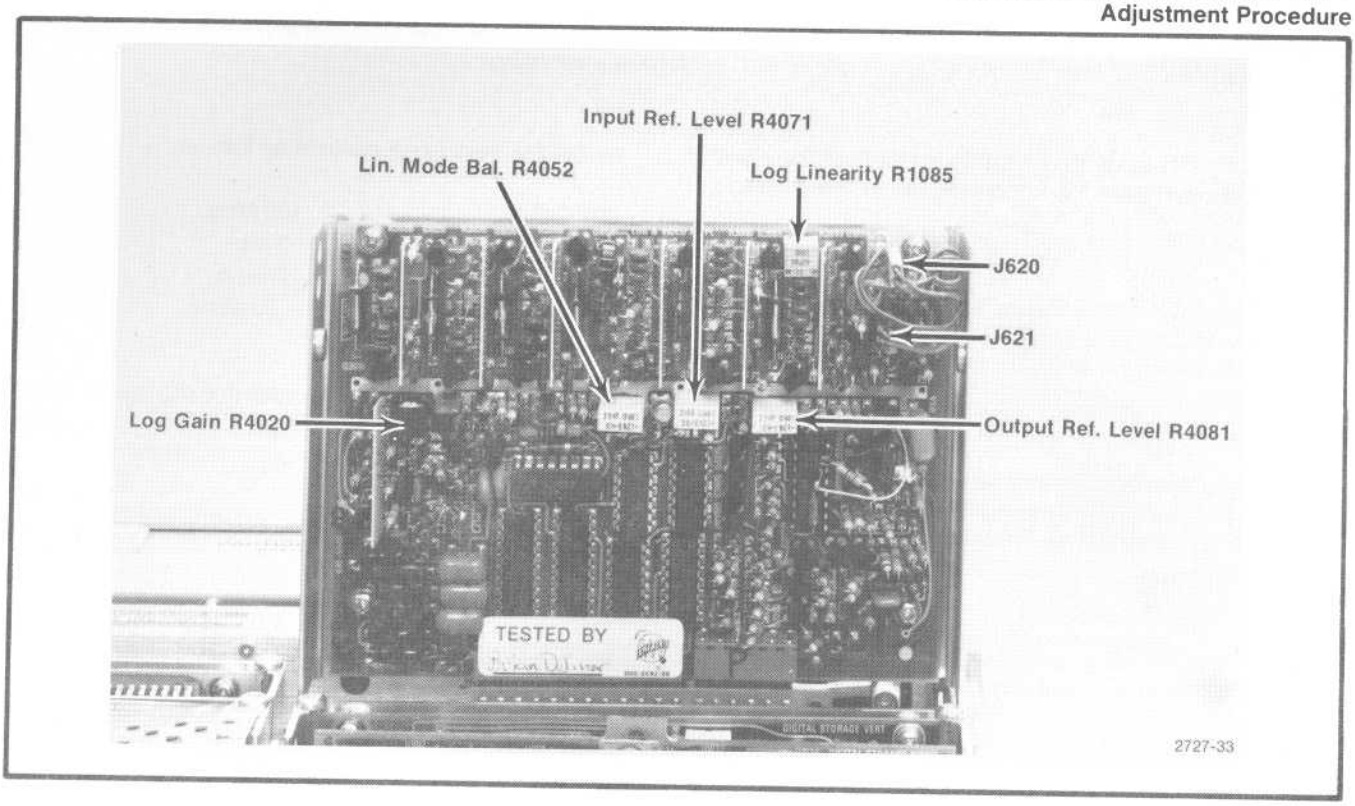


Fig. 3-35. Location of connectors and adjustments on the Log and Video Amplifier.

g. Alternately switch the Vertical Display between 10 dB/DIV and 2 dB/DIV while adjusting Input Ref Lvl, R4071 (Fig. 3-35), for minimum amplitude change between the two displays. MAY HAVE TO ADJUST R4081 TOO!

h. Switch Vert Display to 2 dB/DIV. Switch in 10 dB of attenuation and note how close the 10 dB step is to five divisions of display change. If the 10 dB step is short (trace falls short of the correct line), adjust gain with R4020 slightly in the same direction; then switch out the 10 dB of attenuation and adjust R1071 for a full screen display. Repeat this check until the 10 dB step is within 0.2 dB. Switch to 10 dB/DIV display mode and recheck 10 dB logging.

i. Switch to the 2 dB/DIV mode; then momentarily remove the input signal to the Log Amplifier and position the display on the bottom graticule line. Re-apply the signal to the Log Amplifier.

j. Adjust Output Ref Lvl, R4081 (Fig. 3-35), for a full screen (eight divisions) display.

k. Switch to the 10 dB/DIV mode and set the step attenuators for 40 dB. Adjust Log Linearity, R1085 (Fig. 3-35), so the display is mid-screen.

l. If a large change in the setting of R1085 was required in part k of this step, repeat the adjustments of R4071 and R4081 because of interaction.

m. Check the accuracy of 10 dB/DIV and 2 dB/DIV display modes by switching the attenuation in 10 dB steps for 10 dB/DIV mode and 1 dB steps for the 2 dB/DIV mode. Note that the display steps one division ±0.25 minor division for each 10 dB step, and ±1.0 minor division for the 2 dB mode. Once the individual steps have been verified, reset the signal level for full screen; then switch in the appropriate step attenuation to step the display down screen to measure the worst case error over the dynamic range. Maximum error must not exceed ±1.5 dB over the first 80 dB of range, or ±1.0 dB over the 16 dB range.

n. If the 10 dB log step in the 2 dB/DIV mode is long, adjust gain with R4020 for less gain and rebalance R4071.

o. Set the step attenuators for 10 dB of attenuation; then adjust the signal output level for a full screen display (+10 dBm) in the 2 dB/DIV mode.

p. Activate MIN NOISE and switch out the 10 dB of attenuation.

q. Check that the display level returns to within ±1.0 dB of reference.

r. Set the Ref Level to −15 dBm and adjust the signal generator output for a full screen display in the 2 dB/DIV mode.

s. Switch the Vertical Display to LIN and adjust Lin Bal, R4052 (Fig. 3-35), for a full screen display. Display amplitude of LIN, 2 dB/DIV, and 10 dB/DIV display should now be the same.

t. Check LIN mode linearity by adding 6 dB, 12 dB, and 18 dB of attenuation and noting that the display level is down from top of screen four (±0.4), six (±0.4), and seven (±0.4) divisions.

u. Remove the signal generator signal connection to the Log Amplifier input jack and replace P621.

8. Calibrating the Resolution Bandwidth and Shape Factor

NOTE

The filters are aligned separately and then combined with a signal applied through both the VR#1 and VR#2 modules. The final touch-up adjustments can be made for filter shape and bandwidth. Because of interaction, it is easy to offset one filter with misadjustment of the other; therefore, only slight adjustments should be made.

Adjust the bandwidth of each filter section at the 3 dB down level. This point should be as wide or slightly wider than the 6 dB down point of the combined two filter sections.

For gain levels and alignment theory, refer to the VR part in the Theory of Operation section.

a. Equipment setup is shown in Fig. 3-36. Place the VR module on an extender and connect the output 10 MHz signal, from the 3rd Converter, to the input of the VR#2 section. Use a Sealectro male-to-male adapter and coaxial cable to connect between P693 and J683.

b. Connect the output of VR#2 to the input of the Log Amplifier assembly by connecting a cable from J682 to J621 (see Fig. 3-35).

c. Connect the CAL OUT signal through a coaxial cable to the RF INPUT.

d. Set the front-panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	50 kHz
RESOLUTION BANDWIDTH	100 kHz
REF LEVEL	−20 dBm

e. Tune the signal to center screen and change the Vertical Display to 2 dB/DIV. Adjust the REF LEVEL for a seven division signal. Tune the display to center screen.

NOTE

The 10 kHz filter is used as the reference for centering the response of all filters.

f. Increase the FREQ SPAN/DIV to 50 kHz and the RESOLUTION BANDWIDTH to 100 kHz.

g. Adjust C2050 and C5055 (Fig. 3-37) for the best 100 kHz filter shape and waveform centering (100 kHz, 3 dB down, and centered with respect to the 10 kHz reference). Refer to Fig. 3-38.

h. Return the RESOLUTION BANDWIDTH to 10 kHz and recheck for centering. Switch the FREQ SPAN/DIV to 500 kHz and the RESOLUTION BANDWIDTH to 1 MHz.

i. Adjust C2026 and C1022 (Fig. 3-37) for the best 1 MHz filter shape and waveform centering.

j. Switch the RESOLUTION BANDWIDTH to 100 Hz and FREQ SPAN/DIV to 500 Hz.

k. Adjust the 100 Hz filter shape and response amplitude with C6011 and C7011. Adjust for maximum amplitude and a bandwidth, at the 3 dB down point, of 100 Hz.

l. Now disconnect the 10 MHz third converter signal (P693) from the VR#2 input and connect it to the input of VR#1 (J693), through the Sealectro male-to-male adapter and coaxial cable. Connect the output of VR#1 (P683) through another Sealectro male-to-male adapter and coaxial cable to the input of the Log Amplifier at J621 (Fig. 3-35).

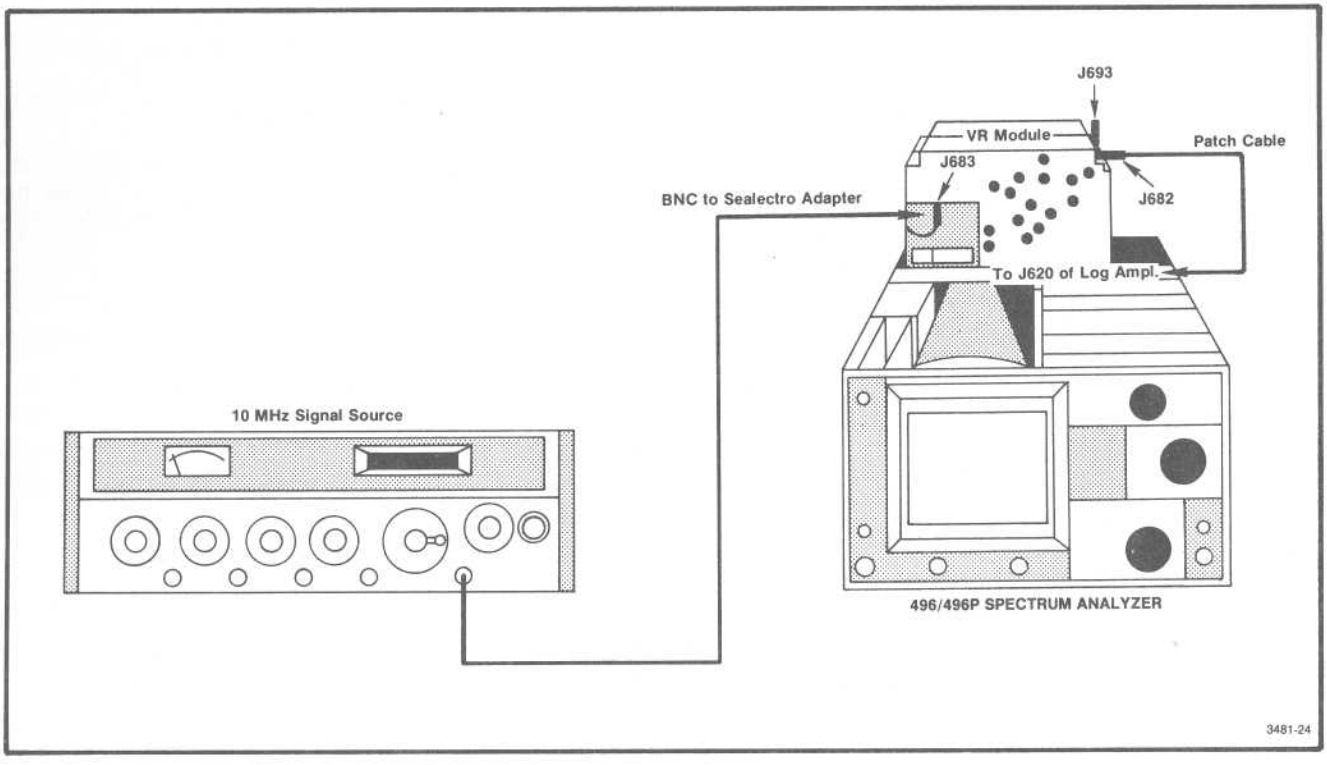


Fig. 3-36. Test equipment setup for calibrating the VR section.

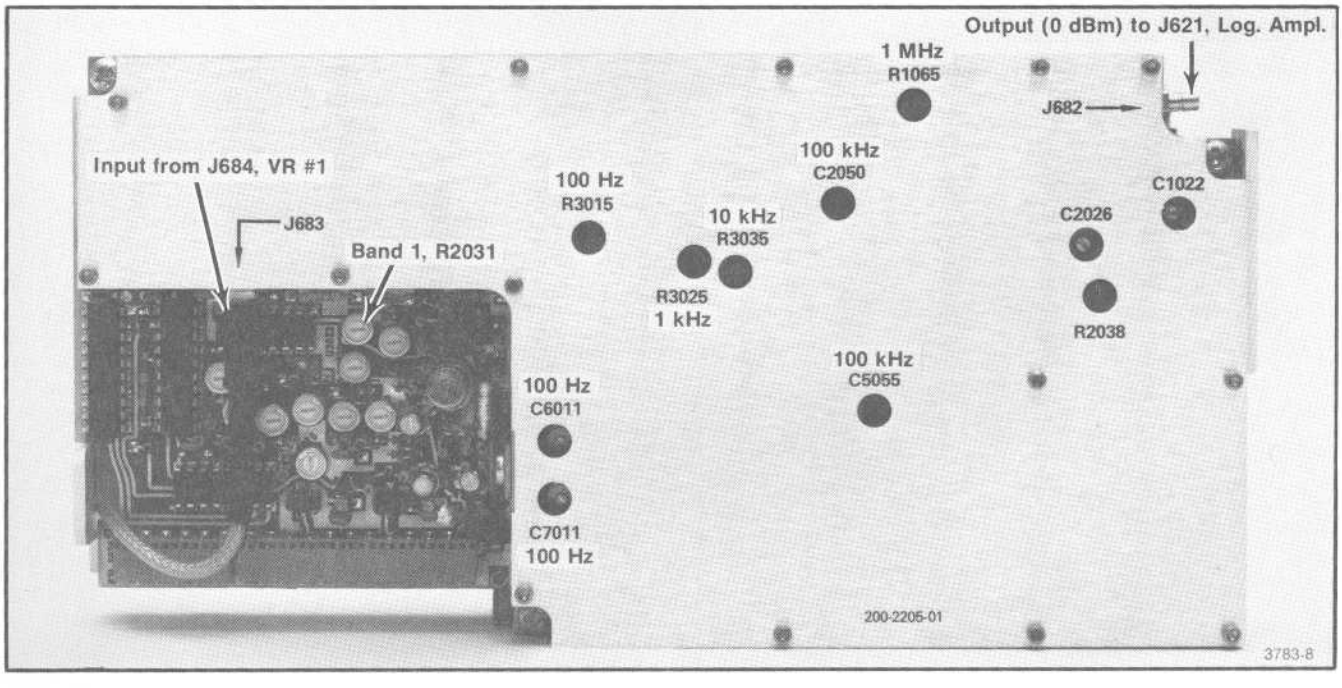


Fig. 3-37. Calibration adjustments on the VR #2 module.

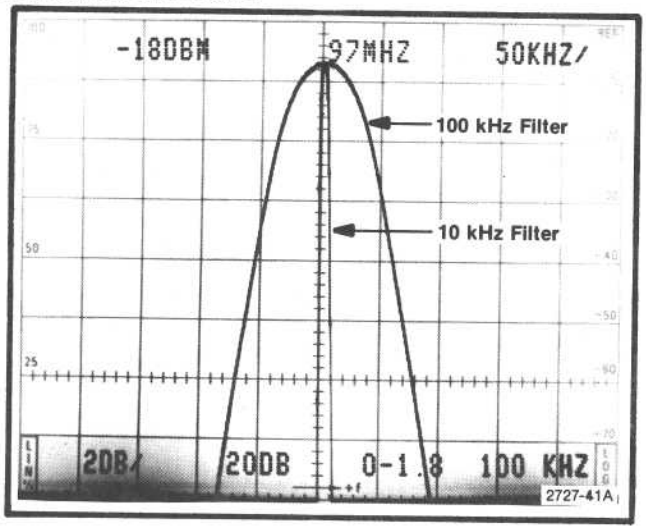


Fig. 3-38. Response of the 100 kHz filter.

m. Change the FREQ SPAN/DIV to 500 kHz and RESOLUTION BANDWIDTH to 100 kHz. Readjust the REFERENCE LEVEL for a seven division signal in the 2 dB/DIV display mode.

n. Switch the FREQ SPAN/DIV to 10 kHz and the RESOLUTION BANDWIDTH to 10 kHz. Center the response on screen.

o. Now, switch the FREQ SPAN/DIV to 50 kHz, the RESOLUTION BANDWIDTH to 100 kHz, and adjust the 100 kHz filter with C3023 and C3035 (Fig. 3-39) for filter shape and frequency centering.

p. Switch back to 10 kHz RESOLUTION BANDWIDTH and recheck centering.

q. Switch the RESOLUTION BANDWIDTH to 1 MHz and FREQ SPAN/DIV to 500 kHz; then adjust the 1 MHz filter response and centering with C1033 and C1026 (Fig. 3-39).

r. Return the FREQ SPAN/DIV to 5 kHz and RESOLUTION BANDWIDTH to 10 kHz and center the signal on screen.

s. Adjust the 10 kHz filter with C2037 (Fig. 3-39) for best filter shape.

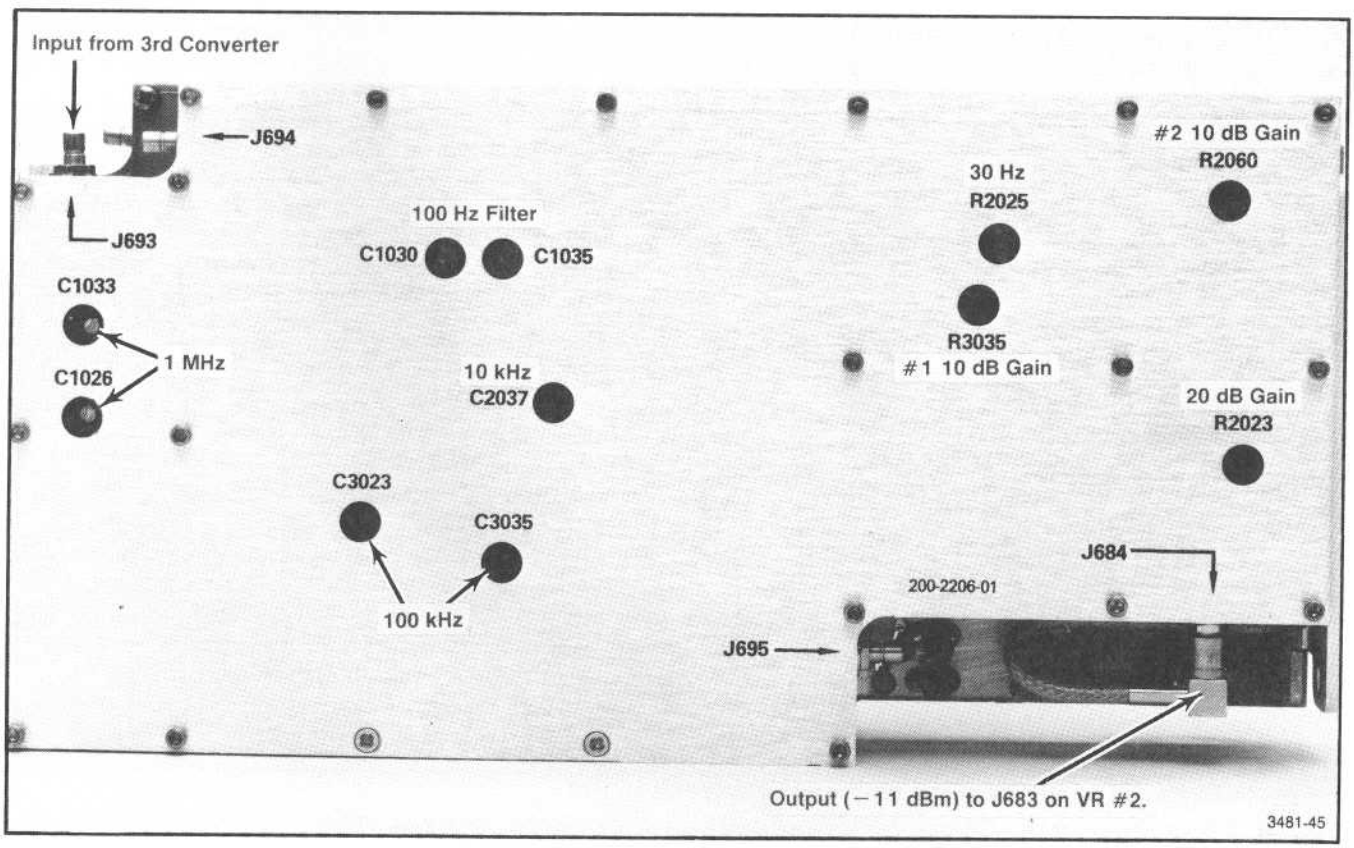


Fig. 3-39. Calibration adjustments on VR #1 module.

t. Switch the RESOLUTION BANDWIDTH to 100 Hz and the FREQ SPAN/DIV to 500 Hz. Adjust the 100 Hz filter with C1030 and C1035 (Fig. 3-39) for amplitude and waveshape.

u. Disconnect the cable between P683 and the Log Amplifier input (J621). Reconnect P683 to J683 and connect the output from the VR#2 to the Log Amplifier input (J621). The signal should now pass through both VR#1 and VR#2 to the input of the Log Amplifier.

v. Check the waveshape, bandwidth, and centering of all filters. Center the 100 kHz and 1 MHz filter response around the 10 kHz filter. If necessary, make only fine or minor adjustments. Figure 3-40 shows typical response shapes.

w. Check filter leveling using the 100 kHz filter as the reference amplitude. Adjust all filters to the 100 kHz level as follows:

Filter	Adjust	Location
1 MHz	R1065	VR#2
10 kHz	R3035	VR#2
1 kHz	R3025	VR#2
100 Hz	R3015	VR#2
30 Hz	R2025	VR#1

Locations of the adjustments are shown in Figs. 3-37 and 3-39.

9. Presetting the Variable Resolution Gain

NOTE

The Log Amplifier must be calibrated before adjusting any VR gain settings. Log Amplifier calibration can be verified by applying a 0 dBm, 10 MHz signal to the input (J621) of the Log Amplifier and checking for full screen display with a −20 dBm REF LEVEL.

The Post VR Gain, R2038 (Fig. 3-37), is normally preset by removing the VR#2 module cover and applying a −21 dBm, 10 MHz signal to pin JJ. Adjust for a full screen display with a REF LEVEL of −30 dBm. Replace the cover before proceeding with the other gain adjustments. If the range of any band gain adjustments is insufficient, add a diode between the output from U3023 and the base of Q2046, as shown on the schematic diagram for Variable Resolution No. 2.

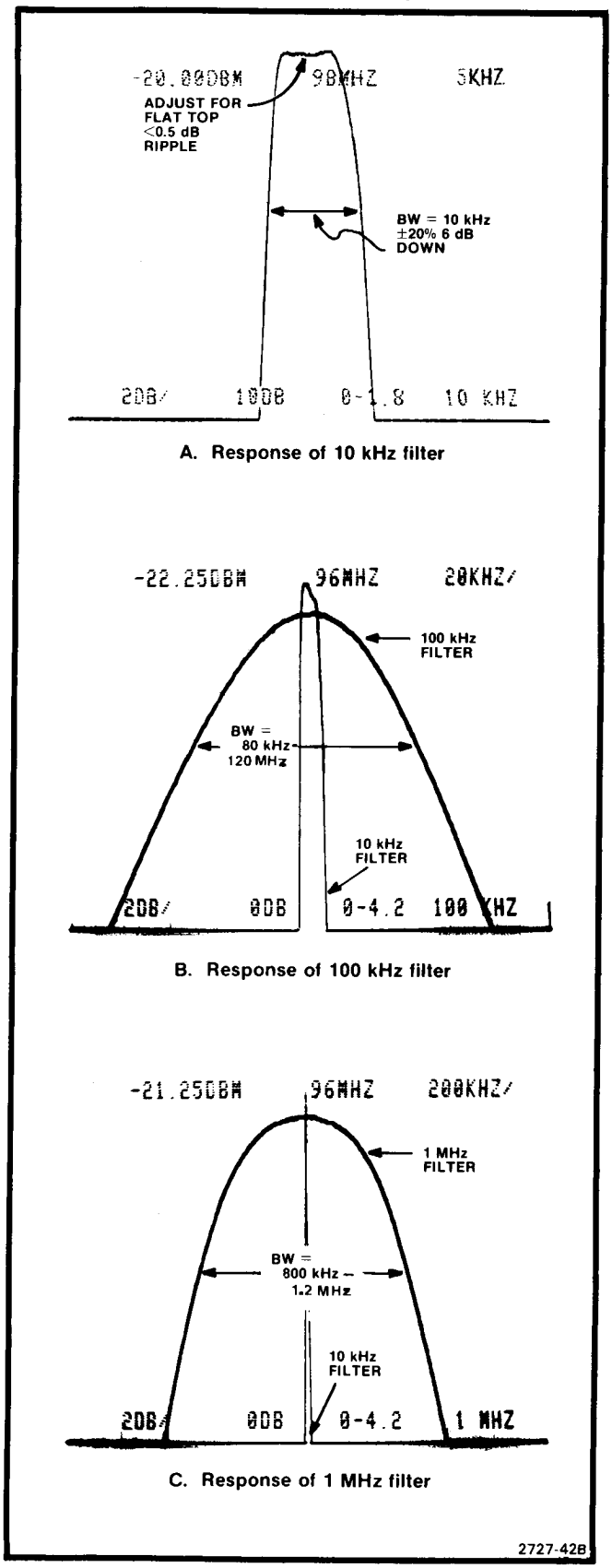


Fig. 3-40. Typical response of 10 kHz, 100 kHz, and 1 MHz bandwidth filters.

a. Test equipment is shown in Fig. 3-36. Install VR#2 module on an extender board as shown in Fig. 3-37. Set the front panel-controls as follows:

REF LEVEL	−30 dBm
MIN RF ATTEN	0 dB
FREQ SPAN/DIV	1 MHz
RESOLUTION BANDWIDTH	100 kHz
VERT DISPLAY	2 dB/DIV

b. As described in the preceding note, the gain of the Post VR Amplifier should be 21 dB for best signal-to-noise ratio through the VR stages. If any maintenance has been performed on this stage, perform the following steps.

1. Remove the cover for the VR#2 module. Disconnect the jumper connector to the input of the Post VR Amplifier (pin JJ).

2. Apply a 10 MHz, −21 dBm signal from a 50 Ω signal generator source to pin JJ of the amplifier.

3. Adjust Gain R2038 for a full screen display.

4. Remove the signal from the input to the Post VR Amplifier and replace the jumper between pins JJ of the 2nd Filter Select output and the input to the Post VR Amplifier. Replace the cover for the VR#2 module.

c. Adjust the front panel AMPL CAL to its fully ccw position and set the Band 1 Gain R2031 (Fig. 3-37) on VR#2 fully ccw.

d. Disconnect P693 from the input to VR#1 module (Fig. 3-39) and apply a 10 MHz, −35 dBm signal from the signal generator through a bnc-to-Sealectro adapter to J693. Adjust the generator frequency to peak the signal.

e. Signal amplitude should be between 3.5 and 6.5 divisions. (If signal amplitude is not within these limits it indicates a gain problem in the VR.)

f. If the signal is above 5 divisions, adjust the Post VR Gain R2038 (Fig. 3-37) for a 5 division signal amplitude (if the signal amplitude is less than 5 divisions proceed to step g).

g. Adjust the front panel AMPL CAL for a 7 division signal.

h. Decrease the generator output to −45 dBm and change the REF LEVEL to −40 dBm.

i. Adjust the 10 dB Gain R3035 (Fig. 3-39) of VR#1 so the signal amplitude is 7 divisions.

j. Change the generator output to −55 dBm and the REF LEVEL to −50 dBm.

k. Adjust the 20 dB Gain R2023 (Fig. 3-39) for a 7 division signal amplitude.

l. Change the generator output to −75 dBm and the REF LEVEL to −70 dBm.

m. Adjust the 10 dB Gain R2060 (Fig. 3-39) for a 7 division signal amplitude.

n. Increase the REF LEVEL to −30 dBm and the generator output to −35 dBm. Check for a 7 division signal amplitude. Repeat this check for −45, −55, −65, and −75 dBm input levels and note that each maintains the 7 division signal to verify that the gain of the VR gain stages are correct. Readjust gain if necessary.

o. Remove the 10 MHz signal to J680 and reconnect P680. The final band gain level adjustments are described after calibrating the Preselector Tracking and checking flatness. The mean level for each band is set to the level of band 1.

10. Calibrator Output Level

The calibrator output level is calibrated to a known reference. The procedure for checking the level is described in step 3 of the Performance Check part. Output level is adjusted with Cal Level, R1045 (Fig. 3-41). An adjustable capacitor, C3031 within the cover, is only adjusted if the oscillator fails to start. It is adjusted for maximum output. If the Cal Level adjustment (R1045) should run out of range, change the value of select resistor A34A1R1018.

11. IF Gain Calibration

a. Set the RESOLUTION BANDWIDTH to 100 kHz, REF LEVEL to −20 dBm, and apply a −21.5 dBm, 110 MHz signal through the step attenuators to the input (J365) of the 110 MHz filter (Fig. 3-41).

b. Set the step attenuators for 0 dB (with −21.5 dBm input the signal level should be 7 divisions or more). Adjust the generator output for a 7 division signal reference level.

REF −20dB, MIN NOISE, 0dB ATTEN

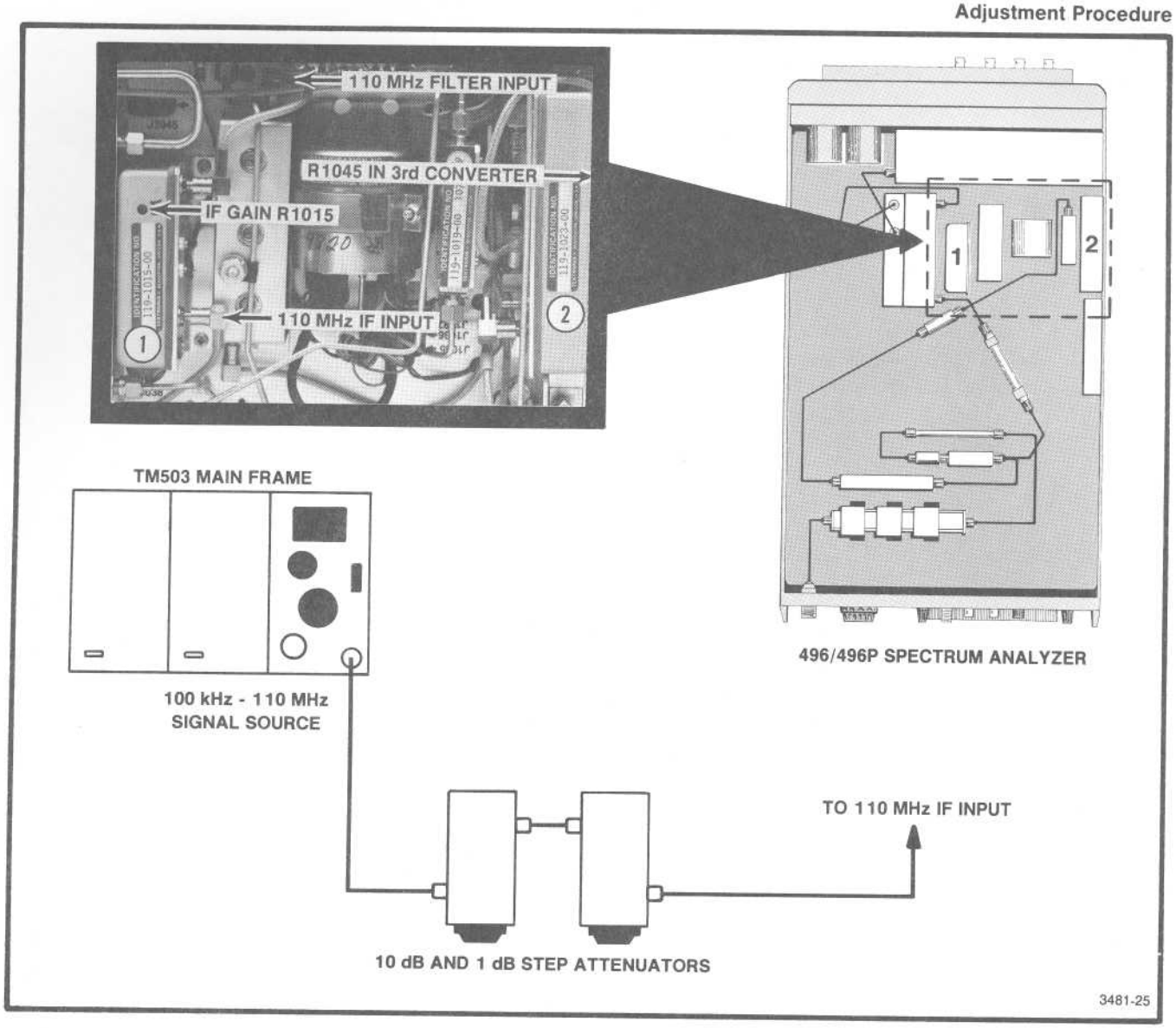


Fig. 3-41. Test equipment setup for adjusting IF gain.

c. Remove the 110 MHz signal to the 110 MHz filter and reconnect P365.

d. Set the step attenuators for 21 dB; then apply the 110 MHz signal to the input (J321) of the 110 MHz IF amplifier (Fig. 3-41).

e. Adjust the gain of the IF amplifier with R1015 for a display amplitude that equals the seven division reference set in part b.

f. Remove the 110 MHz signal and reconnect P321.

g. Apply the CAL OUT signal to the RF INPUT. Set the REF LEVEL to −20 dBm. Center the 100 MHz calibrator signal on screen then decrease the FREQ SPAN/DIV to 100 kHz with a RESOLUTION BANDWIDTH of 100 kHz. Keep the calibrator signal centered on screen with the FREQUENCY control.

h. Set the 110 MHz IF Gain R1015 (Fig. 3-41) fully clockwise (maximum gain) and set the front panel AMPL CAL fully ccw.

i. Adjust band 1 Gain R2031 for a signal amplitude of 5 divisions. (If this cannot be achieved, it indicates excessive loss through the front end.)

j. Adjust AMPL CAL for a full screen signal. AMPL CAL should now have 6 dB down range and at least 6 dB of up range.

NOTE

Two variable capacitors, C325 and C2047, do not require adjustment during calibration. Procedure requires return loss measurement which is a maintenance and repair function.

12. Digital Storage Calibration

NOTE

This is a two-part procedure; the first can be used to calibrate the 496/496P, the second is a program to be used with TEKTRONIX 4050-Series Computer terminal with the programmable 496P only.

a. Apply the CAL OUT signal to the RF INPUT and set the front-panel controls as follows:

FREQUENCY	200 MHz
FREQ SPAN/DIV	20 MHz
REF LEVEL	−10 dBm
MIN RF ATTEN	0 dB
AUTO RESOLUTION	On
TIME/DIV	AUTO
Vertical Display	10 dB/DIV
Digital Storage	VIEW A

b. Adjust the PEAK/AVERAGE cursor so it is about one division above the bottom of the screen.

c. On the Horizontal Digital Storage board:

1) adjust Horizontal Offset, R3041 (Fig. 3-42), so the left edge of the cursor is at the left edge of the crt (about 0.25 division over-span from the left graticule line);

2) adjust Output Gain, R1040 (Fig. 3-42), so the right edge of the cursor is at the right edge of the crt;

3) alternately switch the VIEW A (Digital Storage) on and off while adjusting Input Gain, R1045 (Fig. 3-42), so the storage signal at the right edge tracks with the non-store signal.

d. On the Vertical Digital Storage board:

1) output Gain R1024 and Output Offset R1036 (Fig. 3-42) are adjusted at the factory in the 496P only (the alternate procedure follows). These adjustments should not be changed; however, if they are disturbed, center these adjustments and center Input Gain R1034 before proceeding;

2) switch to 2 dB/DIV display mode;

3) using a signal near the bottom of the display, adjust Vertical Offset R1030 (Fig. 3-42), so the stored display is the same amplitude as the non-store signal;

4) change the REF LEVEL to raise the amplitude of the signal to full screen;

5) adjust Input Gain R1034 (Fig. 3-42), so the stored display of the high amplitude signal is the same as the non-store display;

6) repeat the low level and high level adjustments to compensate for interaction.

ALTERNATE PROCEDURE FOR 496P INSTRUMENTS

a. Set the front-panel controls as follows:

FREQUENCY	100 MHz
FREQ SPAN/DIV	10 MHz
REF LEVEL	−10 dBm
MIN RF ATTEN	0 dB
RESOLUTION BANDWIDTH	1 MHz
TIME/DIV	AUTO
Vertical Display	2 dB/DIV
Video Filter	NARROW
Digital Storage	VIEW A/VIEW B
PEAK/AVERAGE	Fully ccw

b. Connect CAL OUT to the RF INPUT.

c. Connect the 496P and 4050-Series Controller with a GPIB cable (both should already be turned on). Set the 496P GPIB ADDRESS switches on the rear panel for address 1 (switch 1 up, all others down).

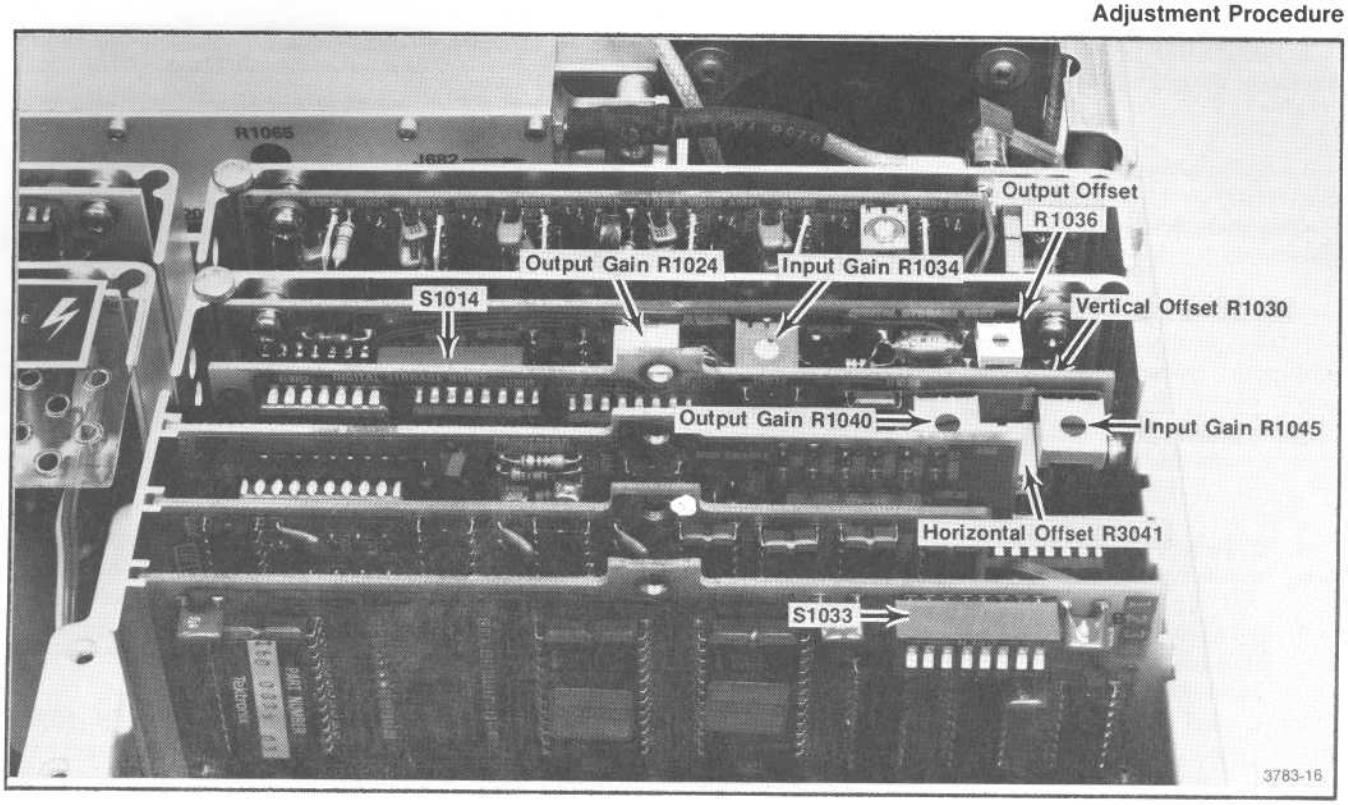


Fig. 3-42. Digital Storage adjustment locations.

d. Enter and run the following program:

```
100 DIM C(1000)
110 K=125
120 I1=0
130 FOR I=1 TO 10
140 FOR J=1 TO 100
150 C(I1+J)=K
160 NEXT J
170 K=K-25
180 I1=I1+100
190 IF K>=25 THEN 210
200 K=225
210 NEXT I
220 PRINT @1:"SIGSWP"
230 WBYTE @33:64,C,-255
```

e. Adjust the POSITION controls to center the FREQUENCY dot and place the baseline on the bottom graticule line.

f. Adjust the following (Fig. 3-42) to match the step waveform to the graticule:

Assembly	Adjustment
Horizontal Digital Storage	Horizontal Offset, R3041
Horizontal Digital Storage	Output Gain, R1040
Vertical Digital Storage	Output Offset, R1028
Vertical Digital Storage	Output Gain, R1024

Be sure that the left and right edges of the step waveform coincide with the left and right edges of the graticule. (This matches the horizontal display width of a 1000-point waveform to the graticule.)

g. Press FREE RUN and reduce the span to 200 kHz/div. Keep the signal centered with the FREQUENCY control.

h. Increase REF LEVEL for a signal peak about one division above the bottom of the graticule.

i. Cancel VIEW A, while pressing VIEW B repeatedly, and adjust Vertical Offset R1030, on the Vertical Digital Storage board to minimize the amplitude difference between the stored and real-time waveforms.

j. Reduce REF LEVEL to bring the signal peak close to the top of the graticule.

k. Again, while pressing VIEW B repeatedly, adjust Input Gain R1034 on the Vertical Digital Storge board to minimize the amplitude difference between the stored and real-time waveforms.

l. Because the offset and gain adjustments interact, repeat parts h through k as necessary.

m. Cancel the NARROW Video Filter.

n. Increase FREQ SPAN/DIV to 10 MHz and tune the signal to within one division of the right edge of the graticule.

o. While pressing VIEW B repeatedly, adjust Input Gain R1045 on the Horizontal Digital Storage board, so the horizontal position of the stored signal matches that of the non-stored signal.

13. Setting B−SAVE A Reference Level

When B−SAVE A is selected, the expression implemented is (B−SAVE A)−k where k is a constant set by the input data for an 8-to-4 line encoder, U1015. Each bit will move the reference level about 0.2 minor division. Normally, the reference level is set at the center graticule line; however, it can be set anywhere within the graticule area by the setting of an 8-bit binary switch, S1014 (Fig. 3-43). The MSB (switch #8) shifts the display about five divisions, switch #7 half this amount, etc. The following procedure sets the reference level.

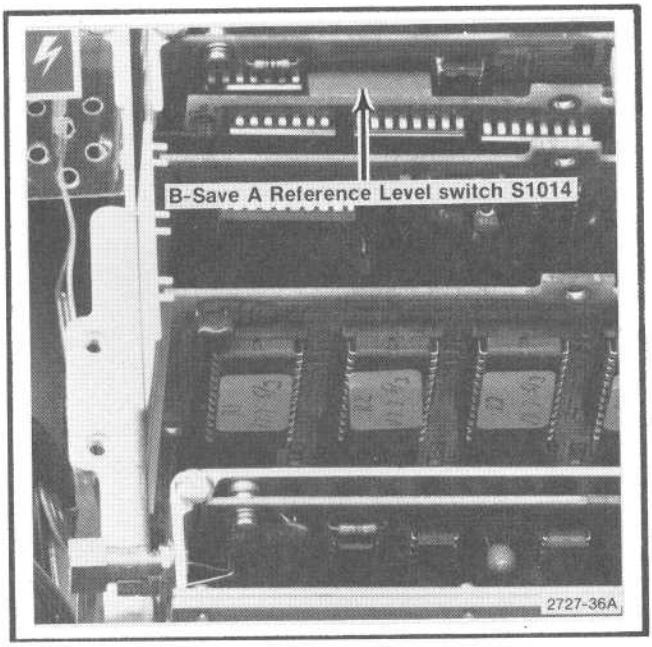


Fig. 3-43. Location of binary switch (S1014) for setting B−SAVE A reference level.

a. Estimate the amount and direction the reference level is to be shifted.

b. Switch the POWER on and close or open the switches on S1014 (Fig. 3-43) to obtain the desired B−SAVE A reference level.

This concludes the Adjustment Procedure. Refer to the appropriate Performance Check to verify specification.

MAINTENANCE

Introduction

This section describes the procedure for reducing or preventing instrument malfunction, plus troubleshooting, and corrective maintenance. Preventive maintenance improves instrument reliability. Should the instrument fail to function properly, corrective measures should be taken immediately; otherwise, additional problems may develop within the instrument.

Static-Sensitive Components

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. See Table 4-1 for relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

Observe the following precautions to avoid damage:

1) minimize handling of static-sensitive components;

2) transport and store static-sensitive components or assemblies in their original containers, on a metal rail, or on conductive foam. Label any package that contains static-sensitive assemblies or components;

3) discharge the static voltage from your body by wearing a grounded wrist strap while handling these components. Servicing static-sensitive assemblies or components should be performed only at a static-free work station by qualified service personnel;

4) nothing capable of generating or holding a static charge should be allowed on the work station surface;

5) keep the component leads shorted together whenever possible;

6) pick up components by the body, never by the leads;

7) do not slide the components over any surface;

8) avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge;

9) use a soldering iron that is connected to earth ground;

10) use only special anti-static suction type or wick type desoldering tools.

Table 4-1

RELATIVE SUSCEPTIBILITY TO STATIC DISCHARGE DAMAGE

Semiconductor Classes	Relative Susceptibility Levels[a]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs. (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFETs	6
Linear microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

[a]Voltage equivalent for levels:

1 = 100 to 500 V 4 = 500 V 7 = 400 to 1000 V (ext)
2 = 200 to 500 V 5 = 400 to 600 V 8 = 900 V
3 = 250 V 6 = 600 to 800 V 9 = 1200 V

(Voltage discharged from a 100 pF capacitor through a resistance of 100 Ω.)

PREVENTIVE MAINTENANCE

Preventive maintenance consists of cleaning, visual inspection, performance check, and if needed, a recalibration. The preventive maintenance schedule that is established for the instrument should be based on the environment in which the instrument is operated and the amount of use. Under average conditons (laboratory situation) a preventive maintenance check should be performed every 1000 hours of instrument operation.

Elapsed Time Meter

A 5000 hour elapsed time indicator, graduated in 500 hour increments is installed on the Z-Axis/RF Interface circuit board. This provides a convenient way to check operating time. The meter on new instruments may indicate from 200 to 300 hours elapsed time. Most instruments go through a factory burn-in time to improve reliability. This is similar to using aged components to improve reliability and operating stability.

Cleaning

Clean the instrument often enough to prevent dust or dirt from accumulating in or on it. Dirt acts as a thermal insulating blanket and prevents efficient heat dissipation. It also provides high resistance electrical leakage paths between conductors or components in a humid environment.

Exterior. Clean the dust from the outside of the instrument by wiping or brushing the surface with a soft cloth or small brush. The brush will remove dust from around the front-panel selector buttons. Hardened dirt may be removed with a cloth dampened in water that contains a mild detergent. Abrasive cleaners should not be used.

Interior. Clean the interior by loosening accumulated dust with a dry soft brush, then remove the loosened dirt with low pressure air to blow the dust clear. (High velocity air can damage some components.) Hardened dirt or grease may be removed with a cotton tipped applicator dampened with a solution of mild detergent in water. Do not leave detergent on critical memory components. Abrasive cleaners should not be used. If the circuit board assemblies need cleaning, remove the circuit board by referring to the instructions under Corrective Maintenance in this section.

After cleaning, allow the interior to thoroughly dry before applying power to the instrument.

CAUTION

Do not allow water to get inside any enclosed assembly or components such as the hybrid assemblies, RF Attenuator assembly, potentiometers, etc. Instructions for removing these assemblies are provided in the Corrective Maintenance section. Do not clean any plastic materials with organic cleaning solvents such as benzene, toluene, xylene, acetone or similar compounds because they may damage the plastic.

Lubrication

Components in this instrument do not require lubrication.

Service Fixtures and Tools for Maintenance

The following kits and fixtures are available to aid in servicing the 496/496P:

Nomenclature	Tektronix Part No.
Service Kit; consisting of:	006-3286-00
1 Front panel extender	067-0973-00
1 Power module extender	067-0971-00
1 Accessories Interface extender	067-0972-00
1 Ribbon cable	175-2901-00
3 Coaxial cables, Sealectro male-to-Sealectro female	175-2902-00
1 VR module handle	367-0285-00
1 Circuit board extender assembly kit: consisting of:	672-0865-00
1 Left extender board	670-5562-00
2 Right extender boards	670-5563-00
1 Frame (extrusion for circuit board extender)	426-1527-00
6 Screws, panhead with flat and lockwashers	211-0116-00

In addition to the above, the following tools are recommended:

Screwdriver, flat, with 1/4 to 3/8-inch bit.
Screwdriver, Posidrive® 440-2.
Wrench, 5/16-inch open end (used to remove or replace semi-rigid coaxial cable connectors).
Hex drive wrenches, 3/32, 5/64, 7/64-inch (used to remove hex screws that hold module assemblies and their covers in place).

Visual Inspection

After cleaning, carefully check the instrument for such defects as defective connections, damaged parts, and improperly seated transistors and integrated circuits. The remedy for most visible defects is obvious. If heat-damaged parts are discovered, try to determine the cause of overheating before the damaged part is replaced; otherwise, the damage may be repeated.

Transistor and Integrated Circuit Checks

Periodic checks of the transistors and integrated circuits are not recommended. The best measure of performance is the actual operation of the component in the circuit. Performance of these components is thoroughly checked during the performance check or recalibration; any sub-standard transistors or integrated circuits will usually be detected at that time.

When handling MOS FET's, keep the shorting strap in place until the transistor is in its socket.

Performance Checks and Recalibration

The instrument performance should be checked after each 1000 hours of operation or every six months if the instrument is used intermittently to ensure maximum performance and assist in locating defects that may not be apparent during regular operation. Instructions for conducting a performance check are provided in the Performance Check part of the Calibration section.

TROUBLESHOOTING

The following are a few aids and suggestions that may assist in locating a problem. After the defective assembly or component has been located, refer to the Corrective Maintenance part of this section for removal and replacement instructions.

Troubleshooting Aids

Diagrams. Block and circuit diagrams, on foldout pages in the Diagrams section, contain any significant waveform, voltage, and logic data information. Any necessary information as to how the data was acquired, such as operational state of the instrument, is provided on the diagram or adjacent to it. Refer to the Replaceable Electrical Parts list section for a description of all assemblies and components.

NOTE

Corrections and modifications to the manual and instrument are described on inserts bound into the rear of the manual. Check this section for changes and corrections to the manual or the instrument.

Circuit Board Illustrations. Electrical components, connectors, and test points are identified on circuit board illustrations located on the inside fold of the corresponding circuit diagram or the back of the preceding diagram. A grid on the circuit board illustrations and the circuit schematic plus a look-up table, provides the means to quickly locate components on either diagram.

Wiring Color Code. Color coded wires are used to aid circuit tracing. Power supply dc voltage leads have either a red background for positive voltage or a violet background for negative voltage. Signal wires and coaxial cables use an identifying one-band or two-band color code.

Multiple Terminal (Harmonica) Connectors. Some intercircuit connections are made through pin connectors that may be mounted in a harmonica type holder. The terminals in the holder are identified by numbers that appear on the holder and the circuit diagrams. Connector orientation to the circuit board is keyed by triangles on the holder and the circuit board (see Fig. 4-1). In some cases, the triangle or arrow is screened on the chassis adjacent to the connector. Some connectors contain more than one section. Connectors are identified on the schematic and board with a "P" or "J".

Resistor Values. Many types of resistors (such as composition, metal film, tapped, thick film resistor network package, plate, etc.) are used in the 496/496P. The value is either color coded in accordance with the EIA color code, or printed on the body of the component.

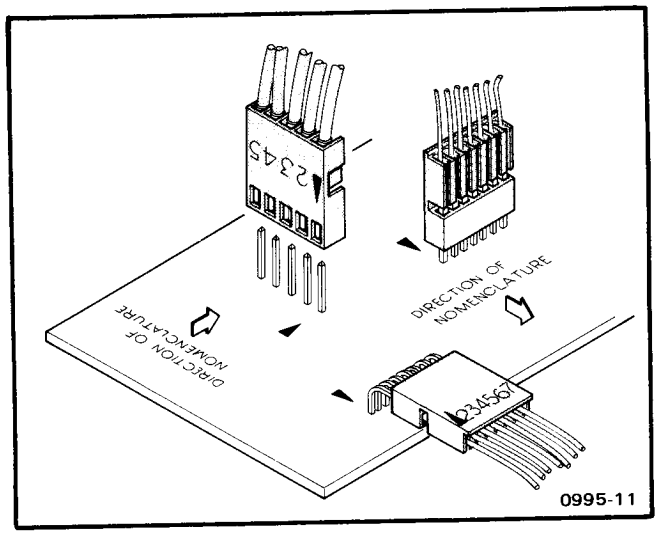


Fig. 4-1. Multipin (harmonica) connector configuration.

Capacitor Marking. The capacitance value of ceramic disc plate and slug capacitors or small electrolytics are marked in microfarads on the side of the component body. The ceramic tubular capacitors and feedthrough capacitors are color coded in picofarads. Tantalum capacitors are color coded as shown in Fig. 4-2.

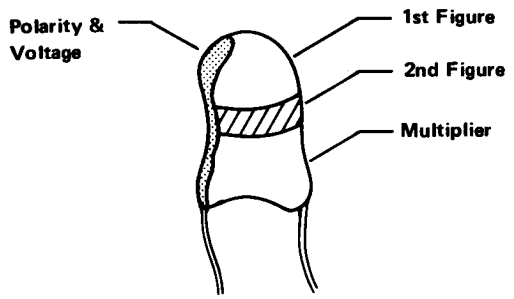
Diode Color Code. The cathode of each glass encased diode is indicated by a stripe, a series of stripes, or a dot. Some diodes have a diode symbol printed on one side. Figure 4-3 illustrates diode types and polarity markings that are used in this instrument.

Transistor and Integrated Circuit Electrode Configuration. Lead identification for the transistors and MOS FET's is shown in Fig. 4-4. IC pin outs are shown either by table or box on the schematic diagram.

Semiconductor failures account for the majority of electronic equipment failures. Most semiconductors are soldered to the boards. The following guidelines should be observed when substituting these components.

NOTE

Before using any test equipment to make measurements on static-sensitive components or assemblies, be certain that any voltage or current supplied by the test equipment does not exceed the limits of the components to be tested.



DIPPED TANTALUM CAPACITOR MARKING

A AND B CASE

CAPACITANCE AND VOLTAGE COLOR CODE

Rated Voltage VDC 25°C	Color	CODE FOR CAPACITANCE IN PICOFARADS		
		1st Figure	2nd Figure	Multiplier
3-4	Black	0	0	None
3-6	Brown	1	1	X10
3-10	Red	2	2	$X10^2$
3-15	Orange	3	3	$X10^3$
3-20	Yellow	4	4	$X10^4$
3-25	Green	5	5	$X10^5$
3-35	Blue	6	6	$X10^6$
3-50	Violet	7	7	$X10^7$
	Gray	8	8	
3	White	9	9	

(1733) 1735-9

Fig. 4-2. Color code for some tantalum capacitors.

1. Try to isolate the problem to a component through signal analysis. Determine that circuit voltages will not damage the replacement.

2. Turn the power off before removing a component.

3. Use a de-soldering tool and 25 watt or less soldering iron to remove the components.

4. Use only good components for substitution and be sure the new component is inserted into the socket properly before soldering. Refer to the manufacturer's data sheet or Fig. 4-3 for lead configuration.

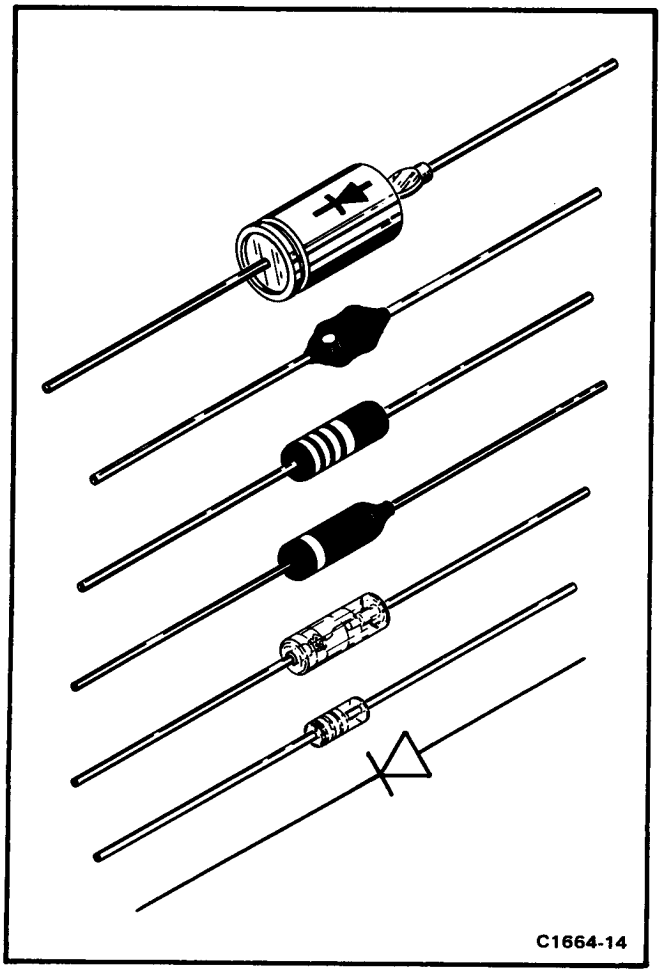


Fig. 4-3. Diode polarity markings.

5. Turn power on and check performance.

NOTE

If a substitute is not available, check the transistor or MOS FET with a dynamic tester such as the TEKTRONIX Type 576 Curve Tracer. Static type testers, such as an ohmmeter, can be used to check the resistance ratio across some semiconductor junctions if no other method is available. (Do not measure resistance across MOS FET's because they are very susceptible to static charges.) Use the high resistance ranges (R X 1k or higher) so the external test current is limited to less than 6 mA. If uncertain, measure the external test current with an ammeter. Resistance ratios across base-to-emitter or base-to-collector junctions usually run 100:1 or higher. The ratio is measured by connecting the meter leads across the terminals, noting the reading, then reversing the leads and noting the second reading.

Diode Checks. Most diodes can be checked in the circuit by taking measurements across the diode and comparing these with voltages listed on the diagram. Forward-to-back resistance ratios can usually be taken by referring to the schematic and pulling appropriate transistors and pin connectors to remove low resistance loops around the diode.

CAUTION

Do not use an ohmmeter scale with a high external current to check the diode junction. Do not check the forward-to-back resistance ratios of mixer diodes. See Replacing the Dual Diode Assembly instructions under Replacing Assemblies.

WARNING

The 496/496P uses a high efficiency power supply. The potential of the primary ground for this supply is different than chassis or earth ground. An isolation transformer, with a turns ratio of 1:1 and a 500 VA minimum rating, should be used between the power source and the 496/496P power input receptacle. The transformer must have a three-wire input and output connector with ground through the input and output. Stancor No. 6298 is a suitable transformer. A jumper should also be connected between the primary ground side to chassis ground (emitter of Q2061 and the ground terminal of the input filter FL301).

If the power supply is separated from the instrument and operated on the bench, hazardous potentials will exist within the supply for several seconds after power is disconnected. This is due to the slow discharge of capacitors C6101 and C6111. A relaxation oscillator lights DS 5112 (next to C6111) when the potential exceeds 80 volts.

General Troubleshooting Techniques

The following procedure is recommended to isolate a problem and expedite repairs.

1. Ensure that the malfunction exists in the instrument. Check the operation of associated equipment and the operating procedure of the 496/496P (see Operating Instructions).

2. Determine and evaluate all trouble symptoms. Try to isolate the problem to a circuit or assembly. For example: Absence of the frequency marker dot could indicate a mal-

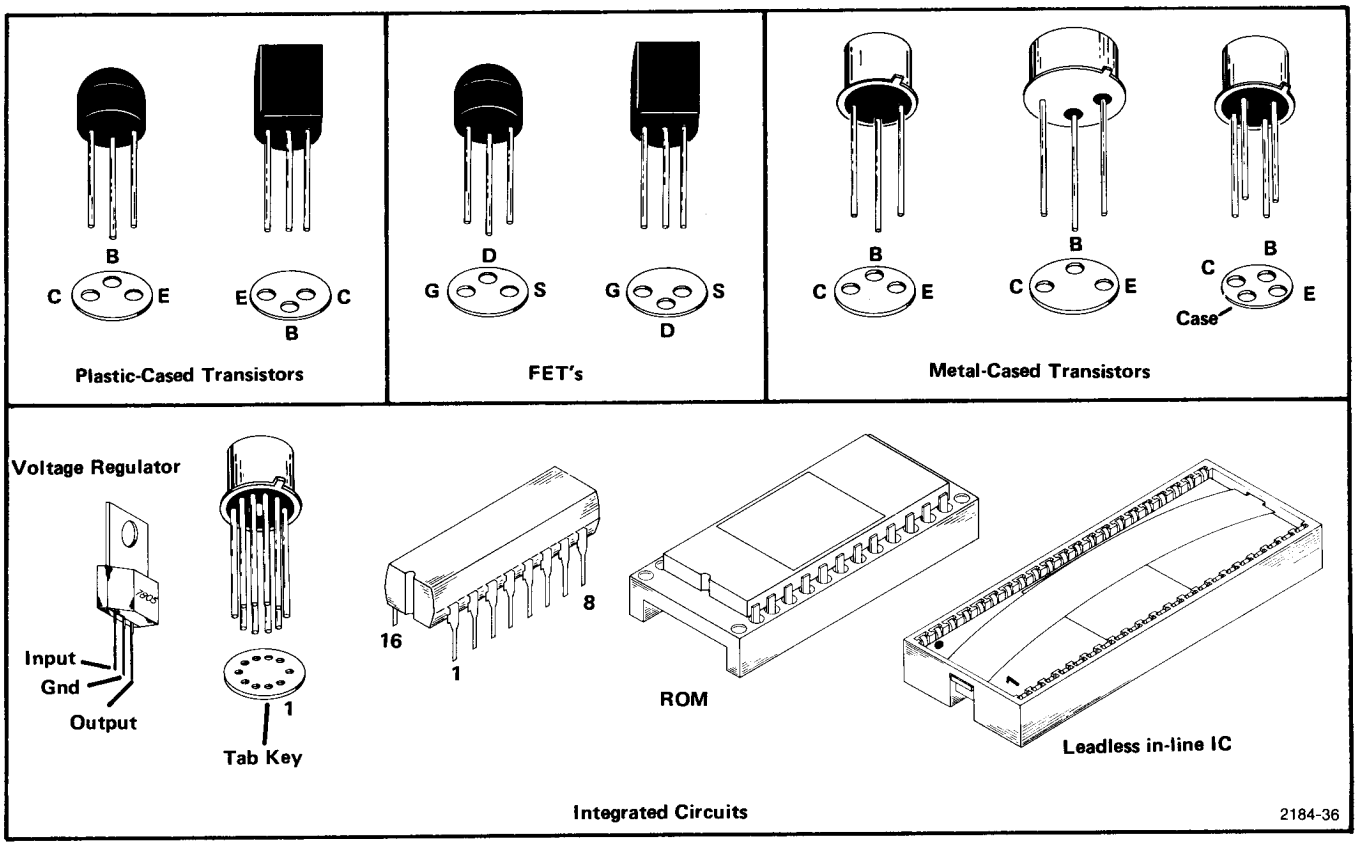


Fig. 4-4. Pin configuration for semiconductor components.

function in the video summing stage, the marker generator, or the switching circuitry. A test oscilloscope will check the input to the video summing stage and isolate the problem to one or the other of the two circuits. The block diagrams in the Diagrams section can aid in signal tracing and circuit isolation. It also shows the required signal level at different points to produce full screen deflection.

Block diagrams are provided in three levels. The first level shows all major circuit systems for the 496/496P, the second level shows detail block diagrams of each system, such as the phaselock system, and the third level shows a block diagram of a given circuit or circuit board within the system. Levels two and three block diagrams usually contain signal and voltage levels for each stage.

CAUTION

When measuring voltages and waveforms, use extreme care in placing meter leads or probes. Because of high component density and limited access within the instrument, an inadvertent movement of the leads or probe could cause a short circuit. This may produce transient voltages which can destroy many components.

3. Make an educated guess as to the nature of the problem such as component failure or calibration, and the functional area most likely at fault.

4. Visually inspect the area or assembly for such defects as broken or loose connections, improperly seated components, overheated or burned components, chafed insulation, etc. Repair or replace all obvious defects. In the case of overheated components, try to determine the cause of the overheated condition and correct before applying power.

5. By successive electrical checks, locate the problem. At this time an oscilloscope or signature analyzer is a valuable test item for evaluating circuit performance. If applicable, check the calibration adjustments. Before changing an adjustment, note its position so it can be returned to its original setting. This will facilitate recalibration after the trouble has been located and repaired.

6. Determine the extent of the repair needed; if complex, we recommend contacting your local Tektronix Field Office or representative. If minor, such as a component replacement, see the Replaceable Parts list for replacement information. Removal and replacement procedure of the assemblies and sub-assemblies is described under Corrective Maintenance.

CORRECTIVE MAINTENANCE

Corrective maintenance consists of component replacement and instrument repair. Special techniques and procedures required to replace components in this instrument are described here.

Obtaining Replacement Parts

All electrical and mechanical parts are available through your local Tektronix Field Office or representative. The Replaceable Parts list section contains information on how to order these replacement parts.

NOTE

Some components that are heat sinked to the circuit board extrusion or module wall are soldered to the board after the board is mounted in place. This is necessary to avoid cracking the IC case when the mounting screw is tightened. These components are identified by a note on the schematic drawing. Their part number appears with chassis mounted components in the Replaceable Electrical Parts list.

Parts orientation and lead dress should be duplicated because some components are oriented to reduce interaction or control circuit characteristics.

If a part you have ordered has been replaced with a new or improved part, your local Field Office or representative will contact you concerning any change in the part number. After repair, the circuits may need recalibration.

Parts Repair and Return Program

Assemblies containing hybrid circuits or substrates in a semi-sealed module, complex assemblies such as the YIG oscillator or phase gate detector, can be returned to Tektronix for repair under the repair and return program. Contact your local Field Office for exchange rates.

Tektronix repair centers provide replacement or repair service on major assemblies as well as the unit. Return the instrument or assembly to your local Field Office for this service.

Soldering Techniques

CAUTION

Disconnect the instrument from its power source before replacing or soldering components.

Some of the circuit boards in this instrument are multilayer; therefore, extreme caution must be used when a soldered component is removed or replaced. Excess heat from the soldering iron and bent component leads may pull the plating out of the hole. We suggest clipping the old component free. Leave enough lead length so the new component leads can be soldered in place. If you desire to remove the component leads, use a 15 watt or less pencil type iron. Straighten the leads on the back side of the board; then when the solder melts, gently pull the soldered lead through the hole. A desoldering tool should be used to remove the old solder.

Replacing the Square Pin for the Multi-pin Connectors

It is important not to damage or disturb the ferrule when removing the old stub of a broken pin. The ferrule is pressed into the circuit board and provides a base for soldering the pin connector.

If the broken stub is long enough, grasp it with a pair of needle nose pliers, apply heat with a small soldering iron to the pin base of the ferrule, and pull the old pin out. (The pin is pressed into the ferrule so a firm pull is required to pull it out.)

If the broken stub is too short to grasp with pliers, use a small dowel (0.028 inch in diameter) clamped in a vise to push the pin out of the ferrule after the solder has been heated.

The old ferrule can be cleaned by reheating the solder and placing a sharp object such as a toothpick or small dowel into the hole. A 0.031 inch drill mounted in a pin vise may also be used to ream the solder out of the old ferrule.

Use a pair of diagonal cutters to remove the ferrule from the new pin; then insert the pin into the old ferrule and solder the pin to both sides of the ferrule.

If it is necessary to bend the new pin, grasp the base of the pin with needle nose pliers and bend against the pressure of the pliers to avoid breaking the board around the ferrule.

Selected Components

Some components, such as microcircuits, are selected to meet Tektronix specifications. These components carry only Tektronix part numbers under the Mfr Part number column, in the Replaceable Parts list.

Some circuits require a selected component value to compensate for parameter differences between active components. These are identified on the circuit diagram and the Replaceable Parts list. The Replaceble Parts list description for the component gives either a nominal value or range of value. If the procedure for selection is not obvious or complex, such as setting the gain or response of a stage, the criteria for selection is explained in the Calibration or this section of the manual. Where the selection procedure is obvious, such as establishing the frequency of an oscillator, no procedure is given.

Installing Matched Crystals for the 100 Hz VR Filters

The crystals for the 100 Hz filter circuit of the VR assembly are matched. The four crystals come with rubber tie-down straps. Plug the matched crystals into the two boards, insert the rubber tie-down into the two holes provided on either side of the crystal on the board and pull through until the crystal is held in place by the tension of the rubber tie-down.

Replacing EPROM's or ROM's

Firmware for the microcomputer is contained in ROM's on the Memory and GPIB boards. Refer to the Replaceable Electrical Parts list (Vol. 2) under these assemblies (A54 Memory, and A56 GPIB) for the versions and IC part numbers.

Firmware Version and Error Message Readout

This feature of the 496/496P provides readout of the firmware version when the power on/off is cycled. During the initial power-up cycle, the firmware version flashes on screen for approximately two seconds. The Replaceable Electrical Parts list section, under Memory board (A54), lists the ROM's and their Tektronix part number for each firmware version.

An additional feature is error message readout. The following is a list of these messages and their meaning.

Error #	Meaning
57	Tune routine failed to carry from lower DAC.
58	Failed to phaselock.
59	Lost lock.
60	Failed to recenter when phaselock cancelled or when going to an unlocked span.

Servicing the VR Module

The VR module requires mechanical support when it is installed on board extenders. Mechanical support is provided by moving the mounting plate at the upper side of the module (Fig. 4-5A) to the bottom side. This allows installation of a mounting screw through a support bracket into the mounting plate screw hole as shown in Fig. 4-5B.

REPLACING ASSEMBLIES AND SUBASSEMBLIES

Most assemblies or sub-assemblies in this instrument are easily removed and replaced. The following describes procedures for replacing those assemblies that require special attention. Top and bottom views of the 496/496P are shown in Figs. 4-6 and 4-7. These figures identify most assemblies by name and assembly number.

Removing or Replacing Semi-rigid Coaxial Cables

Performance of the instrument is easily degraded if these connectors are loose, dirty, or damaged. The following procedure will help ensure good performance.

Replacing the Dual Diode Assembly

The diode sub-assembly housing the Schottky mixer diodes permits easy field replacement of the diodes.

CAUTION

The diodes are beam-lead devices mounted on a quartz suspended substrate; these diodes are extremely static sensitive. Refer to the Caution note on static at the beginning of this section. Do not expose the diode assembly to any RF field.

1. Use a 5/16 inch open-end wrench to loosen or tighten the connectors. When loosening, it is good practice to use a second wrench to hold the rigid (receptacle) portion of the connector to prevent bending or twisting the cable. Tighten slightly more than finger tight or until the cable just starts to twist.

2. Ensure that the plug and receptacle are clean and free of any foreign matter.

3. Insert the plug connector fully into the receptacle before screwing the nut on.

The diode sub-assembly is secured in place with four 0-80 screws. An 8-32 threaded hole is provided to facilitate insertion and removal of the sub-assembly. There are three contact points located on the substrate side of the sub-assembly. Use care when mounting and orienting these contacts with the mating contacts in the mixer assembly to ensure proper fit and function. Insertion and removal of the sub-assembly more than twice is not recommended due to the gold ribbon attach technique used in fabrication.

A tuning screw, mounted through the top of the diode assembly, adjacent to the 8-32 screw hole is adjusted to minimize the zero Hz spur. Although pre-calibrated, care should be taken not to force the tuning screw after it bottoms out on the surface of the quartz suspended substrate. (The null usually occurs about one turn from the bottom.)

The diode assembly is packaged in a static-free package. Keep the diode sub-assembly in this package until ready to install. The following procedure should be used when replacing this sub-assembly.

1. Remove the two mounting screws and remove the assembly from the 496/496P; then loosen and disconnect the three coaxial cable connections to the mixer assembly.

2. Remove the four 0-80 screws and insert a 8-32 screw into the threaded hole provided in the center of the diode assembly.

3. Lift the diode assembly out of the mixer assembly by means of the 8-32 screw; then remove the screw.

4. Open the diode package, grasp the diode assembly by its side with tweezers and place it on a static-free surface. Grasp the side of the assembly with the fingers to avoid contact with the diodes and insert the 8-32 screw.

5. Orient the diode assembly so the three contact tips are aligned with their respective contacts in the mixer; then using the index fingers of both hands so equal pressure is applied, press the sub-assembly into place.

6. Insert the four mounting screws, tighten, then replace and tighten the three coaxial connectors so they are just snug. Install the two mounting screws that hold the assembly in the 496/496P.

7. Refer to Start Spur Adjustment procedure, in the Maintenance Adjustment part of this section for calibrating the zero-hertz response amplitude.

Replacing the Crt

Removal

1. Remove the snap-in printed bezel and crt light filter.

2. Use a 8/64 inch Allen wrench to remove the four bezel screws, unplug and remove the inner bezel.

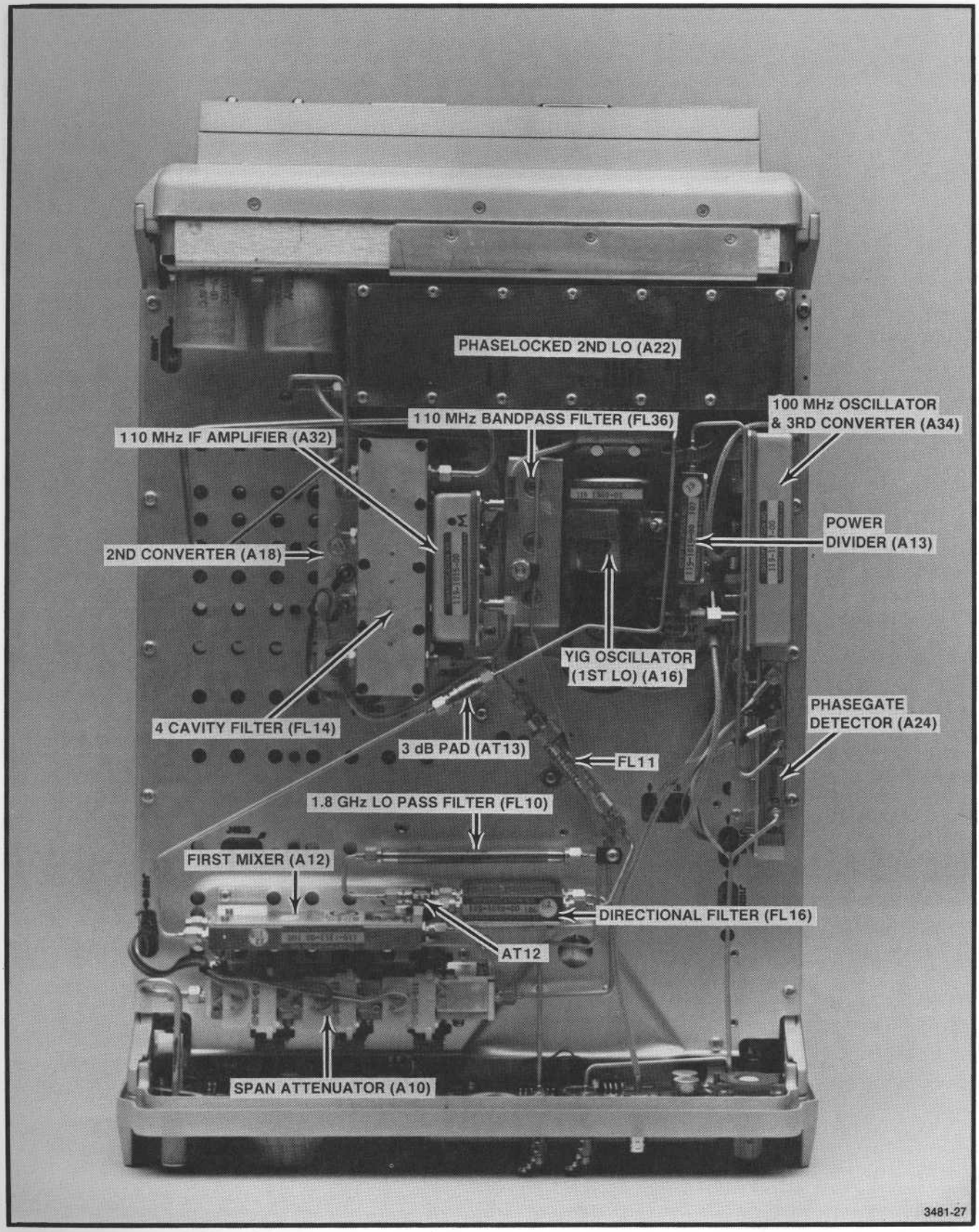


Fig. 4-6. View of the 496/496P RF deck showing major assemblies.

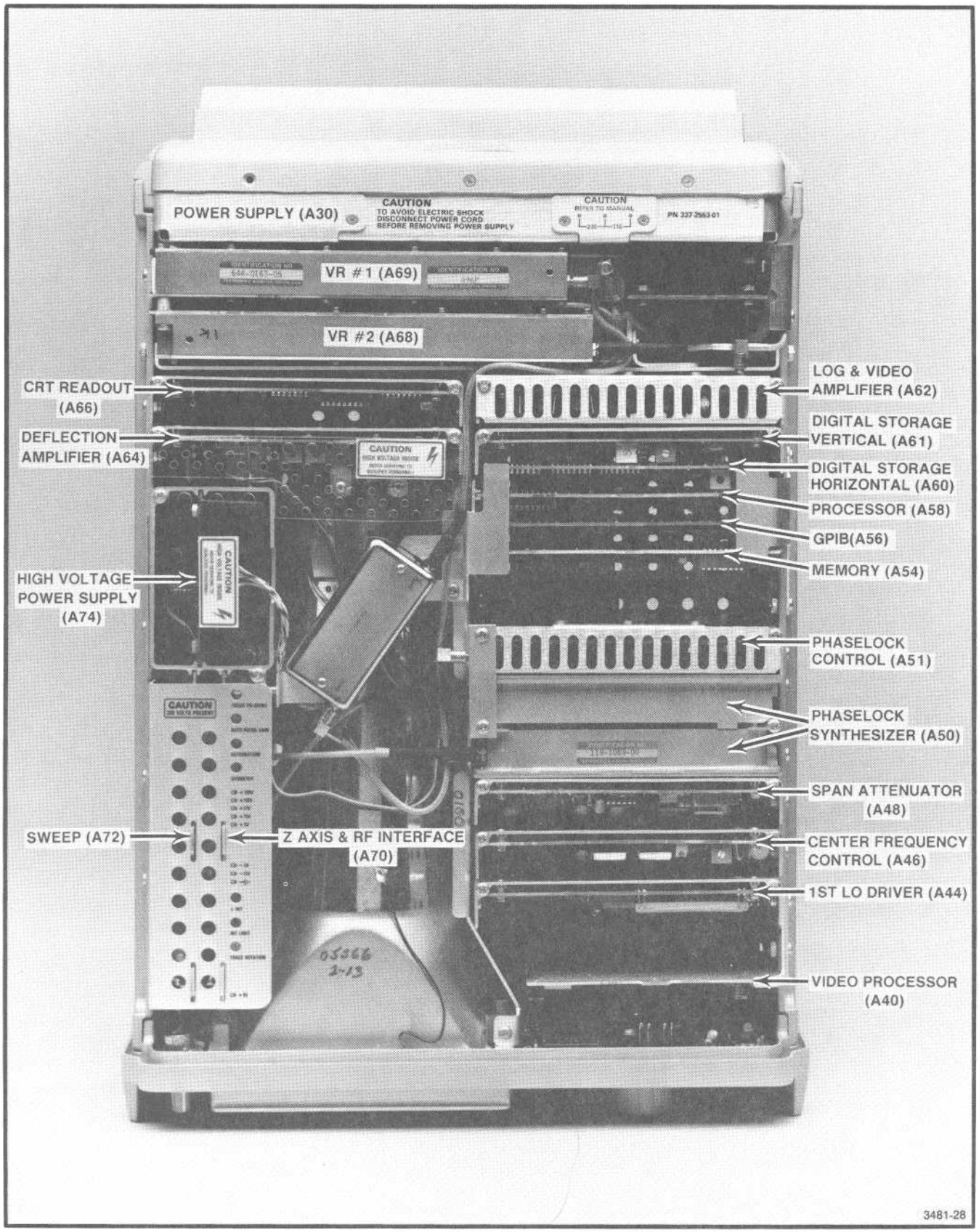


Fig. 4-7. View of the 496/496P top deck showing major assemblies.

3. Unsolder the ground wire from the front-panel casting and unplug the crt cables at their respective board connections (high voltage module, deflection amplifier, and Z-Axis board).

4. Slide the crt, with its shield, out through the front panel.

5. Remove the crt shield as follows:

a) remove the tube base cap and unplug the socket;
b) remove the two side screws that hold the upper shield in place; then remove the shield;
c) loosen the screws that clamp the plastic bracket around the crt; then remove the bracket.

Replacement

1. Install the plastic bracket so the back on the clamp is 5.07 inches from the back of the crt socket guide.

2. Replace the crt shield plus the socket and base shield by reversing the removal procedure. The finished crt assembly length, with cap installed, must equal 11.05 inches. If it is longer, the assembly may short circuit the Log Amplifier circuit board when it is installed.

3. Install crt with shield assembly into the front panel. Install bezel and tighten the four mounting screws.

CAUTION

Do not reposition the front-panel blue plastic crt holders. They have been factory aligned so the crt assembly seats properly. Visually inspect to ensure that the crt assembly clears the circuit board components.

4. Reconnect cables to their respective board connectors and resolder the ground lead to its terminal. Replace crt light filter and snap-in bezel.

Repairing the Crt Trace Rotation Coil

The trace rotation coil is part of the crt assembly. If the coil is damaged beyond repair, the crt with the coil must be replaced.

If the "finish" (red) lead is broken, remove the tape and unwind one or two turns so it can be respliced and soldered to the lead wire. Rewind and retape.

If the "start" (black) lead is broken and the lead is too short to resplice, attempt to fish out the broken end so one or two turns can be unwound. Resplice and solder to the lead; then rewind and retape.

Front-Panel Assembly

The front-panel assembly does not have to be removed to replace any of the push buttons. Refer to Replacing Front-Panel Push Buttons procedure that follows. The crt is removed with the front-panel assembly.

Removal

1. Unscrew and remove the mounting nuts and washers for the RF INPUT and the two 1st and 2nd LO OUTPUT connectors.

2. Remove the two screws that hold the front panel to the RF deck (center and left side).

3. Unplug the CAL OUT coaxial cable from the 3rd Converter; then disconnect the five crt cables from the Z-Axis/RF Interface, High Voltage module, and Deflection Amplifier.

4. Looking at the top of the instrument, remove the one screw that holds the front panel to the side extrusion, between the crt and the right side of the instrument.

5. Now set the instrument on its side and remove the four screws that hold the front panel to the side rails.

6. Pull the front panel up and off the Mother board.

Replacement

Replace the front panel by reversing the removal procedure.

Front-Panel Board

Removal

1. Remove the front-panel assembly as described previously.

2. Use an Allen wrench to loosen the knob locking screw and remove all knobs.

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3. Lay the front-panel on its face; then remove the eleven circuit board screws and the screw that heat sinks and holds IC U6090 on the board. Note that the screw next to the connector plug has a fiber washer.

4. To prevent losing the grounding rings or bushings between the front-panel controls and the front-panel casting, hold the circuit board against the front-panel casting while turning the complete assembly so it rests on the base of the crt assembly.

5. Gently lift the casting from the circuit board. Ensure that the grounding rings remain on the shaft of all controls as the casting is removed.

Replacement

Reverse the removal procedure, ensuring that the fiber washer is on the board screw next to the connector plug. This washer prevents the screw from shorting a circuit board run to the front-panel casting.

Replacing Front-Panel Push Button Switches

The front-panel assembly does not have to be removed to replace any push button switch. The procedure follows.

1. Remove front-panel knobs. Loosen and remove nuts and washers for the RF INPUT and the 1st and 2nd LO connectors.

2. Remove the screw that was under the FREQUENCY tuning knob which holds the panel to the front-panel casting.

3. Loosen the black screws through the crt bezel so the panel can be moved enough to lift it off the casting.

4. Unplug and replace the desired switches.

Main Power Supply Module

CAUTION

To avoid damage to the Mother board connector J5041 and Interface connector J1034 during removal or installation of the Power Supply Module, use the following procedure.

Removal

1. Disconnect the power cord, set the 496/496P on its face or front panel and remove the instrument cover.

2. Unplug the coaxial cable connector P620 from the Log Amplifier assembly and pull the cable through so it is clear.

3. Remove the three screws that hold the power module to the RF deck flange (bottom right side).

4. Remove the four screws that hold the power supply module to the side-rails.

5. With the instrument on its face and the RF deck on the near side, pull the left side of the power module from its side-rail (no more than one and one-half inch). Now grasp both sides of the module and lift to separate the module from the Mother board.

WARNING

Because C6011 and C6101 discharge very slowly, hazardous potentials exist within the power supply for several minutes after the power switch is turned off. A relaxation oscillator, formed by C5113, R5111, and DS5112, indicate the presence of voltages in the circuit until the potential across the filter capacitors is below 80 V.

Replacement

1. Set the instrument face down with the RF deck on the near side.

2. Hold the power supply module over the instrument so the right side is touching the side-rail and the left side is about one and one-half inch above its side-rail.

3. Align connectors P5041 and P1034 with their respective Mother board and Interface board connectors and press the module into place between the side-rails.

4. Replace the four module holding screws and the three flange screws.

5. Thread the coaxial cable under the semi-rigid cables on the RF deck and through the deck opening to the Log Amplifier assembly connector J620 so the cable will not catch when the instrument cover is replaced.

6. Replace the instrument cover.

High Voltage Power Supply

Before the High Voltage Power Supply circuit board can be unplugged and removed, a screw through the side-rail into a nylon standoff bushing, at the bottom corner of the board, must be removed.

Replacing the 1st (YIG) Local Oscillator Interface Board

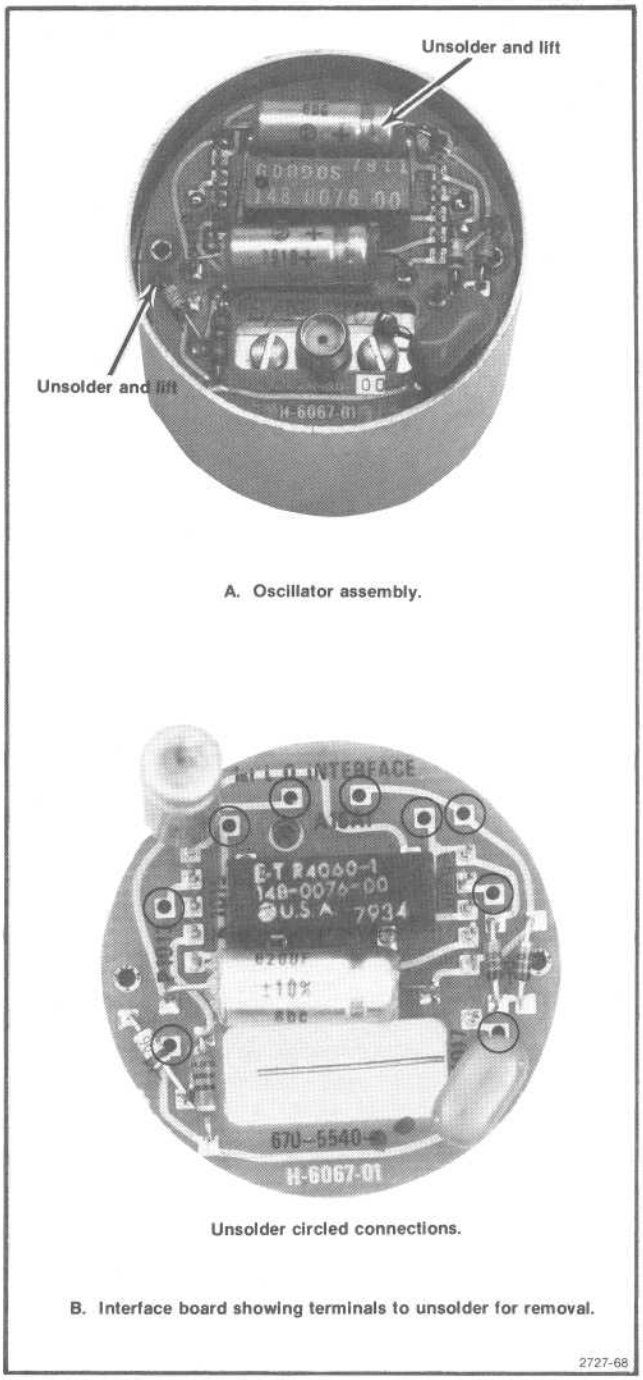
The YIG oscillator assembly includes an interface circuit board that can be ordered separately. To replace the board refer to Fig. 4-8 and the following procedure. Use a desoldering tool to remove the solder as these leads are unsoldered.

1. Unsolder and lift one end of C1014 (820 μF) capacitor at the top of the board.

2. Unsolder and lift one end of VR1010.

3. Unsolder and lift the wire to the ground lug on P166.

4. Unsolder the eight leads to the YIG and lift the board off the assembly.



A. Oscillator assembly.

Unsolder circled connections.

B. Interface board showing terminals to unsolder for removal.

2727-68

Fig. 4-8 Removing YIG oscillator interface circuit board.

MAINTENANCE ADJUSTMENTS

The following procedures are not part of the regular calibration. They are applicable when an assembly is replaced or after major repair.

110 MHz IF Assembly Return Loss Calibration

NOTE

The IF assembly must be removed to gain access to the adjustments.

Table 4-2
EQUIPMENT REQUIRED FOR 110 MHz IF ASSEMBLY CALIBRATION

Test Equipment	Characteristics	Recommended Type
Spectrum Analyzer	Frequency range ≥110 MHz	TEKTRONIX 496/496P or 7L13 Spectrum Analyzer
Signal Generator	Frequency 110 MHz at +10 dBm	TEKTRONIX SG 503 for the TM 500 Series
VSWR Bridge		Wiltron VSWR Bridge, Model 62BF50
10 dB and 1 dB Step Attenuators	50 Ω, 0 dB to 40 dB	TEKTRONIX 2701 Attenuator
Termination	50 Ω	Tektronix Part No. 011-0049-01
Adapter	Bnc-to-Sealectro	Tektronix Part No. 175-0419-00

1. Test equipment setup is shown in Fig. 4-9. Apply 110 MHz at 2 V peak to peak (+10 dBm) through 35 dB attenuation to the RF Input of the VSWR bridge. Connect the RF Out of the VSWR bridge to the RF Input of the spectrum analyzer. (Do not connect the 110 MHz IF to the VSWR bridge.)

2. Set the spectrum analyzer center frequency to 110 MHz, SPAN/DIV to 5 MHz, RESOLUTION BANDWIDTH to 3 MHz, VERTICAL DISPLAY to 10 dB/DIV, and REFERENCE LEVEL to −20 dBm.

3. Adjust the step attenuator for full screen (−20 dBm) display.

4. Connect the 110 MHz IF input to the VSWR bridge and connect a 50 Ω termination to the output of the IF amplifier. Now plug the power cable P3045 into the + and −15 V source and ground the case of the assembly.

5. Adjust C2047 and C325 (Fig. 4-10) simultaneously for minimum signal amplitude on the spectrum analyzer display. Minimum amplitude must be at least 35 dB down from the full screen reference of −20 dBm.

6. Disconnect test equipment setup and replace the 110 MHz IF assembly.

2072 MHz 2nd Converter

CAUTION

Do not open the assembly. Adjust the tuning slug only after checking the filter characteristics.

The 2nd Converter assembly consists of a four cavity 2072 MHz bandpass filter, mixer, and a 110 MHz lowpass filter. The assembly is calibrated at the factory, prior to installation, and requires no calibration after it is installed. We recommend replacing the assembly if it should malfunction. The following procedure describes adjustments that can be made if the biasing should malfunction or the seal on any of the filter tuning slugs is broken. The mixer diodes are not to be replaced in the field. Return the assembly to Tektronix, Inc., for repair.

FOUR CAVITY FILTER

The characteristics of the filter are checked with a network analyzer. Frequency of the filter is 2072 MHz,

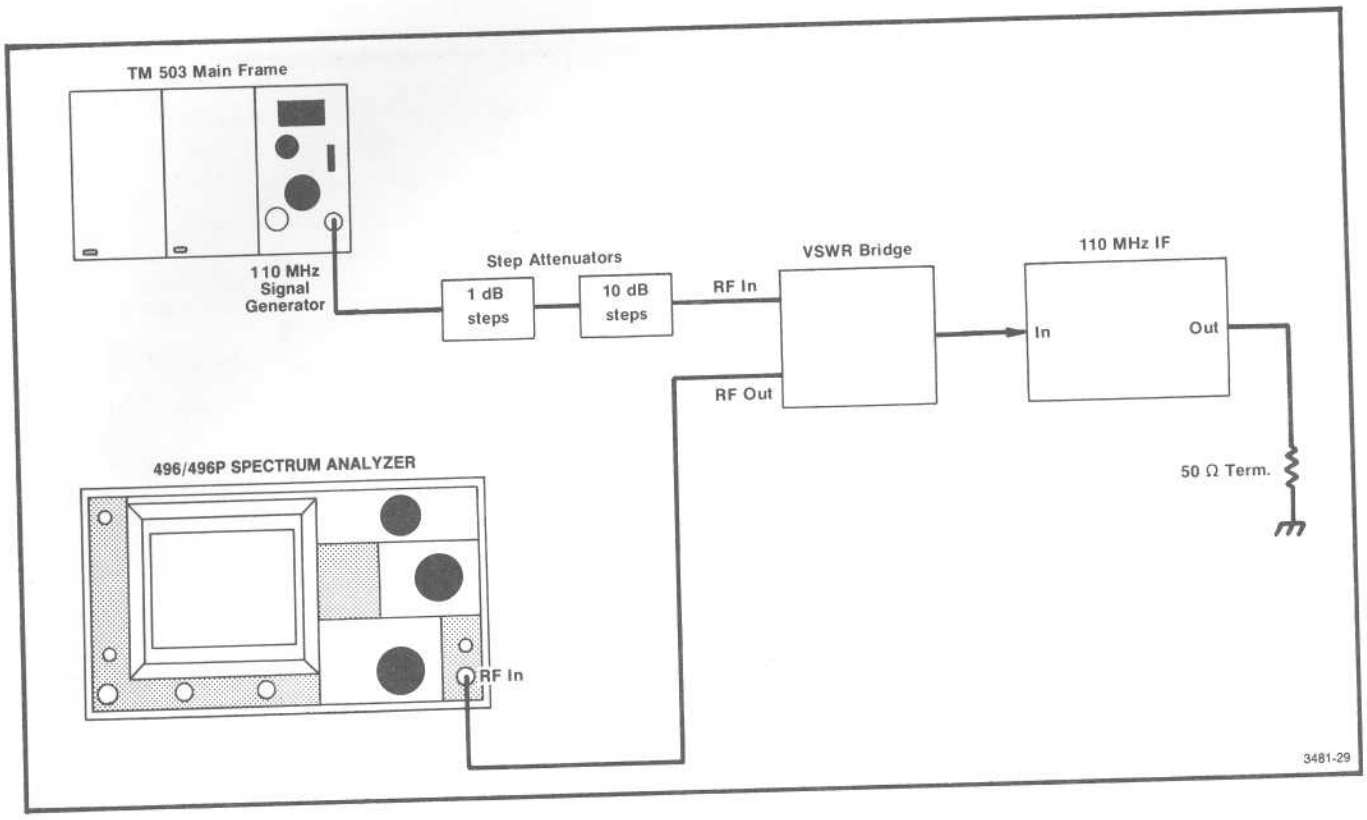


Fig. 4-9. Test equipment setup for adjusting return loss of the 110 MHz IF assembly.

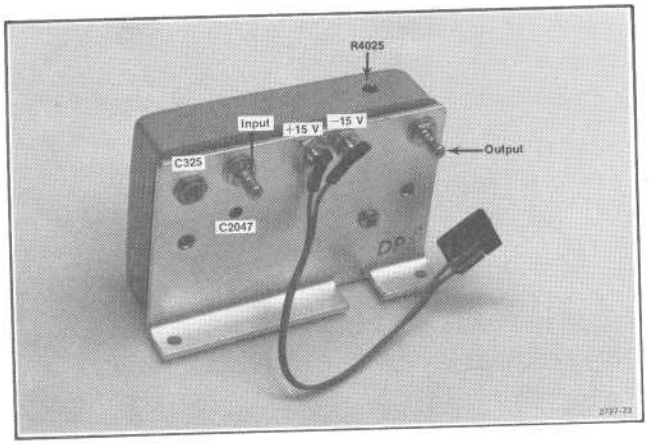


Fig. 4-10. Location of the 110 MHz IF return loss adjustments and IF Gain adjustment.

bandpass is 15 MHz down 1 dB, return loss is 20 dB or greater, and insertion loss is 1 dB.

If the seal is broken on any tuning slug, adjust for maximum return loss.

MIXER

To gain access to the Bias adjustments, remove the assembly from its mounting; then remove the mounting plate on the bottom of the assembly. Reconnect the Mixer to the input/output lines, using the same cables (cable length of semi-rigid cables is critical). Apply the CAL OUT signal to the RF INPUT and tune a marker to center screen. Simultaneously adjust both bias potentiometers for maximum signal amplitude.

110 MHz THREE CAVITY FILTER

Alignment is not a normal calibration adjustment. The tuning slugs are adjusted for center frequency and response shape so the resolution bandwidth is within specifications. The adjustment procedure follows.

1. With the CAL OUT signal applied to the RF INPUT, tune the signal to center screen and reduce the RESOLUTION BANDWIDTH to 1 kHz.

2. Tune the signal to center screen to establish center frequency reference; then increase the RESOLUTION BANDWIDTH to 1 MHz.

3. Adjust the tuning slugs for best response shape, centered around the reference. Ensure bandwidth (6 dB down) is 1 MHz.

4. Check resolution bandwidth accuracy over the range of the RESOLUTION BANDWIDTH selector to ensure that bandwidth is within specification.

Zero-hertz Response Adjustment

This adjustment is required only after replacing the 1st Mixer assembly A12, Mixer Diode assembly A12A1, or the 50 Ω load AT133.

a. Set the front panel controls as follows:

FREQUENCY	0
FREQ SPAN/DIV	200 kHz
RESOLUTION BANDWIDTH	100 kHz
Vertical Display	10 dB/DIV
Digital Storage	VIEW A
RF ATTEN dB	0
MIN NOISE	On
Triggering	FREE RUN
TIME/DIV	AUTO

b. Terminate the RF INPUT with a 50 ohm termination (BNC-to-N adapter and BNC 50 ohm terminator). Turn the 496/496P over to gain access to the RF deck. Remove the protective cover from the end of the Var Load assembly (see Fig. 10A) and center the start spur potentiometer.

c. Adjust the FREQUENCY to center the zero hertz response on screen.

d. Insert a small "jewelers" screwdriver into the access hole, on the diode assembly for the 1st mixer, and adjust for minimum amplitude of the zero-hertz response.

CAUTION

Use extreme care when adjusting the screw clockwise so as not to crack the internal diode substrate due to excessive torque. The end of the range is easily recognized when the screw bottoms out.

e. Re-adjust the Start Spur potentiometer in the Var Load assembly (see Fig. 10A) for a −30 dBm amplitude peak of the zero-hertz response.

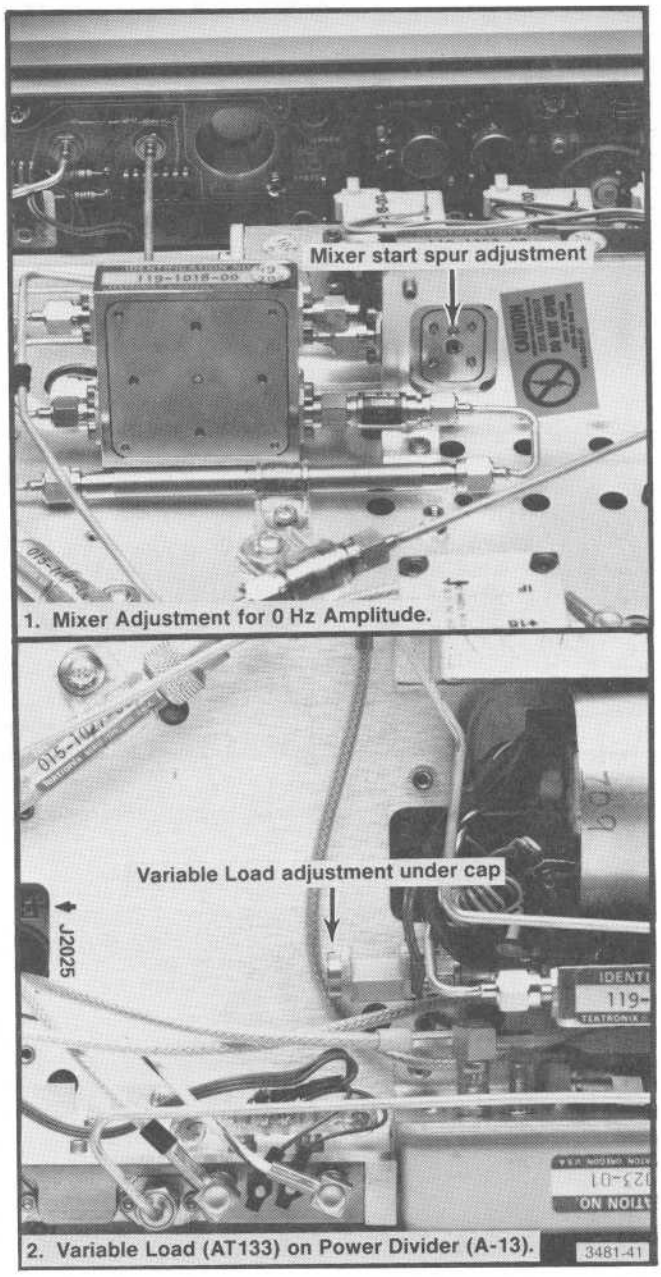


Fig. 10A. Adjustment locations for start spur amplitude.

f. Replace the protective cover over the adjustment for the Var Load assembly.

1st LO Phaselock Calibration

The phaselock assembly normally requires calibration only after some part of the assembly has been repaired or replaced. Phase noise, produced by the phaselock loop, is specified for −70 dBc or better 3 kHz out from the response. This should be checked before calibrating the assembly. The equipment required for 1st LO phaselock calibration is shown in Table 4-3.

1. Test equipment setup is shown in Fig. 4-11. Remove the Phaselock module and the two cover plates so all circuit test points and adjustments are accessible. Plug the assembly on extendor boards and into the instrument. Use extender cables and adapters to reconnect signal cables to their respective connector (cable with yellow band to J501, cable with black band to J502, and cable between J500 and J511 on Phaselock Control board).

Table 4-3

EQUIPMENT REQUIRED FOR 1ST LO PHASELOCK CALIBRATION

Test Equipment	Characteristics	Recommended Type
Test Oscilloscope	Vertical sensitivity, 50 mV/Div to 5 V/Div	Any TEKTRONIX 7000-Series or 400-Series oscilloscope
Digital Frequency Counter	10 Hz to 1 GHz, 20 mV rms Sensitivity	TEKTRONIX DC 508A Digital Counter
Service Kit	Extender boards and extension cables	Tektronix Part No. 006-3286-00

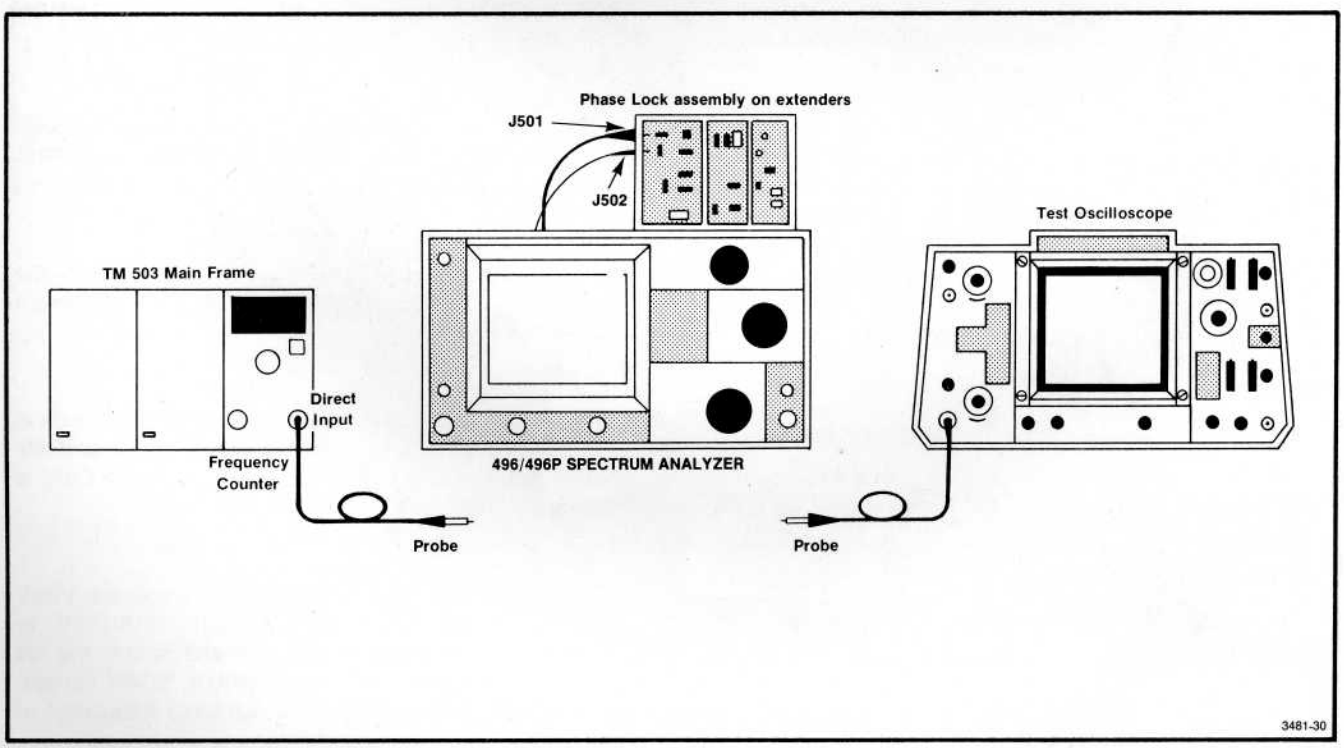


Fig. 4-11. Test equipment setup for calibrating the Phaselock assembly.

2. Switch the 496/496P POWER on, set the TIME/DIV to MNL, FREQ SPAN/DIV to 50 kHz, and Phaselock on.

3. Check Offset Mixer—This part of the procedure is only required after repair or replacement of the Mixer board.

a. Connect the Direct Input of a frequency counter to pin N (Fig. 4-12A) and adjust the counter controls for a count. Note the frequency.

b. Connect the counter to pin K and note the frequency.

c. Connect the counter to the collector of Q1040 and note the frequency. Frequence should equal the difference between pins N and R (e.g., 25.080 −25.00 = 80 kHz). Disconnect the counter probe from the collector of Q1040.

d. Connect the probe of a test oscilloscope to the collector of Q1040 and check for a 50% duty cycle.

4. Check Controlled Oscillator frequency—This part of the check is only required after repair or replacement of the Controlled Oscillator board.

a. Connect the Direct Input of the frequency counter to TP2011 (Fig. 4-12A). Ground pin L on the Offset Mixer board.

b. Connect an 80 kΩ variable resistor in seriese with a 2 kΩ variable potentiometer from pin H to ground; then adjust the variable resistor for a voltage reading of 12.0, ±0.1 V at pin H.

c. Adjust C1013 (Fig. 4-12A) for a freuency of 25.10 MHz.

d. Now replace the 80 kΩ resistor with a 4 kΩ resistor and adjust the variable resistor for a reading of 5.75, ±0.1 V at pin H.

e. Adjust C2011 (Fig. 4-12A) for a frequency of 25.032 MHz.

f. Repeat sub-parts c through e until the oscillator range is 25.100 to 25.032 MHz.

5. Error Amplifier Adjustment—This part of the procedure sets loop gain and error count break point. This part is required when either the Phaselock assembly, 1st LO, Phase Detector, or Error Amplifier is replaced.

a. Set the TIME/DIV to 1 s, PHASELOCK on, FREQUENCY SPAN/DIV to 50 kHz, and AUTO RESOLUTION on.

b. Pull P3057 (Fig. 4-12B); this turns the strobe to the Phase Gate on. Turn Loop Gain R3082 fully counterclockwise. Pull and install P2035 between pins 2 and 3.

c. Connect the test oscilloscope probe to TP3081 and trigger the test oscilloscope on the signal at TP2037 (U2048-6), both shown in Fig. 4-12B. Set the Time/Div to 5 ms and Volts/Div to 0.5 V. Note the beat notes. Beat notes are produced by the difference between strobes from the phaselock (one every 5 MHz) and the particular frequency the 1st LO is tuned to.

d. Turn Loop Gain R3082 clockwise slowly and note the amplitude of the beat notes prior to lock. This usually occurs between 0.5 V and 1.5 V peak to peak. The beat notes will disappear when lock occurs.

e. Turn Loop Gain R3082 fully clockwise, increase FREQ SPAN/DIV to MAX, set RESOLUTION BANDWIDTH to 100 Hz, and TIME/DIV to AUTO.

f. As the sweep scans across the span note the position of the smallest beat note. Tune the center FREQUENCY to position the frequency dot at this location.

g. Reduce the FREQ SPAN/DIV to 100 MHz. Set TIME/DIV to 1 s and activate VIEW A if the instrument has Digital Storage.

h. Adjust Loop Gain until the beat note amplitude is 1.5 times the amplitude noted in part 4 of this step. If this doese not occur, it is an indication the Phase Gate is defective.

i. Change the TIME/DIV to MNL, deactivate VIEW A/VIEW B, reduce the FREQUENCY SPAN/DIV to 50 kHz, then increase to 100 kHz and center the crt beam on the screen with the MANAUL SCAN control. Now adjust FREQUENCY for a null (zero frequency) of the display on the test oscilloscope.

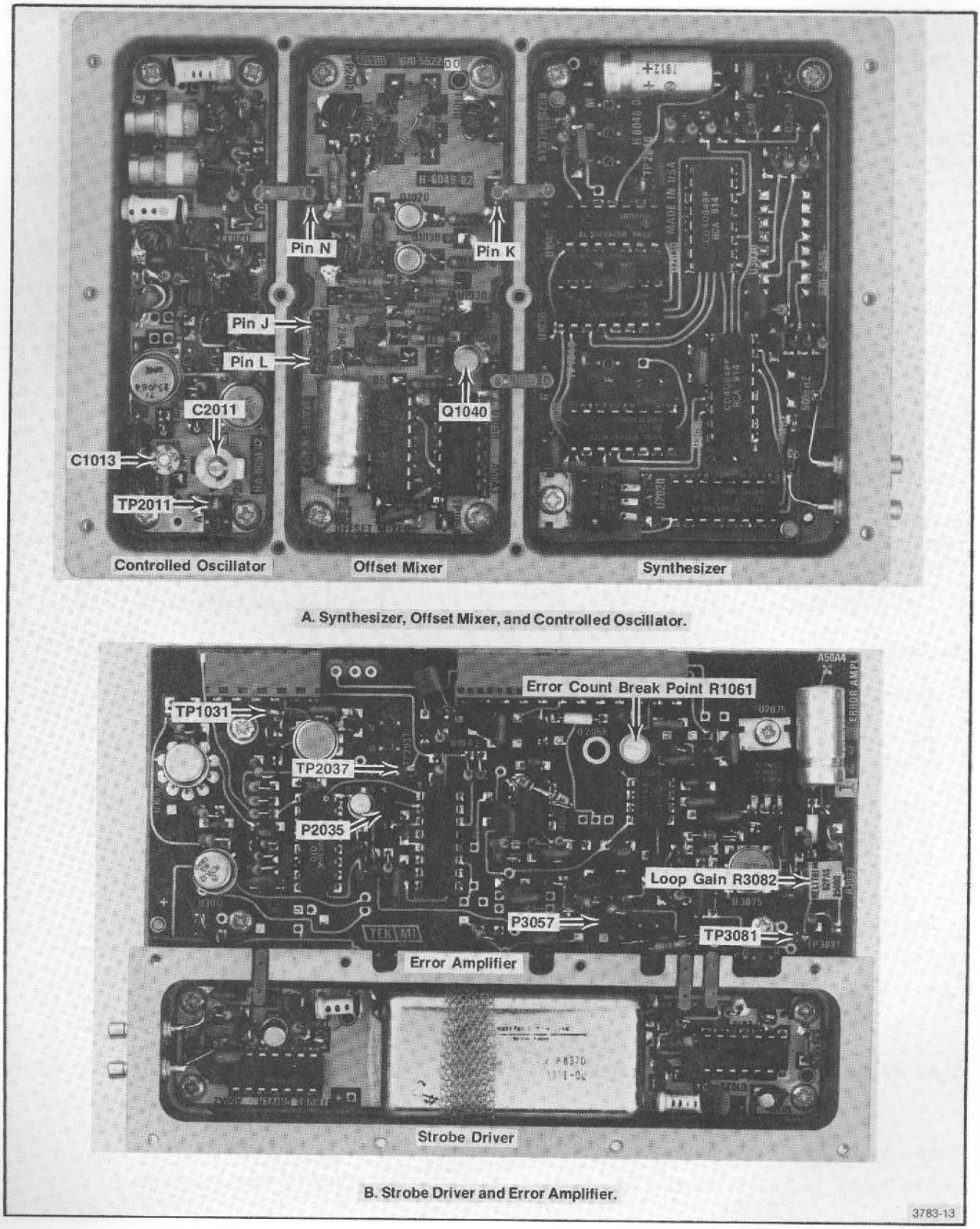


Fig. 4-12. Adjustments and test point locations within the Phaselock assembly.

j. Adjust MANUAL SCAN to position the crt beam four divisions from the center screen reference (four divisions represents 400 kHz).

k. Monitor and trigger the test oscilloscope on TP1031 at the top of R1038 (Fig. 4-12B) and adjust the Error Count Breakpoint potentiometer R1061, from its mid-range position, clockwise until the display just starts to break up.

l. Move the crt beam four divisions to the other side of center with the MANUAL SCAN control and note that the square wave response again starts to break up 400 kHz from center. As the beam crosses center, the display on the test oscilloscope should go through a null. If a null is not found, readjust center frequency. Adjust R1061, if necessary, so break points are 400 kHz either side of the null at center screen.

m. Reconnect P2035 between pins 1 and 2 and install P3057. Disconnect the test oscilloscope trigger and probe connections. Insure that P2035 and P3057 are installed correctly; their absence will produce spurious responses on the display.

n. Reduce FREQ SPAN/DIV to 50 kHz and ensure phaselock occurs.

o. Replace the covers on the assembly and reinstall the module in the 496/496P.

p. Perform the phaselock noise check as described in the Performance Check part.

2nd LO Calibration

The 2nd LO assembly normally requires calibration only after some part of the assembly has been repaired or replaced. This procedure has been divided into two parts: the LO section and the phaselock section. The LO section describes the calibration procedure for the three boards (2182 MHz Microstrip Oscillator, 2200 MHz Reference Mixer, and 2200 MHz Reference) within the machined aluminum housing. The phaselock section describes the calibration procedure for the 16–20 MHz Phaselock board within the mu-metal housing. Equipment required for calibrating the LO section is listed in Table 4-4, and equipment for calibrating the phaselock section is listed in Table 4-5.

Oscillator Section

NOTE

The 2nd LO assembly must be removed to gain access to the oscillator section.

Table 4-4

EQUIPMENT REQUIRED FOR 2nd LO CALIBRATION

Test Equipment	Characteristics	Recommended Type
Spectrum Analyzer	Frequency Range to 2.5 GHz	TEKTRONIX 496, 496P, or 7L13 MOD 139U
Signal Generator	Calibrated 100 MHz with spectral purity ±60 dB below fundamental Frequency within ±2.0 kHz	Hewlett-Packard Model 8640 A/B
Digital Voltmeter	Floating Input, measures to 0.01 V VDC Impedance ≥1 MΩ	TEKTRONIX TM 500-Series DM 501A, DM 502A, or DM 505
Terminators (2)	50 Ω 3mm connector	Tektronix Part No. 011-0049-01
Variable Power Supply	0 to −12.5 volts, accurate to 0.1 V	TEKTRONIX TM 500-Series PS 501-1

1. Check the Oscillator Frequency.

a. Test equipment set-up is shown in Fig. 4-13. Turn the 496/496P upside down and remove the semi-rigid connectors from the 2nd LO assembly. Remove the flexible cable from the 100 MHz input. Unscrew the 14 screws and remove the sheet metal cover.

b. Unsolder the jumpers to feedthrough capacitors C2203, C2204. These are the center two feedthroughs out of five which rise through the circuit board. Replace the lid and screw it down with a few of the 14 screws that were removed. Be very careful not to strip these screws. Save the remaining screws.

c. Remove the 2nd LO assembly from the 496/496P, taking care to keep the power supply connections intact. Turn the 2nd LO assembly upside down, so the machined aluminum housing is facing upward. Remove the lid from this housing, exposing the three RF boards within. Keep the 26 screws in a safe place.

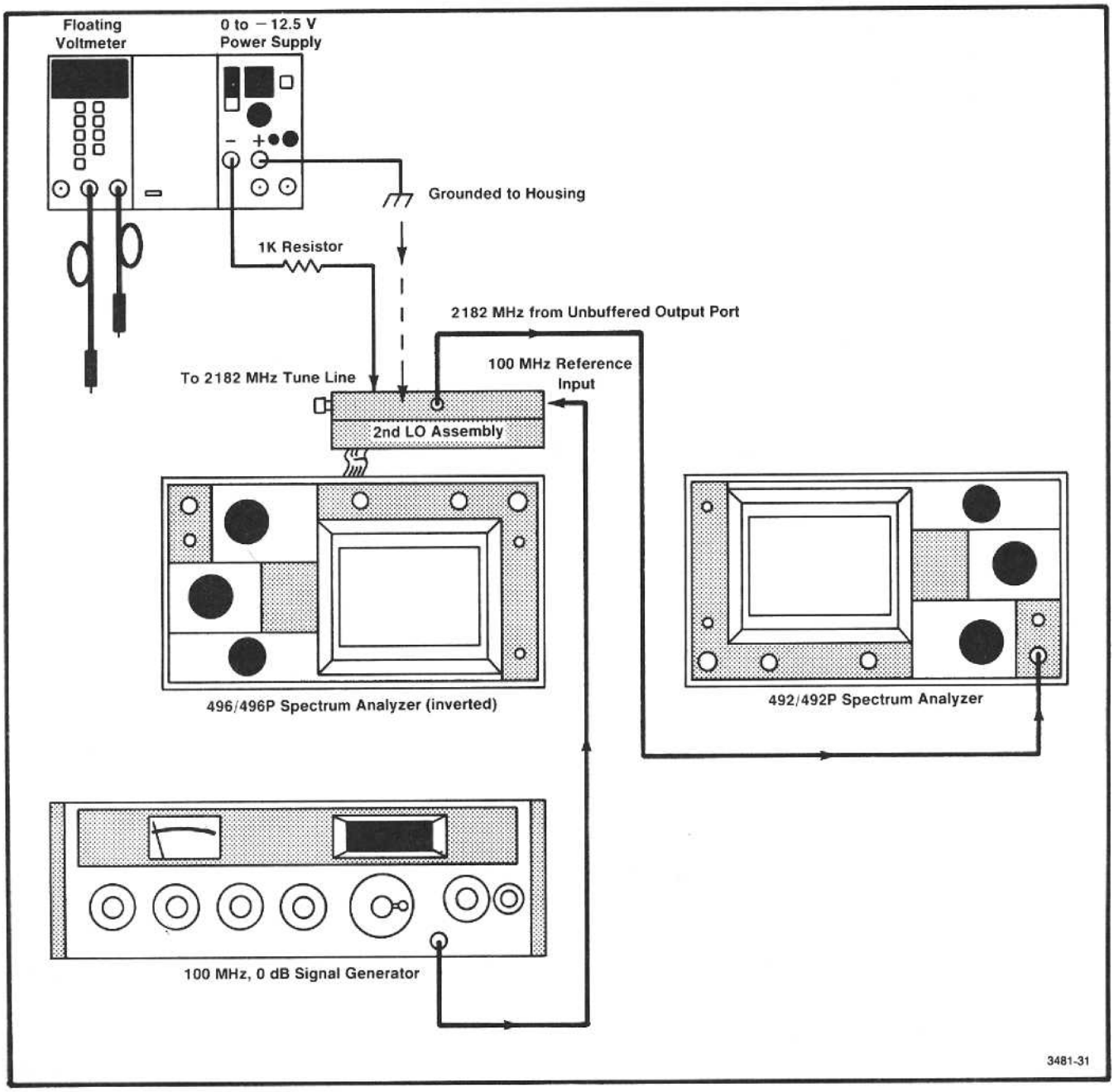


Fig. 4-13. Test equipment setup for calibrating oscillator section of the 2nd LO.

d. Refer to Fig. 4-14. Connect a 50 termination to the 2182 MHz buffered output port. Set the variable supply to 0 volts. Connect the + terminal of the supply to the 2nd LO housing; connect the − terminal to the exposed end of C2203 and L2031 through a 1 kΩ resistor. Connect the 100 MHz 0 dBm signal from the signal generator to the 100 MHz Reference Input port. Set the signal generator within ±20 kHz of 100 MHz.

e. Refer to Fig. 4-13. Connect the second analyzer to the 2182 unbuffered output port of the 2nd LO assembly. Set this analyzer for a center frequency of 2182 MHz, a Span/Div of 20 MHz, and a Reference Level of −10 dBm. Make sure that no cables are draped over the oscillator compartment; these may affect tuning.

f. Turn on the 496/496P. Refer to Fig. 4-14 for component locations on the 2182 MHz Microstrip Oscillator board. Bend tabs C and D (the feedback and frequency adjusting tabs) over the resonator so they are angled about 30° away from the board surface. Use your finger to bend the tabs. Turn on the variable supply and set it to 5.0 volts; there should be −5.0 volts on C2203.

g. A signal should appear on the second analyzer screen below 2182 MHz. Check the oscillator collector supply. There should be +10.0 volts ±0.7 volts across C2023. Measure the voltage at the free end of R1015 (Vbe test point). If the Vbe is greater than +0.5 volts, push the feedback adjustment tab to reduce the Vbe. If Vbe is less than −0.3 volts, lift the feedback adjustment tab. If Vbe is greater than +0.8 volts, replace the 2182 MHz Microstrip Oscillator board. If Vbe is less than −1 volt, check the bias circuitry.

h. Bend the feedback tab until there is +0.15 volts (±0.05 volts) at the Vbe test point. The Vbe test point voltage will go negative as the tab is depressed. Do not touch the tabs while measuring Vbe.

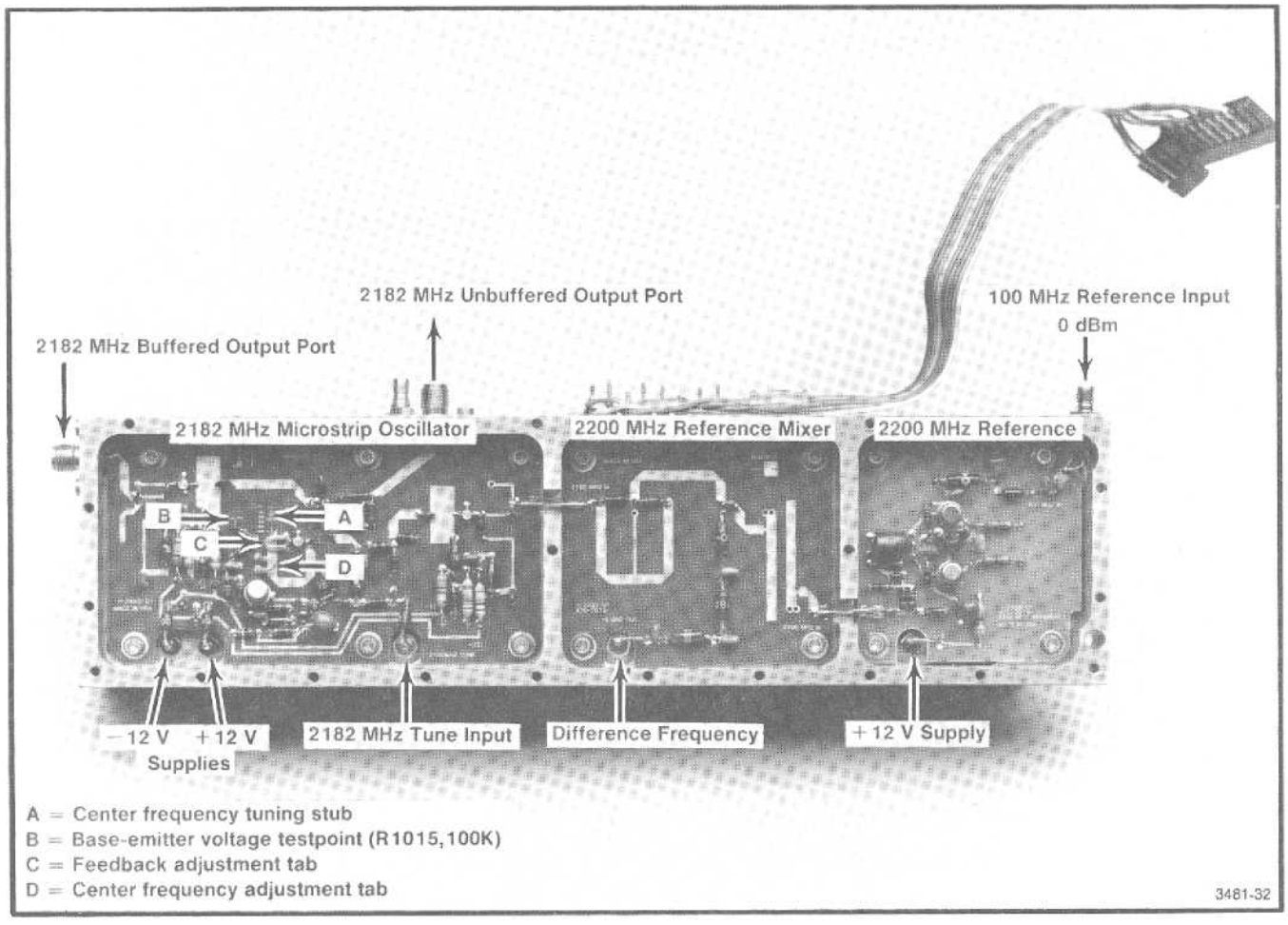


Fig. 4-14. Adjustments and test point locations within the oscillator section.

i. Bend the frequency adjusting tab until the oscillator frequency is 2182 MHz (±5 MHz). Do not touch the tabs while measuring frequency. Repeat steps "h" and "i" if the Vbe test point is no longer at +0.15 volts (±0.05 volts).

j. If there is the adjustment range is inadequate, replace the 2182 MHz Microstrip Oscillator board.

2. Measure the Output Power at 2182 MHz.

a. Before starting measurements, confirm that unused oscillator ports are terminated. Unterminated ports will degrade the accuracy of frequency adjustments and power measurements.

b. Power from the unbuffered output port should be −13 dBm ±3 dB. Power from the buffered output port should be +10 dBm ±3 dB. For troubleshooting, take note that a buffer on the 2182 MHz Microstrip Oscillator board feeds LO power to 2200 MHz Reference Mixer board at a nominal level of +8 dBm ±3 dB.

3. Test the Frequency Reference Circuitry.

a. Connect the second analyzer to the 100 pF feedthrough (C2204) that enters the Reference Mixer compartment through the floor of the housing. Use a short length of semi-rigid coax with a dc block as a probe; ground the probe by resting the outer shield against the 2nd LO housing. Confirm that a signal is present at 18 MHz, ±5 MHz. Carefully adjust the frequency tab on the 2182 Microstrip Oscillator board so this 18 MHz signal is within the ±1 MHz tolerance.

b. The nominal amplitude of the 18 MHz signal shouldbe −36 dBm. If it is less than −46 dBm, check the 2200 Reference Mixer board for sufficient power from the 2182 MHz Microstrip Oscillator (+10 dBm, ±3 dB) and the 2200 MHz Reference Mixer (−28 dBm, ±8 dB). Check the 100 pF feedthrough to see if it is shorted. If the 2200 MHz Reference Mixer is not providing enough 2.2 GHz power, check for +12 volts on the power supply feedthrough for this board. This board should have +10 volts on the junction of R2018 and C2021. Check for +4 volts on the bases of Q1024 and Q2024. Check the ground connections to the snap diode, CR2014, and the secondary winding of T2015. Confirm that the 2182 MHz Microstrip Oscillator and 2200 MHz Reference Mixer are operating at the correct frequencies.

4. Check the Tune Range.

Confirm that the Difference Frequency from the 2200 MHz Reference Mixer board (at C2204) is close to 18 MHz. Vary the adjustable supply connected to the 2182 MHz TUNE voltage line (C2203) over a 0 to −12.5 volt range. Note the total frequency change at C2204. There should be 25 MHz (+10, −5 MHz) shift in frequency. If there is no frequency shift, check the control signal path to the tuning varactor, CR1028.

5. Reassembly.

a. When the adjustments are complete and the performance verified, remove the connections from the variable power supply. Secure the housing lid with the 26 screws. Install the screws loosely and then tighten them, starting at the center of the lid and working towards the two edges of the lid. If the screws are not tightened in the proper sequence, hairline cracks will result between the housing and the lid, causing undesirable microwave leakage within the 496/496P.

b. Reinstall the 2nd LO assembly inside the RF deck of the 496/496P. Remove the 50 Ω terminators and reconnect the semi-rigid cables, using a 5/16 inch open-end wrench. Tighten the connectors slightly more than finger tight. Re-connect the flexible 100 MHz cable.

c. Remove the sheet metal lid from the 2nd LO. Reconnect the wire jumpers on the 16–20 MHz Phaselock board to feedthroughs C2203 and C2204. Install the sheet metal lid with the original 14 screws. Tighten the screws by beginning at the lid center and working outwards (this will prevent a bulge in the lid). Do not overtighten; the screws are easily stripped.

Table 4-5

EQUIPMENT REQUIRED FOR 2nd LO PHASELOCK CALIBRATION

Test Equipment	Characteristics	Recommended Type
Digital Voltmeter	Flotaing Input, measures to 0.01 VDC	TEKTRONIX TM 500-Series DM 501A, DM 502A, or DM 505
Frequency Counter	Frequency Range to 80 MHz	TEKTRONIX TM 500-Series DC 503A, DC 504, DC 505A, DC 508A, or DC 509
Time Mark Generator	Marker output, 1 s to 1 μs; accuracy, 0.001%	TEKTRONIX TM 500-Series TG 501
Service Kit (Extender) Board		Tektronix Part No. 672-0865-00

1. Check Incoming Voltages.

a. Test equipment setup is shown in Fig. 4-15. The 2nd LO should be installed in the 496/496P. Remove the Center Frequency Control board and place it on an extender. Place the 496/496P on its side.

b. Turn on the power to all instruments. Check that the Phaselock light is off and proceed to measure the voltages at the feedthrough capacitors in the housing wall. Refer to Fig. 4-16 or the housing lid to identify the feedthroughs.

c. The incoming supply voltages should be +15 volts, −15 volts, and +9 volts.

d. The voltages appearing at the sweep and tune pins should be 0.0 volts ±0.05 volts. Make sure that the FREQ SPAN/DIV is set to 100 kHz/Div or more.

2. Setting Center Frequency.

a. This step adjusts the 16–20 MHz Phaselock board. To gain access to this board, remove the mu-metal lid of the 2nd LO assembly. Save the 14 screws in a secure place. Refer to Fig. 4-16 for component locations.

b. Measure the re-regulated supplies on the board. There should be +12 volts (±0.4 volts) at the cathode of CR2012, −12 volts (±0.4 volts) at the anode of CR2019, and +5.2 volts (±0.25 volts) at TP1019. Check the output of the shaper at TP1083; this should be 0.0 volts ±0.3 volts.

c. Connect the frequency counter to TP2035. Between a transformer and a choke (T2092 and T1091) are two rows of circuit board pads. The row of three is connected to T1091 and the row of two is connected to T2092. A jumper wire is used to connect one of T1091's three terminals to either terminal of T2092.

d. Replace the existing jumper with a 1 inch length of flexible wire; solder only the T2092 end of wire, leaving the T1091 end free (facing the rwo of three pads). Use a plastic tuning tool to press the wire in each of the three pads; if the frequency counter reads within ±500 kHz of 18 MHz, replace the wire with a new jumper of the right size to fit the appropriate pads.

CAUTION

If this flexible wire touches ground while the circuit is operating, the supply regulators will be damaged. The regulators are not protected against short circuits.

e. If the frequency is not close enough, unsolder the T2092 end of the wire and solder it to the other T2092 pad. Press the free end to each of T1091's three pads; one of these pads should cause the frequency counter to read within 500 kHz of 18 MHz. Replace the wire with a new jumper of the right size to fit the appropriate pads.

3. Setting Sweep and Tune Sensitivity.

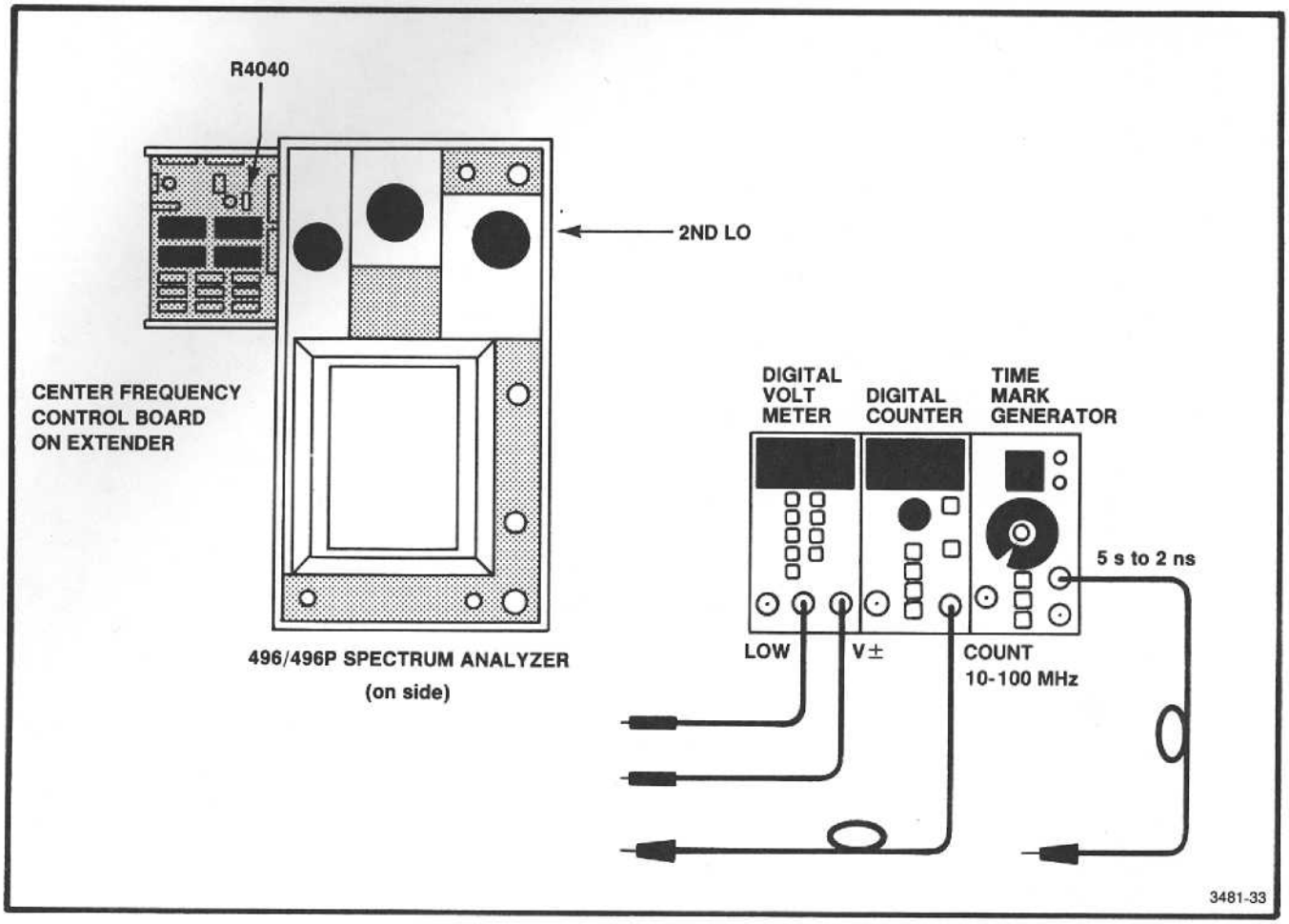


Fig. 4-15. Test equipment setup for calibrating the phaselock section of the 2nd LO.

a. Center the Fine Tune Range adjustment (R4040) on the Center Frequency Control board and the 2nd LO Sweep adjustment (R1067) on the Span Attenuator board. Refer to Fig. 4-17 for these locations.

b. Connect the time mark generator to the RF INPUT of the 496/496P. Set the Marker control on the generator to 5 μsec (this produces 200 kHz comb lines).

c. Set the 496/496P front-panel controls as follows:

FREQUENCY	5 MHz
FREQ SPAN/DIV	100 kHz
RESOLUTION BANDWIDTH	10 kHz
TIME/DIV	AUTO
Vertical Display	10dB/Div

d. Adjust the REF LEVEL to produce a full screen display of the comb lines. Set the Vertical Display to 2 dB/Div. Adjust the FREQUENCY to place a comb line within one minor division of center screen. Reset the FREQ SPAN/DIV to 50 kHz/Div; the phaselock light should be on.

e. The 2nd LO is now in the center of its tune range. Decrease the FREQUENCY by 1.4 MHz (7 comb lines) and line up the nearest comb line at center screen.

f. Press Δ Frequency. Increase FREQUENCY by exactly 14 comb lines. If the Δ Frequency readout display is 2910 kHz or greater, refer to Fig. 4-16, then replace two resistors on the circuit board. Replace R2072 with a 3.24 kΩ resistor and replace R2070 with a 2.8 kΩ resistor. If the readout is 2690 kHz or less, replace R2072 with a 2.8 kΩ resistor and R2070 witha 3.24 kΩ resistor. This step leaves the 2nd LO at the end of its tuning range.

g. Tune the 2nd LO downward over 3 MHz by counting 15 successive comb lines. Adjust the Fine Tune

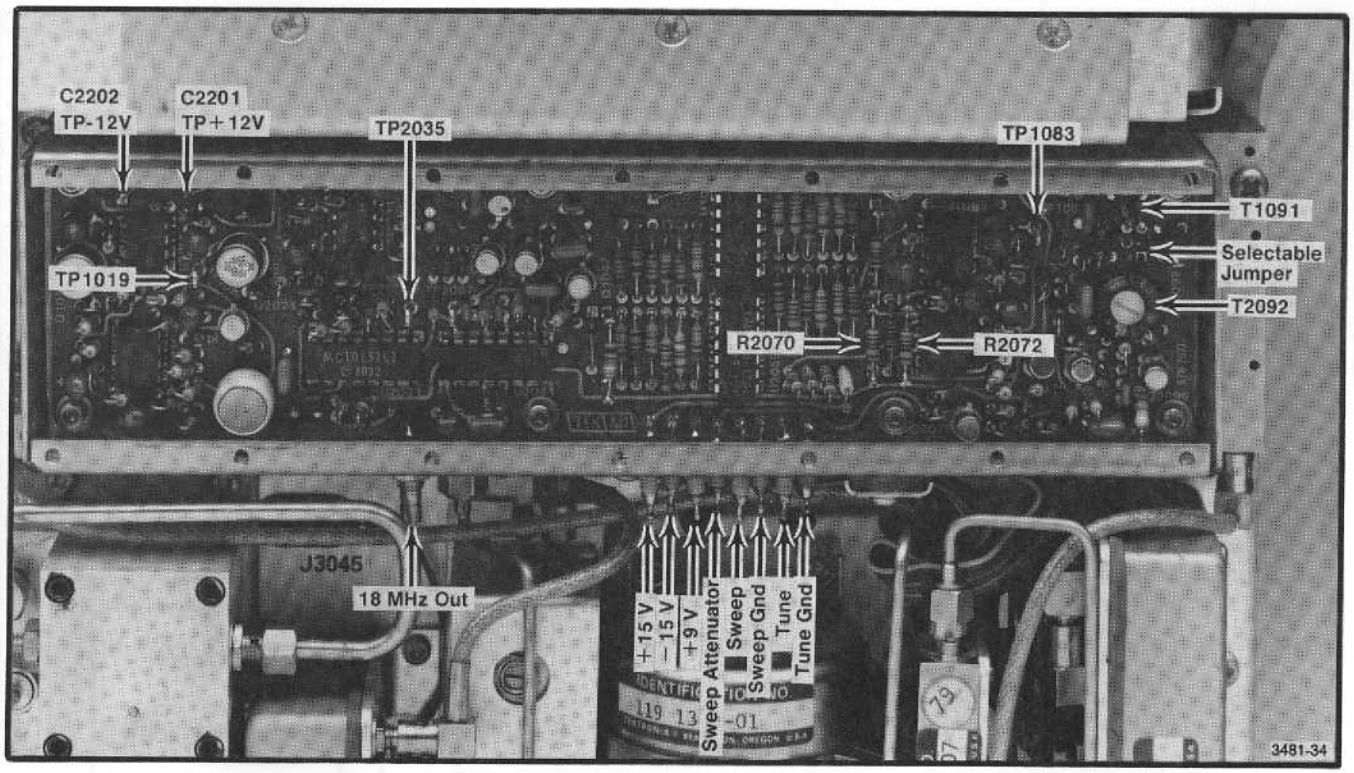


Fig. 4-16. Adjustments and test point locations on the 16–20 MHz phaselock board.

Range adjustment (R4040) on the Center Frequency Control board (Fig. 4-17) so that tuning the 496/496P over a 3 MHz range produces a Δ Frequency display of 3 MHz, ±20 kHz. Several successive tunings over this range will be necessary to reach the correct setting on the Fine Tune Range adjustment.

h. Set the FREQ SPAN/DIV to 100 kHz/Div, then back to 50 kHz/Div. This recenters the 2nd LO's tuning range. Tune the 496/496P to place a comb line on the center of the screen. Adjust the 2nd LO Sweep adjustment (R1067) on the Span Attenuator board (Fig. 4-17) so that the comb lines on opposite sides of the screen are exactly 8 major divisions apart.

4. Adjusting the Tune Linearity.

a. Set the Sweep and Tune sensitivity as described in part 3.

b. Connect the time mark generator to the RF INPUT of the 496/496P. Set the Marker control on the generator to 5 μsec (this produces 200 kHz comb lines).

c. Set the 496/496P front-panel controls as follows:

FREQUENCY	10 MHz
FREQ SPAN/DIV	50 kHz/Div
RESOLUTION BANDWIDTH	10 kHz
TIME/DIV	AUTO
Vertical Display	2 dB/Div

Adjust the REF LEVEL so the comb lines appear at the top of the screen. Check that the phaselock light is on.

d. Reduce the FREQUENCY until the 496/496P stops tuning. Tune upwards until a comb line falls exactly one major division from the left edge of the screen. A comb line should appear at, or very near, one major division from the right edge of the screen.

e. If the right-hand comb line is not exactly one major division from the right edge of the screen, note the error in units of minor division (for example, −1.5 minor divisions error may be noted).

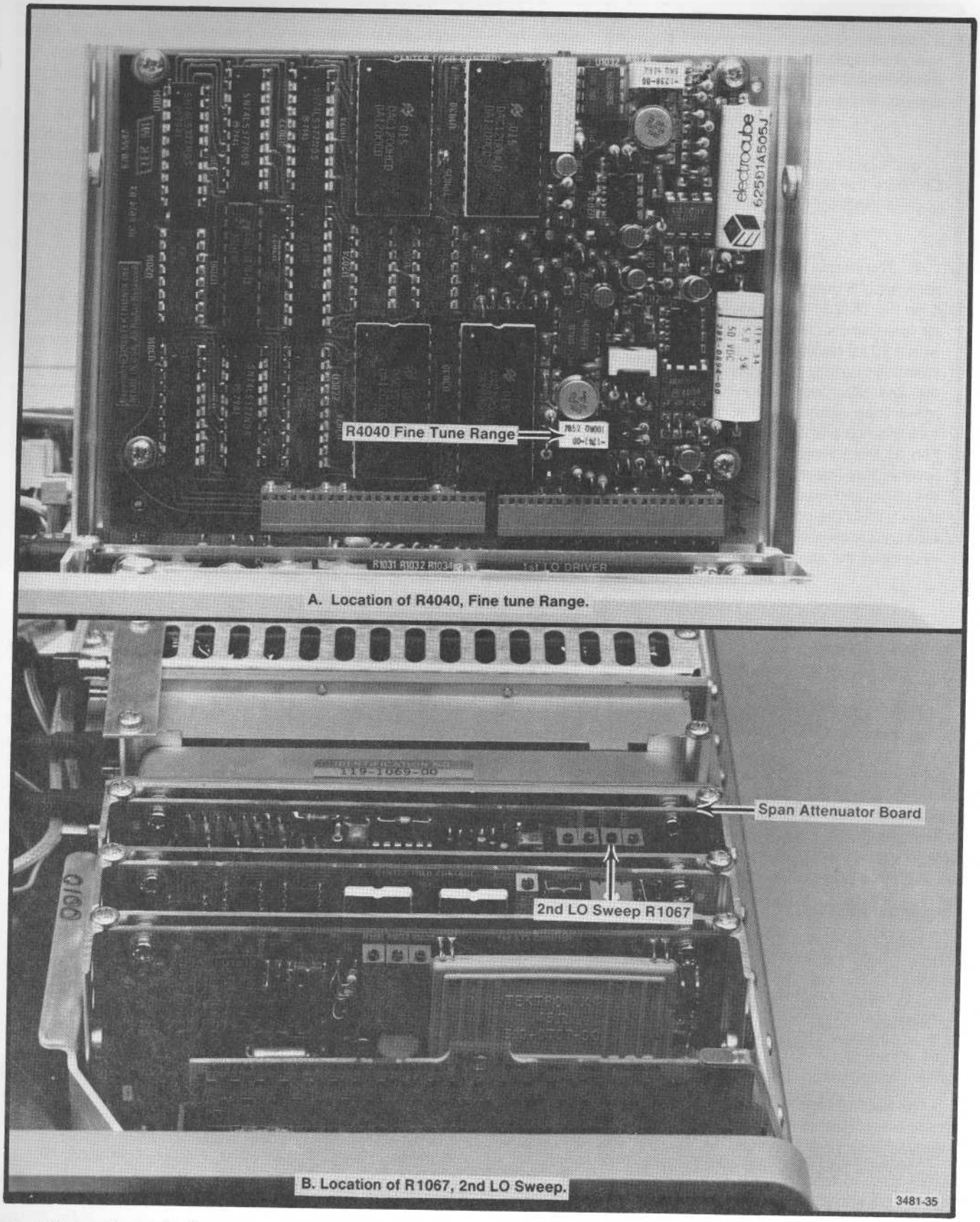


Fig. 4-17. Location of the fine tune range pot (R4040) on the center frequency control board and the sweep gain pot (R1067) on the span attenuator board.

f. Increase FREQUENCY until this comb line is exactly one major division from the LEFT edge of the screen. A new comb line should appear at, or very near, one major division from the right edge of the screen. Note the amount and direction of the error as before.

g. Repeat part f until the 496/496P stops tuning. Compare the 16 error measurements and find the peak-to-peak range of the errors.

h. The shaper circuit needs adjustment if the peak-to-peak error is greater than 2.5 minor divisions. This circuit is on the 16–20 MHz Phaselock board; refer to Fig. 4-16 for component locations. Temporarily replace R2049 with a 20 kΩ resistor. Adjust this test resistor to minimize variation in comb line spacing across the tuning range of the 2nd LO. Decreasing the resistance will bring the comb lines closer together in the upper portion of the tuning range and spread the comb lines in the lower portion of the tuning range. Increasing the resistance will reverse this effect. Comparing the comb line spacing in the upper and lower tuning limits will expedite this adjustment. When the correct setting is found, remove the test resistor, measure the resistance, and replace with a fixed resistor of the same value.

i. A shaper diode may be defective if the comb line spacing is consistent for part of the tuning range and 3 minor divisions off for the rest of the tuning range. To test the tuning diodes for forward conduction, tune the 496/496P to the low end of the 2nd LO tune range and short R2049. (Refer to Fig. 4-16.) Pin 1 of U1073A, the output of the first shaper amplifier, should be approximately +3 volts. U1059 diodes B through G and U2059 diodes A through F should all have a 0.48 volt forward drop. A floating or differential voltmeter should be used since the diodes are not at ground potential.

j. Replace the sheet metal cover using the 14 screws supplied. Start tightening from the center outward to avoid bulges in the lid. Do not overtighten the screws; they will strip easily.

k. The Tune Linearity procedure completes the 16–20 MHz Phaselock calibration. Refer to Calibration, Section 3, Adjustment Procedures, and perform steps 5 and 6 "Calibrate the 1st LO System and Center Frequency Control" and "Check/Adjust 2nd LO Tuning Range" to recalibrate the 496/496P.

MICROCOMPUTER SYSTEM MAINTENANCE

Several maintenance aids are built into the microcomputer system. These are microcomputer operating modes that demonsrate correct performance or indicate the location of a problem, if any.

Switches that set up two of these test modes are described first, followed by instructions for the three test modes. In the first mode, the microcomputer executes a self-test that verifies, in so far as possible, correct operation. RAM, ROM, and interface adapters are checked; any failure found is indicated.

The second mode hardwires the microcprocessor to execute an instruction that toggles the address bus; this mode requires less of the system to run, so may be used to troubleshoot problems that disable the first mode.

The third mode gets at communication between the microcomputer and the rest of the instrument. The microcomputer exercises the instrument bus to help isolate problems that do not show up in the first mode, but prevent normal instrument operation because of a breakdown in communication.

Some notes on operation of several versions of instrument firmware conclude the discussion of microcomputer system maintenance.

Memory Board Option Switch

S1033 on the Memory board informs the microcomputer whether to configure itself at power-up for several test modes, and for instrument modifications. Figure 4-18 shows the correct setting of the individual switches in S1033.

The microcomputer reads these switches only at power-up. For a change in a switch position to take effect, the instrument must be powered-up after the switch is changed.

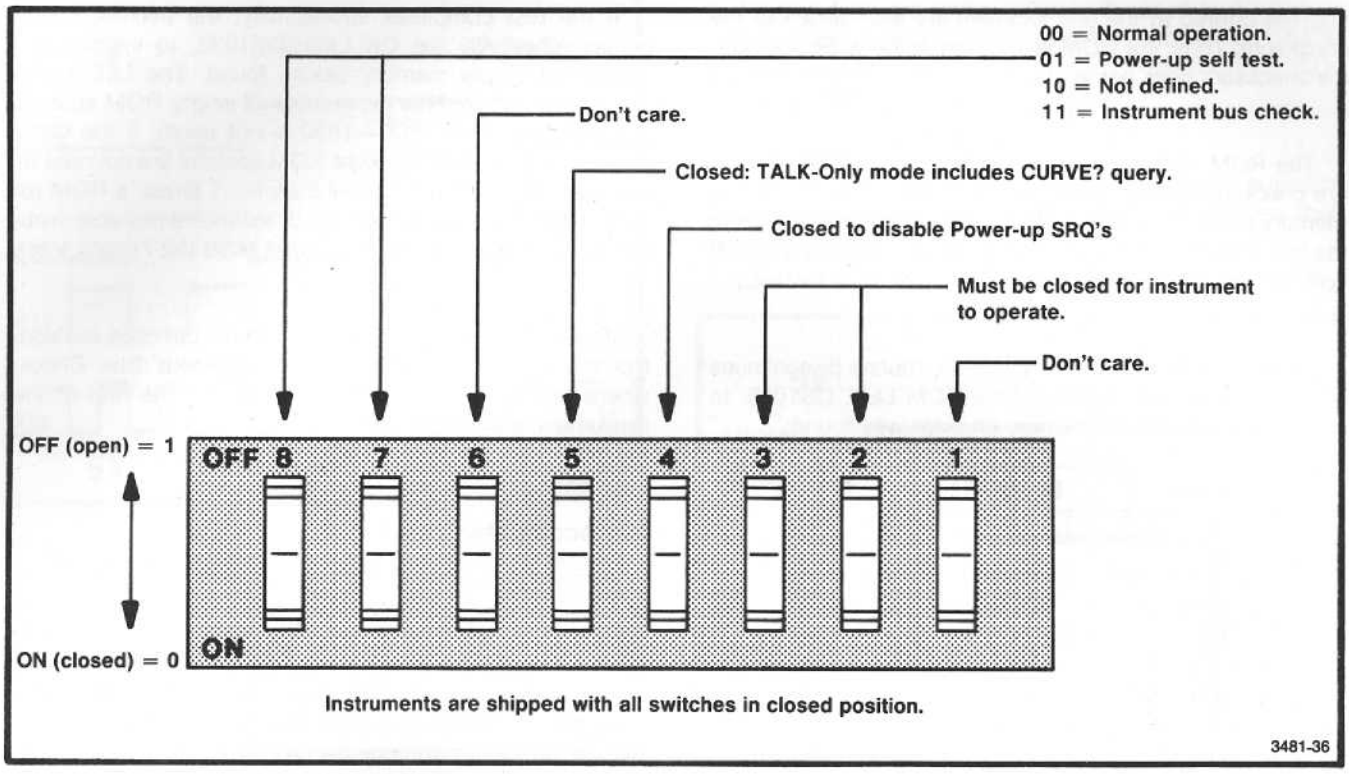


Fig. 4-18. The Memory board option switch band S1033.

Power-Up Self-Test Mode

The microcomputer enters a self-test mode when the instrument is turned on if this mode is selected (Fig. 4-18). In this mode the instrument does not operate normally. The microcomputer performs the following steps, stopping the test to indicate the source of any problem found by blinking an LED on the Processor board.

Addresses are specified as hexadecimal numbers in this description.

Step 1. At power-up, the microcomputer vectors to the self-test in the ROM at the top of address space U2028 on the Memory board. The microcomputer first verifies the checksum of U2028. If the routine for this step runs, but does not obtain the correct checksum for the ROM, the routine halts and blinks the ROM 8 LED, DS1044.

This step uses only U2028 and no other memory; so if the test does not blink the LED and does not proceed to step 2, U2028 is probably the culprit. Consider first, however, that the correct ROM must be installed, both phases of the clock on the Processor board must be present, and the microcomputer system (exclusive of the instrument bus or GPIB) must be operating correctly. If in doubt about the 6800 microprocessor, its bus, or the microcomputer bus, skip to the instructions under Microcomputer Test Mode, to exercise the microcomputer in a more simple manner.

Step 2. The microcomputer next checks the condition of RAM. This step does not rely on the RAM being ok to execute. The procedure is: the microcomputer loads the bit pattern 01010101 into a RAM location, reads the location, and compares what is returned to what was stored. The microcomputer then repeats this test with the pattern 10101010.

The microcomputer attempts to test all RAM addresses. If it finds an error on the Memory board, it stops the test and pulses the RAM LED, DS1042—once for an error in U2035, twice for an error in U2032, and three times for an error in both RAM IC's; these IC's are on the Memory board. If the microcomputer finds an error on the GPIB board, it pulses the LED 7, 8, or 9 times in a similar manner for low RAM—U1046 and U1037—or 9, 10, or 11 times for high RAM—U1042 and U1032. The microcomputer continues to repeat the number of pulses after an error is found.

Step 3. The microcomputer proceeds to checksum all the ROMs. A checksum is stored in the header of each ROM. This is compared to a checksum formed by the successive 8-bit sum of each byte in the ROM starting at the fourth location in the ROM. The upper eight bits of the ROM's

address (stored at the first location) are also added to the checksum. Thus, if a ROM is installed in the wrong socket, it's checksum does not verify.

The ROM sockets, including those on the GPIB board, are checked starting at the lowest address (U1012 on the Memory board). The check starts by looking at the MSB in the first and fourth locations in the ROM's address range. If both bits are one, it is assumed that no ROM is installed.

When a defective ROM is found, the routine discontinues the test and pulses repeatedly the ROM LED, DS1038, to indicate the ROM socket where an error was found:

ROM Socket	Board	Pulses
U1012	Memory	1
U1017	Memory	2
U1023	Memory	3
U1028	Memory	4
U2012	GPIB	6
U2019	GPIB	7
U2025	GPIB	8
U2031	GPIB	9
U3012	GPIB	10
U3019	GPIB	11
U3025	GPIB	12
U3019	GPIB	13
U2012	Memory	14
U2017	Memory	15
U2023	Memory	16
U2028	Memory	17

If this step fails, it can be forced to continue checking ROMs; just turn power off and unplug the defective ROM, then turn power on to restart the self-test.

Step 4. The microcomputer checks part of the instrument bus PIA, U3016 on the Processor board. First the microcomputer writes to the A control register and then reads back from the register. Next it repeats these operations with the A data direction register. If either of these attempts fail, the routine stops and pulses the bus LED, DS1036.

Step 5. This step checks part of the GPIA, U2047 on the GPIB board (if installed). The microcomputer resets the GPIA and checks to see that the GPIA is not addressed to talk or listen. The GPIA is then set to listen-only mode and checked to see that it is addressed to listen. Then the GPIA is set to talk-only mode and checked to see that it is addressed to talk. If any part of this step fails, the test stops and pulses repeatedly the GPIB LED, DS1034.

If the test completes successfully, the microcomputer pulses repeatedly the OK LED, DS1032, to indicate the number of empty memory blocks found. The LED blinks N+1 times, where N is the number of empty ROM sockets (the memory block 1600—1800 is not used). If the GPIB board is not installed, its eight ROM sockets are counted as empty. If the LED blinks more than N+1 times, a ROM (or ROMs) failed to respond in Step 3; look for a possible problem on the chip-select line or on the MSB (bit 7) data line.

If the microcomputer seems to test ok, but does not control the instrument, skip to the Instrument Bus Check, where microcomputer communication with the rest of the instrument is exercised.

Microcomputer Test Mode

A microcomputer test mode is selected by moving jumper P1020 on the Processor board to the TEST position. This hardwires the 6800 data lines to hex 5F. As a result, the 6800 continuously executes a CLRB instruction, repetitively cycling through all of its address space. The instrument does not function in this mode. Rather it sets up a known pattern on the microcomputer address, data, and control lines and at the output of address decoders. This mode allows an attack on problems that prevent the microcomputer from running its self-test check.

NOTE

If CR2025 on the Processor board is missing, it may be added as shown on the Processor diagram to make the correct instruction on the data lines.

Microcomputer Bus. As the microcomputer cycles through its address space, it toggles the address lines. The MSB, A15, has a period of about 1540 ms; the period of A14 through A0 is divided by two from the line above down to the LSB, A0, with a period of about 4.7 μs. The four high-order lines, A15 through A12, are shown in Fig. 4-19. Ignore the narrow pulses that may be evident during the low portion of each cycle.

The data lines on the microprocessor side of U1013 on the Processor board are static; D7 and D5 are low, the others are high. In the TEST position, P1020 disables U1013. On the other side of this buffer, the data lines are being driven by the various memory devices on the bus as they are addressed.

Examining the data lines can locate shorted or open lines—lines inactive at high, low, or in-between states or

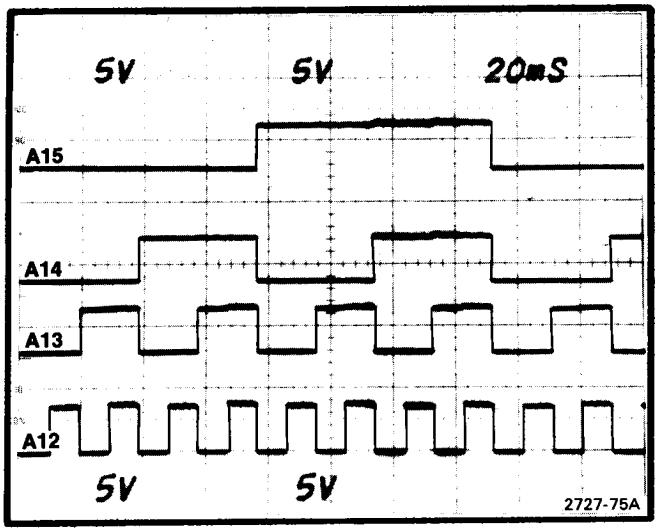


Fig. 4-19. A15 through A12 in microcomputer test mode.

changing in unison, usually to indeterminate logic levels of +1 to +2 V. A problem related to a particular device may be evident only while that device is addressed; compare a problem that occurs only during a portion of the A15 cycle to the address decoder outputs pictured below.

Processor Address Decoders. Address decoder U2044 on the Processor board sets its outputs low in turn to access block of memory space. See Fig. 4-20, where the Y0 through Y2 outputs are compared to A15. The other outputs follow in sequence with similar pulse widths. The self-test indicators connected to the decoder outputs blink in sequence as the microcomputer cycles through its address space.

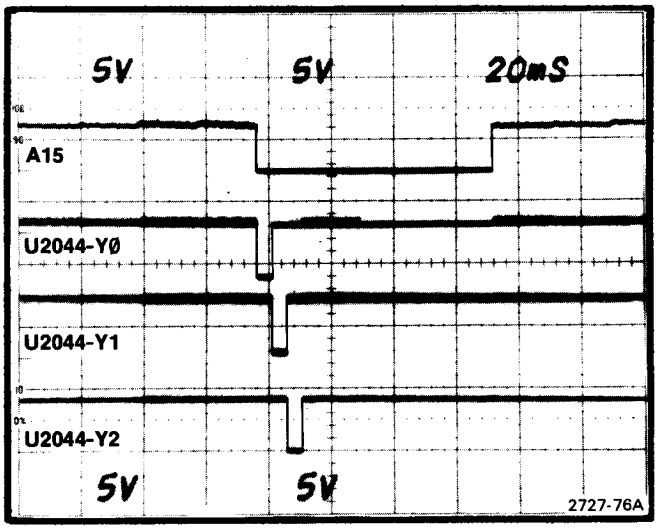


Fig. 4-20. A15 and Y0 through Y2 of address decoder U2044.

A portion of one address block, decoded by U2044, is further decoded by U1037B. Figure 4-21 shows the U1037B enable line on top and below it in order, Y0 through Y2. Y3 is similar in width and follows in sequence.

The narrow pulses evident during the time each output of U2044 and U1037B is asserted result from address lines toggling between microcomputer cycles.

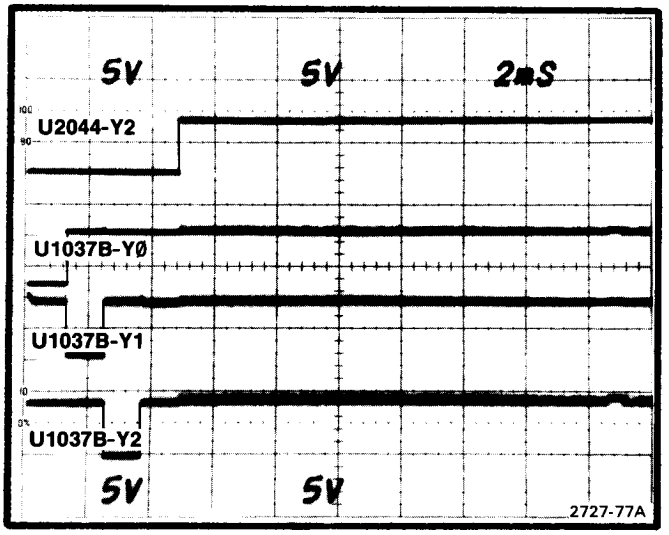


Fig. 4-21. Enable and Y0 through Y2 of address decoder U1037B.

Clocks and Control Lines. The 6800 clock lines are complementary, nonoverlapping square waves with periods of about 1.17 μs. VMA, RESET, NMI, and R/W should be high (logic one). IRQ may be either high or low, depending on how assemblies on the insrument bus powered up.

Memory Address Decoders. Address decoders U1036 and U1038 on the Memory board set their outputs low to access blocks of ROM addresses. These outputs are shown in relation to A15 in Fig. 4-22. The RAM (U2035 and U2032) chip-select lines and option switch register (U1033) enable line are also decoded on the Memory board as shown in part d of Fig. 4-22. The narrow pulses which may be evident during the time each output is asserted can be ignored for the reason noted above under Processor Address Decoders.

GPIB Board Address Decoders. Address decoder U1021 on the GPIB board sets its outputs low in sequence while the 496P is operating in the microcomputer test mode. Y0 through Y2 are shown in relation to A15 in Fig. 4-23. Although not shown, Y3 through Y7 are asserted in order with the same pulse width.

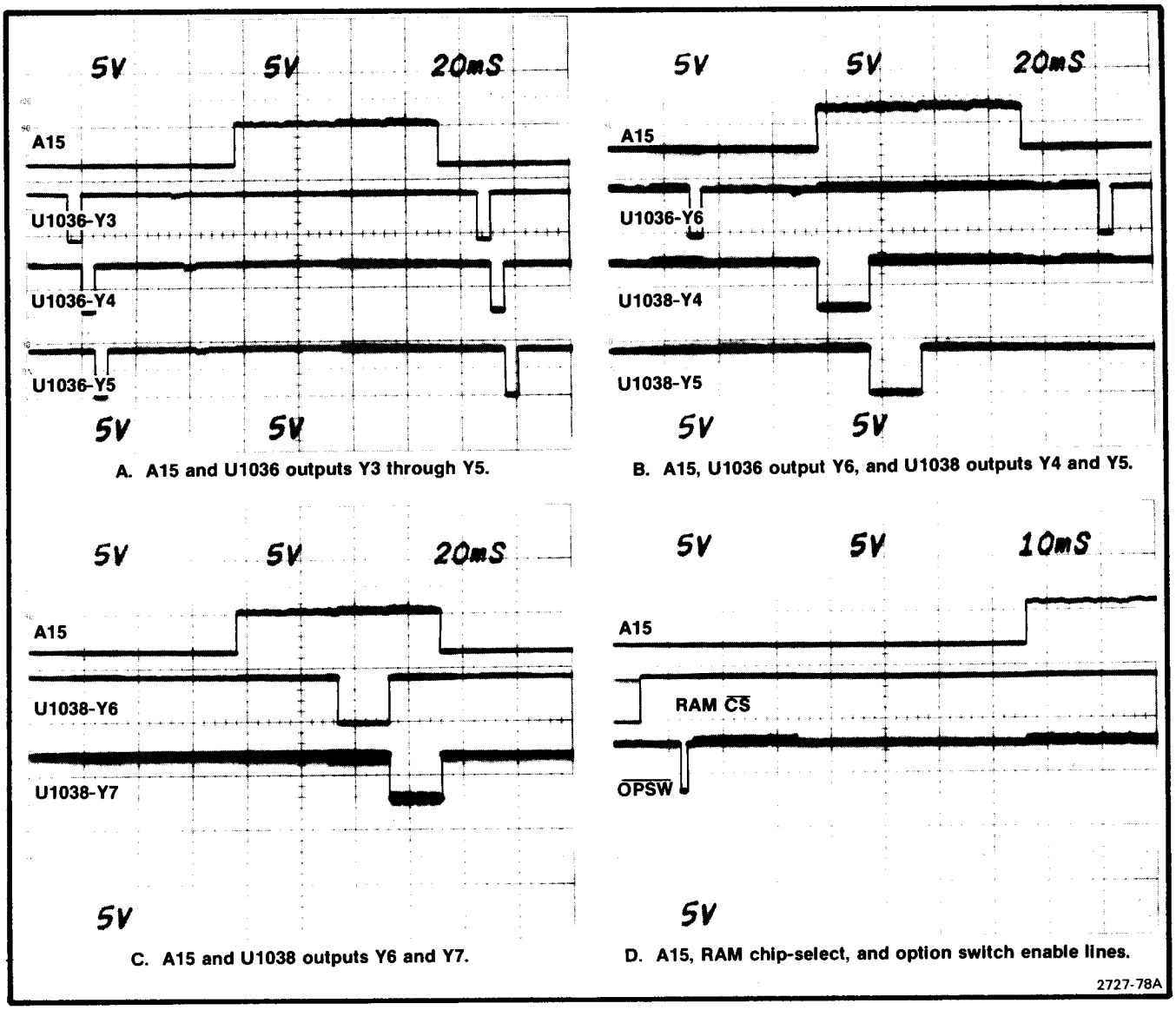


Fig. 4-22. A15 and Memory board address decoder outputs.

U1028 further decodes two address decoder signals from the Processor board. One enable and two output signals are shown in Fig. 4-24. The other output, ASR, is not shown, but looks the same as GPS: they appear to be asserted at the same time. These two signals can be compared for correct operation by speeding up the sweep and noting that they toggle in a complementary fashion during the time they appear to be low in the figure.

Instrument Bus Check Mode

If the microcomputer performs the power-up self-test, but fails to control the instrument properly, the instrument bus check may uncover the problem. The instrument bus check mode may be selected by setting the option switch as shown in Fig. 4-18. In this mode, the microcomputer continuously writes to the instrument bus to exercise it in a repetitive manner. Consequently, the instrument does not operate normally.

The pattern on the instrument bus toggles DATA VALID and POLL and exercises the address and data lines at separate times. The address lines change when DATA VALID is low and the data lines change when DATA VALID is high. There may be an exception on DB4 through DB0; these lines may continue to change after DATA VALID goes low if an assembly on the bus is requesting service because of the way it powered up. In this case, an assembly or assemblies may respond to the high state of POLL and the changing state of AB7 and attempt to report status.

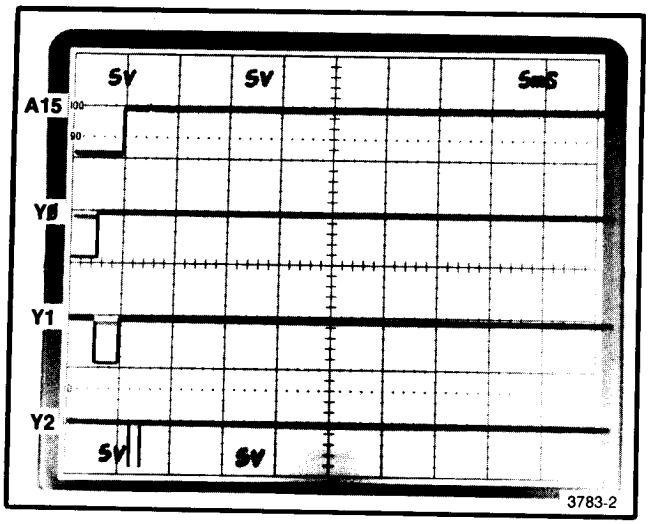


Fig. 4-23. A15 and Y0 through Y2 of address decoder U1028 on the GPIB board.

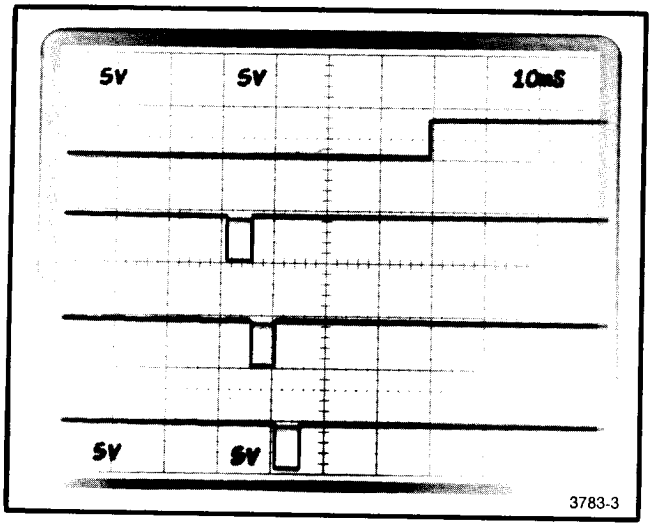


Fig. 4-24. One enable and outputs LORAM, HIRAM, and GPS of address decoder U1028 on the GPIB board.

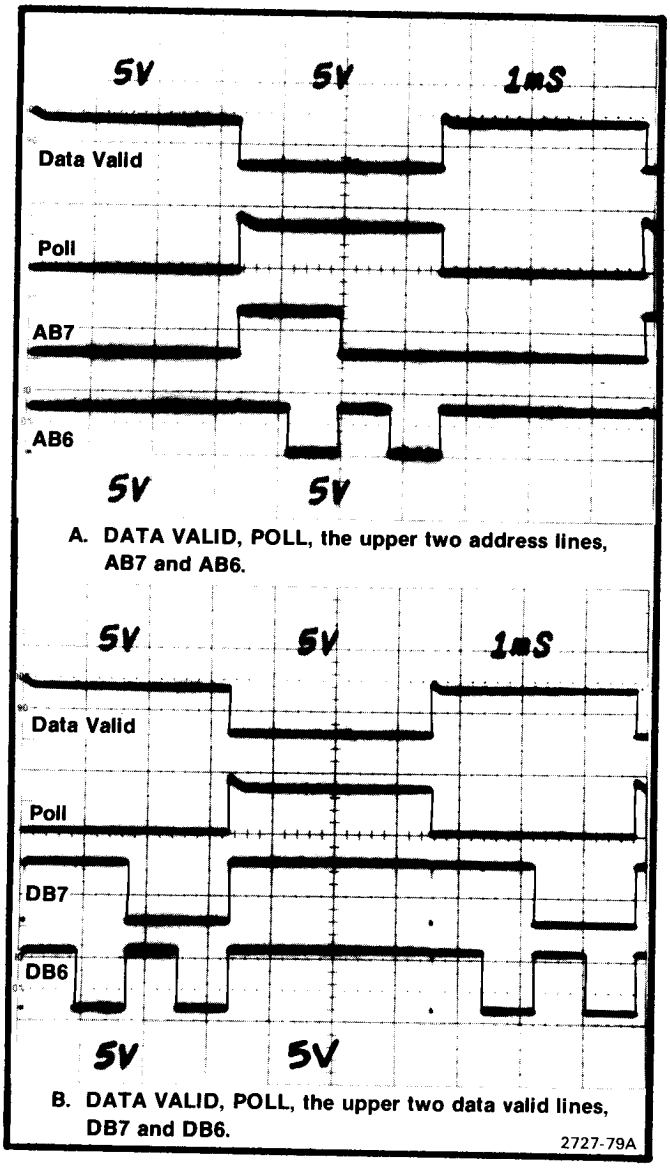


Fig. 4-25. Instrument bus check.

The pattern for the upper address and data lines is shown in Fig. 4-25. Each lower order line changes at a rate that is twice the next higher line, resulting in 128 cycles on the LSB lines. The initial pulse on the upper four data lines is not part of the divide-by-two pattern and is not repeated on the lower four data lines. By comparing the lines to those in Fig. 4-25, checking that they divide-by-two, it is possible to discover open or shorted lines. Look for lines that stay high or low, change together or at wrong times in the pattern, or go to indeterminate logic levels (-1 to -2 V).

TROUBLESHOOTING ON THE INSTRUMENT BUS

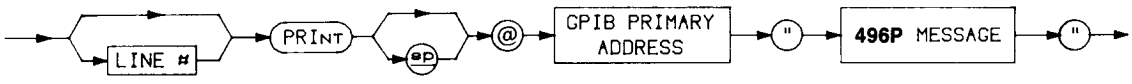
Instrument Bus Data Transfers

The 496P can execute two commands and queries to aid troubleshooting of circuit functions that are interfaced to the instrument bus. These functions are configured by data sent from the microcomputer or respond with data for the microcomputer; in either case, the data is transferred over the instrument bus. The commands and queries provided for this purpose are:

Command	Query	Action
ADDR	ADDR?	Sets, returns address for DATA command
DATA	DATA?	Sets, returns data on 496P instrument bus

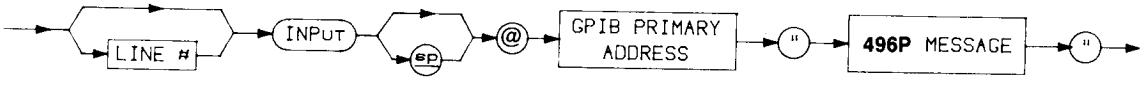
Because the DATA command can change the status of internal functions, its use may prevent normal operation of the 496P

Using a 4050-Series controller, these commands and queries are transmitted to the 496P with the PRINT statement:



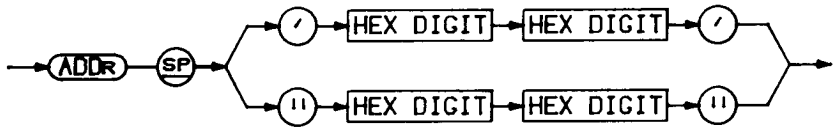
For the GPIB PRIMARY ADDRESS, enter the decimal equivalent of the GPIB ADDRESS switch settings on the 496P rear panel.

The 496P response to a query is input with the INPUT statement:



A string variable is formed by adding a dollar sign ($) to a variable name such as A or X1, making: A$ or X1$.

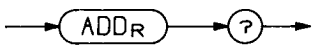
ADDR (instrument bus address) command:



3784-165

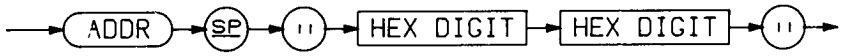
HEX. DIGIT: A character in the sequence 0 through 9 and A through F representing a hexadecimal digit. The two digits (in order) form a number to represent a location on the instrument bus. If a character is not a hexadecimal digit or part of a pair of digits, it is not used in executing the ADDR command and an error is reported.

ADDR (instrument bus address) query:



3784-166

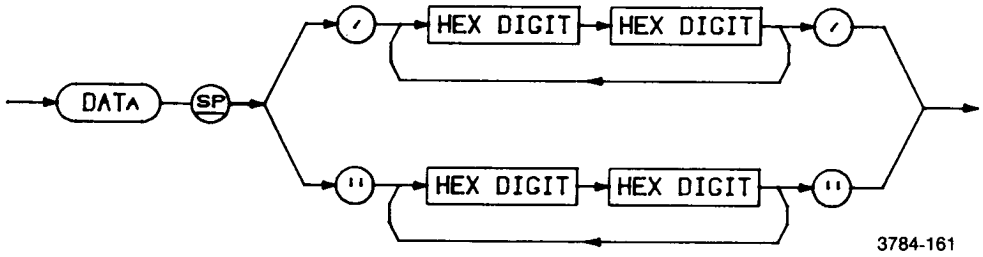
Response to ADDR query:



3784-167

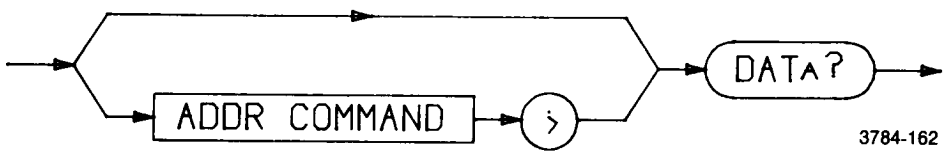
The two digits form the hex. address that applies to succeeding DATA commands or queries.

DATA (instrument bus data) command:

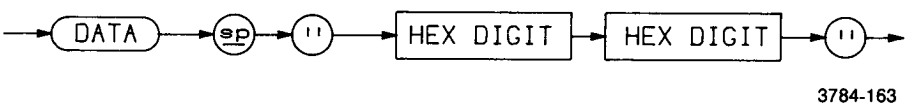


HEX. DIGITS: As with ADDR, a pair of digits forms a hex. number. The number is a data value to be stored at the instrument bus location specified by the last ADDR command. This allows internal 496P parameters to be set for servicing; these parameters control functions by setting the status or mode of 496P circuit assemblies. Up to 16 pairs of characters are accepted to set a function to a new value repeatedly. If a character is not a hex. digit or part of a pair of digits, the data byte formed by the pair is not executed and an error is reported. Also, an error is reported when data is sent to an invalid address.

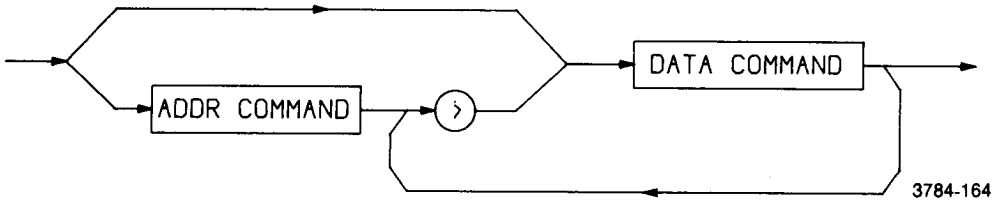
DATA (instrument bus data) query:



Response to DATA query:



Combined ADDR command and DATA command:



The address command may precede a data command or query to identify the instrument bus location as part of the same message.

Errors related to ADDR and DATA commands:

Error	ADDR and DATA COMMAND
41	ADDR/DATA argument invalid
42	ADDR not compatible for DATA command

Instrument Bus Registers

Registers provide the link between the instrument bus and microcomputer-controlled functions. The registers are defined here in order according to the number of the diagram where the register appears. The definitions are provided to help in constructing DATA commands (see above) and interpreting responses to DATA queries.

The data is presented here as binary. In some cases the data occupies the entire register width, as does a value in digital storage, for instance. In other cases, a single bit or group of bits in the register conveys a code. The upper five bits in the sweep rate and mode register indicate the sweep time/division, for instance. The meaning of the data is not fully defined here; refer to the description of the circuit module in Section 5 for details.

To use the binary data and codes presented here with the DATA command and query presented above, you must convert binary to hexadecimal. This takes three steps:

1) group the lower four bits and the upper four bits (break the data byte in half);

2) convert each group of four bits to a hex. digit. Hex. digits range from 0 to F in this sequence: 0123456789ABCDEF;

3) group the two hex. digits together, keeping their respective places—upper and lower.

For example, binary code 01001011 would be transformed by:

1) 01001011 = 0100 1011

2) 0100 = 4 and 1011 = B (8+0+2+1=B)

3) 4 and B make the two-digit hex. number 4B.

Variable Resolution Mother Board #2 (refer to schematic diagrams 19, 21 and 22). There are two variable resolution registers that the microcomputer writes to, although both are addressed at 3F. The data MSB steers the other bits that are defined into the desired register. When DB7 equals 1, it steers DB0 through DB2 to select the resolution bandwidth. When DB7 equals 0, it steers DB6 through DB0 to select the amount of gain added in the VR section and the band-leveling gain. These two functions are addressed and set together by the same data byte, although they are broken into two portions of the table below to show the portions of the data byte that form the codes for the two functions.

Table 4-6

VARIABLE RESOLUTION DATA REGISTER (3F)

Resolution Bandwidth DB7=1

DB7	DB2	DB1	DB0	Selects
1	0	0	1	1 MHz
1	0	1	0	100 kHz
1	0	1	1	10 kHz
1	0	0	1	1 kHz
1	1	0	1	100 Hz
1	1	1	0	30 Hz

Gain, Leveling DB7=0

DB7	DB6	DB5	DB4	DB3	Leveling
0	0	0	0	0	Normal

DB7	DB2	DB1	DB0	Gain
0	0	0	0	0 dB
0	0	0	1	10 dB
0	1	0	0	20 dB
0	1	0	1	30 dB
0	1	1	1	40 dB

Log and Video Amplifier (refer to schematic diagram 24). Two registers receive data from the microcomputer; one controls video offset (78) and the other controls display modes and vertical scale factor (79).

Table 4-7

LOG & VIDEO AMP REGISTERS (78 AND 79)

Bit	Function/Mode
Video Offset (78)	
DB7—DB0	Video offset, LSB = 1/4 dB, total range = 63.75 dB
Modes and Scale Factor (79)	
DB7	Pulse stretcher on/off (1/0)
DB6	Identify offset on/off (1/0)
DB5 DB4	
0 1	Lin
1 0	Log
0 0	Full-screen deflection
DB3—DB0	Log vertical scale factor in dB/div

Video Processor (refer to schematic diagram 25). A register (7C) controls out-of-band clamping, video filtering, and leveling.

Table 4-8

VIDEO PROCESSOR CONTROL (7C)

Bit				Function
DB5	DB6	DB7		Out-of-Band Clamp
1	1	0		No clamp
1	0	0		Clamp upper 5 div
1	1	1		Clamp lower div
0	1	0		Clamp lower 5 div
DB4	DB3	DB2	DB1	Video Filter
0	0	0	0	Off
0	0	0	1	30 kHz
1	0	0	1	3 kHz
1	1	0	1	300 Hz
0	0	1	1	30 Hz
1	0	1	1	3 Hz
1	1	1	1	0.3 Hz
DB0				Base-line Leveling on/off (1/0)

Digital Storage (refer to schematic diagram 26). Two registers (at 7A and FA) on the Vertical Digital Storage board transfer display data to and from the microcomputer for 496P GPIB operations. Another register (at 7B) controls digital storage functions.

Table 4-9

DIGITAL STORAGE REGISTERS (7A, FA, AND 7B)

Bit	Function
Digital Storage Input (7A)	
DB7—DB0	Data values for digital storage. A write to 7B clears the address counter so values are stored for points on display starting at left and proceeding to right in order.
Digital Storage Output (FA)	
DB7—DB0	Data values from digital storage. A write to 7B initializes output to begin at left of trace and proceed to right.
Digital Storage Control (7B)	
DB7	Halt/run (0/1) storage acquisition
DB6 DB5	PEAK/AVERAGE cursor
1 1	Knob position
1 0	PEAK
0 1	AVERAGE
DB4	MAX HOLD on/off (1/0)
DB3	VIEW B−A on/off (1/0)
DB2	VIEW B on/off (1/0)
DB1	VIEW A on/off (1/0)
DB0	SAVE A on/off (1/0)

Z-Axis/RF Interface (refer to schematic diagram 30). A register on the Z-Axis/RF Interface board enables Z-axis and RF attenuator control.

Table 4-10

Z-AXIS AND RF DECK CONTROL (4F)

Bit			Function
DB7			Baseline clipper on/off (1/0)
DB6	DB2	DB0	RF attenuation
1	1	1	0 dB
1	1	0	10 dB
0	1	1	20 dB
1	0	1	30 dB
1	0	0	40 dB
0	0	1	50 dB
1	1	1	60 dB
DB5			= 0
DB4			= 0
DB3			= Set to 0 for 100 ms to switch attenuator

Crt Readout (refer to schematic diagram 29). One register (5F) controls crt readout and data steering. Another register (2F) accepts data from the microcomputer.

Table 4-11

CRT READOUT REGISTERS (5F AND 2F)

Bit	Function
	Crt Control (5F)
DB3	1 = max span dot 0 = center frequency dot
DB2	1 = error or GPIB RDOUT message (page 2) 0 = normal readout (page 1)
DB1	1 = data sent to 2F is character address 0 = data sent to 2F is character code
DB0	1 = readout on 0 = readout off—required to load characters
	Address/Data (2F)
DB1	in 5F = 1
DB6—DB0	Address in readout RAM. Upper line is 0—31. Lower line is 32—63 (page of RAM selected by DB2 at address 5F)
DB1	in 5F = 0
DB7	1 blanks character (used for space)
DB6	1 shifts character down 1/2 screen (used for upper readout only)
DB5—DB0	Lower 6 bits of ASCII code for character

Front Panel (refer to schematic diagram 38). Writing to register 74 loads data into shift registers that drive all the lights on the front panel, including the one for the crt graticule. Four 8-bit shift registers store the data, requiring eight writes of four bits each time (one bit for each register) to update the front-panel lights. The table below shows the order that data is entered to control the lights. A 0 turns on the light (except in the case of the crt graticule); a 1 turns off the light.

Reading from F4 accesses the keyboard encoder and the FREQUENCY knob encoder.

Table 4-12

FRONT-PANEL REGISTERS

Write Number	DB4	DB2	DB1	DB0
Writing data to shift registers for lights (74)				
1	MAX HOLD	ZERO SPAN	GRAT ILLUM	CAL
2	CLIP	REMOTE	FINE	LIN
3	AD-DRESSED	10 dB	READY	NARROW
4	READOUT	20 dB	LINE TRIG	WIDE
5	ΔF	Not Used	SINGLE SWEEP	B—SAVE A
6	Not Used	MIN NOISE	FREE RUN	VIEW B
7	AUTO RESOLU-TION	PHASE LOCK	INT RUN	VIEW A
8	PULSE STRETCH-ER	UNCAL	EXT TRIG	SAVE A
A 1 on DB3 initializes encoder (power-up)				

Bit	Functions
Reading data from switch encoders (F4)	
DB7	FREQUENCY down/up (1/0)
DB6—DB0	Switch codes

Sweep (refer to schematic diagram 32). The microcomputer writes to two registers (0F and 1F) to control sweep rate, mode, holdoff, interrupts and triggering.

Table 4-13

SWEEP REGISTERS

DB7	DB6	DB5	DB4	DB3	Time/Div
Sweep Rate and Mode (0F)					
1	1	0	1	1	20 μs
1	0	1	1	1	50 μs
1	0	0	1	1	100 μs
0	1	0	1	1	200 μs
0	0	1	1	1	500 μs
0	0	0	1	1	1 ms
1	1	0	0	1	2 ms
1	0	1	0	1	5 ms
1	0	0	0	1	10 ms
0	1	0	0	1	20 ms
0	0	1	0	1	50 ms
0	0	0	0	1	100 ms
1	1	0	0	0	200 ms
1	0	1	0	0	500 ms
1	0	0	0	0	1 s
0	1	0	0	0	2 s
0	0	1	0	0	5 s
0	0	0	0	0	10 s
1	1	1	1	1	Manual
0	1	1	1	1	External
A 1 on DB2 sets single-sweep mode					
A 1 on DB0 sets trigger in single-sweep mode					

Bit		Function
Holdoff, Interrupt, Trigger (1F)		
DB7		1 enables end-of-sweep interrupt
DB6	DB5	Sweep Holdoff
0	0	Short
0	1	Medium
1	0	Long
DB4	DB3	Trigger Mode
0	0	Free run
0	1	Internal
1	0	External
1	1	Line
DB0		Aborts sweep

Span Attenuator (refer to schematic diagram 33). Two registers (75 and 76) control the span attenuator.

Table 4-14

SPAN ATTENUATOR REGISTERS (75 AND 76)

Bit		Function
Span Magnitude (75)		
DB7—DB0		Lower 8 bits of 10-bit attenuation code (000 is max attenuation)
Span Magnitude and Attenuator (76)		
DB7		Sweep ± (1/0) to match ± mixing
DB6	DB5	Sweep decade attenuator
0	0	X 1.0
0	1	X 0.1
1	0	X 0.01
DB4	DB3	Output select and calibration
0	0	1st LO main coil
0	1	1st LO FM coil
1	0	2nd LO
DB2		For future use
DB1—DB0		Upper two bits of attenuation code

1st LO Driver (refer to schematic diagram 35). One register (72) controls functions on the 1st LO Driver board.

Table 4-15

1st LO DRIVER REGISTERS (72)

Bit	Function
1st LO Driver Functions (72)	
DB7	Normal/max span mode (1/0)
DB6	Connect/disconnect sweep voltage to driver (1/0)
DB5	Driver off/on (1/0)—off for degauss
DB4	Filter on/off at driver output (1/0)—on for unphase-locked narrow spans
DB3	Normally 0
DB2	Normally 1
DB1	Normally 1
DB0	Normally 0

Center Frequency Control (refer to schematic diagram 34). Registers are provided for control functions (70) and data values for center frequency DAC(s) (71). A read (F0) returns the results of a comparison of the DAC output voltage and a memory voltage.

Table 4-16

CENTER FREQUENCY CONTROL REGISTERS (70, 71, AND F0)

Bit	Function/Meaning
	Control (70)
DB7	1st LO storage gate open/close (1/0)
DB6	0 steers DAC data to 1st LO high byte
DB5	0 steers DAC data to 1st LO mid byte
DB4	0 steers DAC data to 1st LO low byte
DB3	2nd LO storage gate open/close (1/0)
DB2	0 steers DAC data to 2nd LO high byte
DB1	0 steers DAC data to 2nd LO mid byte
DB0	0 steers DAC data to 2nd LO low byte
	DAC Data (71)
DB7—DB0	Data for center frequency DAC(s) steered by control register
	Center Frequency Control Read (F0)
DB7	1st LO DAC stored voltage comparator
DB0	2nd LO DAC stored voltage comparator

1st LO Phaselock Control (refer to schematic diagram 12). A register (73) accepts data to preload the ÷n counter and control the synthesizer. Successive reads from another register (F3) obtain status and counter outputs. After resetting the counter output register selector, three read cycles return status bits and counter bits in the most significant byte and remaining counter bits in following bytes.

Table 4-17

PHASELOCK CONTROL REGISTERS (73 AND F3)

Bit	Function/Meaning
	Write (73)
DB7	1 clocks data on DB0 into a latch
DB6	0 (unused)
DB5	1 clears the counters
DB4	1 transfers DB0 serial data to control latch outputs
DB3	1 resets the counter output register selector
DB2	For future use
DB1	1 transfers DB0 serial data to synthesizer N latch outputs
DB0	Serial data for control of synthesizer N latches
	Read (F3)—Most Significant Byte
DB7	1 = error voltage below a preset amount
DB6	1 = error voltage above a preset amount
DB5	Always 1
DB4	1 when phaselocked
DB3	1 when valid count is in counters
DB2—DB0	Upper three bits of counter output; the remaining 16 bits are in the following two bytes

THEORY OF OPERATION

This section of the manual describes the circuitry in the 496/496P Spectrum Analyzer. The description begins with a general and functional description related to a block diagram of the major systems within the 496/496P. This is followed with a detailed description of the circuitry within each section; for example, the Display section.

The number in the diamond refers to the corresponding schematic diagram number. Note that these same numbers are included on diagrams. Schematics of all major circuits are in Volume 2, section 8.

◇1 FUNCTIONAL AND GENERAL DESCRIPTION

What It Does

The 496/496P Spectrum Analyzer accepts an electrical signal as its input and displays the signal's frequency components on a crt. Signals can be applied directly to the RF INPUT or, if the analyzer is equipped for external mixer operation, to an external mixer, which extends the measurement range of the 496/496P.

The display of the frequency components of the input signal appears on the crt as a graph where the horizontal axis is frequency and the vertical axis is amplitude. The display can also be plotted on a chart recorder using rear-panel connectors. The 496P can transmit the display digitally via the IEEE 488 bus.

Manual operation of the 496/496P Spectrum Analyzer is accomplished through the front-panel knobs and switches. The 496P may also be operated via the IEEE 488 bus using a straightforward language format.

How It Works

The Functional Block Diagram is located at the front of the Diagrams section. It relates the major sections in the instrument and shows the main signal paths. Refer to the diagram while reading this general description.

The 496/496P operates as a swept, narrow-band receiver. As it sweeps a range of frequencies, it moves the crt beam horizontally. When it detects a frequency component of the input signal, it deflects the beam vertically. The center frequency of each span is set by the FREQUENCY control. The frequency range of each span is set by the SPAN/DIV control. The power level represented by the vertical deflection is set by the REFERENCE LEVEL control; this control causes the microcomputer to change the input RF attenuator or IF gain, or both, to bring signals within the display range.

First, Second, and Third Converters

In the 496/496P Spectrum Analyzer, this swept-frequency analysis is achieved with a triple-conversion superheterodyne technique.

Each of the three frequency converters consists of a mixer, a local oscillator, and appropriate filters. Only one frequency can be properly converted in each mixer and pass through all bandpass filters and reach the detector. The analysis frequency is changed by tuning the first or second local oscillators. The fixed 100 MHz calibrator signal is used for the third local oscillator.

The first converter, usually referred to as the front end, converts the input signal frequency to an intermediate frequency (IF) at 2072 MHz. A lowpass filter is used to prevent images and spurious responses.

The second converter has its own local oscillator, mixer, and filters. This stage converts the signal to 110 MHz and sends it to the third converter.

The third converter amplifies and filters the 110 MHz signal and converts it to the final intermediate frequency of 10 MHz. The signal is then passed to the IF section, which applies a set of user-selected bandpass filters and amplifiers.

IF Section

The IF section analyzes how much power is present in the frequency component that has been converted to 10 MHz. Three functions are performed here:

1) weak signals can be amplified by a set of switchable amplifiers so that they may be analyzed. By amplifying the signal, the vertical window (dynamic display range) is shifted up or down. The REFERENCE LEVEL control selects the gain (and input RF attenuation as a pair) to frame this window;

2) the signal is bandpassed by any of several 10 MHz bandpass filters selected by the RESOLUTION BANDWIDTH control. The greater the selectivity, the better two closely-spaced signals can be resolved, but narrow bandwidths require longer sweep times. The microcomputer selects the best combination of bandwidth and sweep time, unless overridden by the operator;

3) the remaining signal is detected by a combination of a logarithmic amplifier and a linear amplitude detector. The output of this combination is a voltage that corresponds to the signal strength in decibels. This amplitude detector output is sent to the vertical channel of the display section to show the strength of the particular component.

Display Section

The display section draws the display on the crt screen. Vertical deflection of the beam is increased as the output of the amplitude detector increases. The horizontal position is controlled by the frequency control section and corresponds to the frequency analyzed at that instant. As the 496/496P sweeps from low frequencies to high frequencies during its analysis, the beam is swept from left to right. Any time a signal is encountered during the analysis, a vertical deflection shows the strength of the signal at the horizontal position corresponding to the frequency. The result is a display of amplitude as a function of frequency.

The video amplifier scales the output of the detector for vertical deflection in dB/div or performs a log/linear conversion, depending on the vertical display mode. The video processor filters the video if either the wide or narrow filter is selected.

The display section displays control settings on the crt based on data from the microcomputer.

The sweep is often rapid enough to give a flicker-free display, but at times the sweep must be slowed below the flicker rate. The display can be recorded and refreshed at a flicker-free rate by the digital storage section. The 496/496P can read out the display data from digital storage through the IEEE 488 interface.

Frequency Control Section

The instantaneous frequency being analyzed is controlled by the frequencies of the local oscillators. To analyze another frequency, a local oscillator frequency is changed so that the new frequency is converted by the three converters to 10 MHz and passes through the IF section. Each converter section has its own local oscillator. Only the local oscillators of the first two converters are changed to vary the frequency being analyzed; the 3rd LO remains fixed.

The 496/496P periodically sweeps and analyzes a frequency range centered about a frequency set by the FREQUENCY knob. The FREQUENCY knob tunes the first and second local oscillators. The analyzer sweep is generated by the sweep generator and the span attenuator. As the sweep generator sweeps through its range, the trace is deflected across the screen on the front panel. The frequency sweep is controlled by the span attenuator, which scales the sweep according to the current SPAN/DIV. The output of the span attenuator drives the 1st LO to sweep wide spans and the 2nd LO to sweep narrow spans. Phaselock circuitry is used to stabilize the 1st LO in narrow spans.

Digital Control Section

Internal functions are controlled from the front panel through a microcomputer. An internal instrument bus allows communication between the microcomputer and all parts of the instrument. Front-panel control data goes to the microcomputer on this bus. The microcomputer controls circuit functions such as; the span attenuator, IF gain, and crt readout on this bus. The microcomputer also receives information from circuit functions such as, the sweep and phase lock circuitry on this bus.

The 496P may be controlled remotely through the IEEE 488 bus, which interfaces to the microcomputer through a General Purpose Interface Bus (GPIB) board. The IEEE 488 connector is located on the rear panel of the instrument. The control language corresponds closely to front-panel operation of the 496P.

Other Systems

The power supply system provides regulated dc power for all parts of the instrument. The switching supply is capable of regulation over wide line frequency and line voltage ranges.

The cooling system consists of an intake on the bottom of the case, air passages within the instrument, a fan, and a rear panel exhaust. Air is routed to all sections of the instrument in proportion to the heat generated by that section. Internal temperature rise is small for reliable operation.

Signal, power, and control connections between sections are accomplished by a mother board distribution system. Most circuit boards plug onto the mother board from the top side. Components on the RF deck underneath the mother board are also connected to the mother board through smaller connectors.

For Further Information

The systems in the 496/496P are described in eight sections as shown by the Functional Block Diagram. Eight block diagrams representing these systems follow the Functional Block Diagram.

For more detailed information, the instrument is divided into circuit diagrams for each assembly or part of an assembly. Each schematic is accompanied by a detailed block diagram and a parts location illustration. These are printed in the Diagrams section with look-up tables to aid in finding components on either the schematic or parts location illustration.

DETAILED DESCRIPTION

The following description is arranged by sections or systems; such as 1st Converter, 2nd Converter, etc., followed by circuit analysis of the circuits within that section. Each system/section is introduced with a description of the system using the block diagram found in the Diagrams section of the manual. This is then followed with a description of each circuit board or major circuit within the system.

1ST CONVERTER CIRCUITS

The 1st Converter mixes the incoming RF signal with a tunable local oscillator signal to generate intermodulation products. All of the products are filtered out except the 2072 MHz IF signal, which is applied to the 2nd Converter circuit.

The 1st Converter consists of the following major segments.

1) The RF Attenuator, which sets the input power to the analyzer;

2) A 1.8 GHz lowpass filter, which attenuates input signals that could cause spurious responses and images. This filter is terminated with a 3 dB pad to prevent interaction between the lowpass filter and the directional filter.

3) A four-port Directional Filter, which couples the input signal to the 1st converter. The 2072 MHz IF product generated by the 1st Converter is sent back through the Directional Filter toward the 2nd Converter. (The fourth port is terminated with a 50 Ω dummy load.)

4) A lowpass filter and a 2.072 GHz bandpass filter, which accept the signal from the Directional Filter and send it to the input of the 2nd Converter.

5) A 1st Mixer, which mixes the incoming RF signal with the 1st Local Oscillator to generate a 2072 MHz IF product.

6) A Power Divider, which splits the signal from the 1st LO for application to the 1st Mixer and the Phase Gate Detector.

7) A Phase Gate Detector, which compares the phase of the 1st LO to the strobe signal of the 1st LO phaselock system.

8) A 1st Local Ocillator (LO), which is a voltage-controlled YIG (Yttrium-Iron-Garnet) oscillator that provides a tunable signal for the 1st Mixer. The phaselock system is activated when spans of 50 kHz/DIV or less are selected.

9) The RF Interface circuits, which select the input RF attenuation.

The input RF is fed through a 0 to 60 dB decade attenuator, a 1.8 GHz lowpass filter, a 3 dB attenuator, and a Directional Filter before it reaches the 1st Mixer. The lowpass filter attenuates out-of-band signals, preventing them from reaching the mixer and creating images. The attenuator matches mixer impedance and protects the mixer diodes from spurious or static signals.

The 1st LO feeds signals to the 1st Mixer through the Power Divider. The Phase Gate Detector couples off a small amount of signal to compare with a strobe signal from the 1st LO phaselock system. The output is an error signal that is used by the phaselock system for determining the FM tuning voltage for the 1st LO.

The 1st LO output is mixed with the incoming RF, and the IM products are routed through the Directional Filter to a 4.5 GHz lowpass filter, a 2.072 GHz bandpass filter and the 2nd Converter. The lowpass filter removes odd multiples of 2.072 GHz that are caused by re-entrant modes of the Directional Filter.

The single balanced mixer creates fewer IM products than an unbalanced mixer, resulting in decreased conversion loss.

RF INTERFACE/Z AXIS 30

Introduction

Refer to the block diagram adjacent to Diagram 30. The RF Interface circuits receive address and instruction data from the Microcomputer, decode it, and control the RF Attenuator. The circuit consists of the Digital control circuits, which decodes the address and control the input data to the buffer. The RF Interface section also includes the driver circuits, which furnish the current required to drive the RF Attenuator.

Digital Control

Address decoder U2045 enables the data at the input of U3046 whenever address 4F is selected by the microcomputer. Table 5-1 lists the purpose of each data line from the buffer.

Transistors Q2025 and Q3028 are enabled by a negative pulse from the microcomputer. The two transistors raise the Vcc of the three attenuator drivers (U3034, U3029, and U3038) to +16 V for about 100 ms; this furnishes sufficient voltage to energize the attenuator solenoids. Each of the attenuator driver output lines is protected by a diode from the inductive kick that occurs when the solenoids change state.

Timer

M1019 is an electrochemical timer. The current through R1015 causes the copper band to progress along the scale that is calibrated for a duration of 5000 operating hours.

Table 5-1
RF INTERFACE LINES

Line	Purpose
Q1	Enables 10 dB attenuator
Q2	No connection
Q3	Enables 30 dB attenuator
Q4	Enable current drivers Q2025 and Q3028
Q5	Not used
Q6	Not used
Q7	Enables 20 dB attenuator
Q8	Enables baseline clipping

1st CONVERTER 11

Introduction

The input RF signal is sent through a 0 to 60 dB attenuator, a 1.8 GHz lowpass filter, a 3 dB pad, and the Directional Filter. The Directional Filter routes the incoming RF to the 1st Mixer, which generates a 2072 MHz IF product from the RF and 1st LO frequencies. The Directional Filter accepts the IF signal from the 1st Mixer and couples it to a 4.5 GHz lowpass filter, which rejects the re-entrant modes of the Directional Filter and sends the IF signal to the 4 Cavity Bandpass Filter. This filter, which has a 15 MHz bandwidth at 2072 MHz, passes the IF signal to the 2nd Converter.

RF Signal Path

The 0 to 60 dB step attenuator consists of three sections (10 dB, 20 dB, and 30 dB), which are controlled by relays that receive drive signals from the RF Interface circuit. The output of the attenuator is connected to the 1st Mixer through a 1.8 GHz lowpass filter, a 3 dB pad. and a Directional Filter. The 3 dB pad protects the mixer diodes from excessive input voltages and static discharges. The lowpass filter prevents RF above 1.8 GHz from generating spurious images in the 1st Mixer.

1st Mixer

The 1st Mixer receives the RF signal through the Directional Filter and the 1st LO signal through the Power Divider. These signals combine to produce intermodulation products that are filtered to yield the 2072 MHz IF signal. The mixer is a single balanced design, which has a lower conversion loss than unbalanced mixers. The local oscillator input is split through a broadband multi-section coupler, whose outputs are equal in power but 90° out of phase. An additional 90° of phase shift is cascaded with the appropriate signal to create a 180° phase difference that is applied across a pair of series-connected Schottky diodes. This causes the diodes to be alternately switched on and off as the oscillator cycles. The RF input is applied to the node between the two diodes; this node is isolated from the 1st LO input by approximately 30 dB. The dc return path for the mixer is through the 50 Ω termination on P124.

The fundamental conversion loss of the 1st Mixer is approximately 14 dB. The Schottky diodes are mounted in a removable assembly that can be removed or replaced within the main mixer module. These diodes are extremely sensitive to static charges; see the Maintenance section before attempting removal or replacement.

Power Divider

The Power Divider splits the output of the 1st LO between the 1st Mixer and the Phase Gate, providing more than 15 dB of isolation at the output ports. The Power Divider also serves to improve the load seen by the 1st LO. The divider is essentially two multi-section directional couplers that are multi-port cascaded, with two output ports of equal power.

1st Local Oscillator (LO)

The 1st LO is a YIG (Yttrium-Iron-Garnet) oscillator with a 2.072 to 3.872 GHz tuning range. The oscillator assembly includes the interface circuit board that couples operating and tuning voltages from the 1st LO Driver, Span Attenuator, and Error Amplifier circuits to the oscillator.

The +15 V1 voltage provides operating bias for the oscillator. The supply is protected by VR1010, C1016, and R1011. The second supply, +15 V2, is for future applications. Diodes CR1018 and CR1019 stop transient voltages from entering the tune voltage coils. It also protects the driving circuits from degaussing transients.

Relay K1015 is closed when the FM coil is used to tune the oscillator. To prevent the tune volts coil from moving the oscillator frequency when the FM coil is in operation, C1012 an C1014 are connected across the tune coil. The heater keeps the YIG sphere at a constant temperature, improving stability.

Directional Filter

The Directional Filter couples the broadband RF signal to the 1st Mixer. It also couples the 2072 MHz IF signal to the 2nd converter through the lowpass and bandpass filters. As intermodulation products from the 1st Mixer flow through FL16, they induce a selected current into a one-wavelength distributed ring, which couples the 2072 MHz IF signal out to FL11, the lowpass filter. The ring is only excited by 2072 MHz. The bandwidth of this ring is approximately 45 MHz.

High IF Filters

The 2072 MHz signal from the Directional Filter is passed through FL11, a lowpass filter that rejects all signals above 4.5 GHz. The second filter, FL14, is a 4 Cavity bandpass filter with a bandwidth of 15 MHz. This filter rejects intermodulation products above and below 2072 MHz.

② 1st LO PHASELOCK SYSTEM

Functional Description

This is a frequency control system that substantially improves the stabilization of the 1st LO (first Local Oscillator).

The phaselock system consists of two frequency servo loops, called the outer loop and inner loop. Operation of the inner loop is as follows: The 100 MHz reference signal from the 3rd Converter is applied to the Synthesizer, where it is first divided by two, then sent to the phaselock circuits to be used as a reference frequency. It is further divided to 25 MHz in the synthesizer circuits and applied to the ÷ N circuits which reduce the signal to a reference frequency (depending on the ÷ N number), between 32 and 94 kHz and applied to the Offset Mixer, where it is compared with the mixer output. The original 25 MHz is also applied to the Offset Mixer.

The Controlled Oscillator operates between 25.032 and 25.094 MHz, depending on the drive from the Error Amplifier. This signal is applied to the Offset Mixer, where it mixes with the 25 MHz reference frequency. The difference frequency, which is from 32 to 94 kHz, is applied to the phase/frequency detector and compared to the ÷ N reference frequency. If the two signals are edge and frequency coincident, phaselock occurs. If they do not coincide, an error signal is generated, passed through the Error Amplifier, and applied to the Controlled Oscillator. This forces the oscillator to shift to the reference frequency. This evolution typically lasts for only a few milliseconds, so the inner loop phaselock is, for all practical purposes, instantaneous.

The outer loop, which includes the inner loop circuits (Offset Mixer, Error Amplifier, and Controlled Oscillator), consists of the Strobe Driver, Phase Gate, Error Amplifier, and 1st LO. (The phaselock control circuits are a part of the operation, but are not considered a part of the loop.)

The 25.032 to 25.094 MHz output from the Controlled Oscillator is applied to the Strobe Driver, where it is divided by five, filtered, and sent to the Phase Gate Detector as a 5.006 to 5.019 MHz strobe signal. This signal generates line spectra that are equally spaced about 5 MHz apart over the entire spectrum (at about the 400th line, which corresponds to about 2 GHz). Assuming that the 1st LO is tuned in that vicinity, one of these lines is within 2.5 MHz of the 1st LO frequency. The Phase Gate outputs a signal that is proportional to the difference between the 1st LO frequency and that of the nearest strobe line. The signal is counted by the phaselock control circuits.

Now, as the search for phaselock begins, the microcomputer moves the strobe in about 1 MHz increments. It does so by sending a new number for each step to the ÷ N Counter. With each change in the ÷ N output signal, the Controlled Oscillator frequency changes to match, and the strobe signal shifts toward the 1st LO frequency. When the Phase Gate generates an error that is below 500 kHz, it passes through the filter in the Error Amplifier circuits, and the microcomputer is notified of the proximity of the strobe. The microcomputer now backs the strobe away from the 1st LO frequency in smaller increments until the 500 kHz bandwidth is encountered. This locates the 1st LO to be about 500 kHz away from the strobe signal. The microcomputer now moves the strobe to the middle of the bandwidth, about 250 kHz away, then takes three small steps closer while noting the change in error frequency with each step. With this information, the microcomputer can compute the position of the 1st LO frequency, does so, and places the strobe within approximately 10 kHz of the 1st LO frequency. Then, the microcomputer commands "lock", which puts a more precise servo system into operation, as follows.

Previously, the microcomputer was moving the strobe around to find coincidence with the 1st LO frequency. The F(s) amplifier in the Error Amplifier circuits will now change the current to the FM Coil of the 1st LO so the 1st LO frequency finds and locks on frequency with the strobe. Any frequency difference between the strobe signal and the 1st LO will generate a correction voltage of low frequency that is filtered by the F(s) amplifier, then used to drive the FM Coil back to the strobe position. If the 1st LO drifts beyond the operating range of the F(s) amplifier, the microcomputer is alerted and the remainder of the circuits indicate the direction of drift. The microcomputer then tunes the Center Frequency Control circuits to null out any FM coil current in the phaselock loop.

1st LO PHASELOCK CONTROL 

Refer to the block diagram adjacent to Diagram 12.

The Phaselock Control section consists of the following major circuits.

1. The address decoder, which receives and decodes the talk and listen commands for the phaselock loop.

2. The service request circuits, which sense an impending loss of phaselock, send a service request to the microcomputer, and cancel the request when directed by the microcomputer.

3. The data buffer, which transmits and buffers data from the microcomputer to the phaselock control and inner loop circuits.

4. The multiplexer divider circuits, which multiplex input signals, including the F ERROR signal, and divide the signal frequency for application to the counter-buffer stages.

5. The counter buffer, which accumulates the divided signal from the multiplexer-divider circuits; then, upon command from the microcomputer, multiplexes the data from the buffers to the data bus. Some status signals share one of these buffer stages.

6. The phaselock sensor circuit, which monitors the SEARCH signal, and informs the microcomputer of phaselock status.

Address Decoder

The addresses from the microcomputer are decoded by decoder U7055. The phaselock control circuits have both a talk address, where the counter-buffer circuits are instructed to talk on the data bus, and a listen address, where U7041 is directed to receive data from the data bus. The talk address is F3; the listen address is 73.

Service Request Circuits

The service request circuits consist of multiplexer U6105, one-shot U6028B, latch U6066A, and associated circuitry. This circuitry alerts the microcomputer in the event that the 1st LO has drifted too far.

The UP and DOWN signals from the window comparator (located on the Error Amplifier board) drive NOR gate U6015. Both signals are also sent to U4025, where their status can be read by the microcomputer. When one of these signals is high it indicates that the Error Amplifier is approaching its operating limits and the microcomputer should adjust the 1st LO frequency so the Error Amplifier returns to the center of its range. A high at either input of U6015B produces a negative transition that triggers one-shot U6028B. U6028B remains set for about 35 μs and sets U6066A, causing two actions to occur: The Q output drives Q7060 into saturation initiating the service request for this address and the complement output of U6066A pulls the 1G and 2G inputs of multiplexer U6105 low, enabling both sides. This device allows Q4090 and U6066A to respond to inquiries by the microcomputer to determine which address requested service. The microcomputer initiates the polling routine, which consists of pulling the POLL signal and AB7 high, then interrogating each data bus line in succession to determine which requested service; that is, which data line is low. This is done by setting the 1Y output of U6105 high, which causes Q4090 to pull the D2 line low. To affirm which address requested service, the microcomputer now causes the 7 address line to move low, which, via the 2Y line from U6105, clocks U6066A to the reset state as the microcomputer holds data bus line 2 low. This cancels the service request by cutting off Q7060, permitting its output to move high. In addition, the complement output of U6066A moves high, disabling the inputs to U6105. This brings the service request circuitry back to its original state.

Data Buffer

This consists of buffers U7041, U6078D, U6078A, and U6078E. U7041 is the listen buffer for the Phaselock Control circuits. When address decoder U7055 is addressed to listen by the microcomputer it enables U7041, which passes on the buffered data to the other circuits in the Phaselock Control and inner loop circuits. The function of each data bits is as follows:

D0 This line carries the data that preloads the ÷ N counter in the synthesizer circuits bit by bit in serial format.

D1 The N LATCH signal is sent on this line. It is used to latch the N DATA into the synthesizer counters.

D2 Reserved for future applications.

D3 This signal resets the buffer sequencer at the outset of a talk cycle for the counters.

D4 This line (CONTROL LATCH) latches a control word into the output buffers of U2025 on the Error Amplifier board.

D5 This signal clears all the counter stages in the counter-buffer circuits in anticipation of a count sequence.

D6 By controlling the state of U6066B, this line selects the signal source to be passed through U2105 to be counted.

D7 This line furnishes the clock pulses for two areas of circuitry. First the clock, which starts out coincident with the N DATA on line D0, is delayed by an RC circuit; then, it passes through buffer U6078D where it is sent in two directions. The signal is buffered through U6078E and used as the clock pulse for U6066B. Also the signal, now delayed, is used as the shift register clock for the ÷ N counter latches on the Synthesizer board. The slight delay is to provide adequate setup time for the data prior to the clock signal arriving.

Multiplexer-Divider

This circuit consists of U6078B, U2105, and U2091. The F ERROR signal enters at pin 12 of the board where it is routed through buffer U6078B and applied to multiplexer U2105. This multiplexer selects between several signal sources to be counted. However, all other possible signal sources apply to future applications, so for the time being, U2105 passes to only the F ERROR signal through to U2091. The F ERROR signal enters the multiplexer at pin 4.

It is passed through to the 1Y output, and into the upper section of dual four-bit binary counter U2091, where it is divided by two, and sent out the QA output. This signal is passed through the other side of the multiplexer, out the 2Y line, into the lower section of U2091. The QC output of U2091, which is the F ERROR signal divided by eight, is applied to the first counter, U2065. The QD output, which is F ERROR signal divided by 16, is used to control the multiplexer, and to keep the microcomputer posted on the progress of the count.

Figure 5-1 illustrates the timing relationships. The circuit functions as follows. At the outset of a count cycle, the microcomputer sets the D5 line high, to clear all of the counters including U2091. All outputs of U2091 that are connected are low. This enables U2105 to pass signals. At the first negative edge from the F ERROR signal, U2091 begins counting. Eight cycles later QC moves high, enabling U2065 to begin counting the buffered 50 MHz signal from the synthesizer circuits, by way of U4014C. The count continues until eight more cycles of F ERROR have occurred, at which time line QD moves high, disabling the multiplexer and stopping the F ERROR signal from passing. The count will remain in the counters until it is cleared by a command from the microcomputer.

Counter-Buffer Stages

This circuit consists of counters U2065, U4062, and U2055; buffers U4049, U2036, and U4025; buffers U6015A and U4074B; and the buffer multiplexer, which consists of counter U2078 and buffer U4074A.

As mentioned earlier, the 50 MHz signal from the Synthesizer is applied to the input of U2065, and the five four-bit stages are permitted to count this signal for the period that U2091, pin 9, remains high. As this occurs, the microcomputer periodically examines the state of the VALID COUNT line. It does so by resetting U2078 through data sent through U7041; when U2078 is reset, pin 3 is high. When the microcomputer pulls the Y7 line of U7055 low, the outputs of U4074A are enabled, which in turn enable the outputs of buffer U4025. These output lines are connected in common to the output lines of the other two buffers, but neither of the others are enabled, so they have no effect for the present. The microcomputer is thus able to examine the VALID COUNT line; if it is still low, indicating that the count is not complete, the microcomputer releases the Y7 line, which increments U2078 and disables U4074A. This in turn disables all three buffers and clears the data bus. If the VALID COUNT line is high when the microcomputer interrogates the stage, the data from U4025 is accepted; the microcomputer then re-addresses U7055, which increments U2078, and U2036 is enabled instead of U4025. The microcomputer accepts that data, then once more increments U2078. This enables the last of the three buffers, U4049, to send its data on the bus. When the microcomputer receives the last of the three data bytes, it resets U2078 and clears the bus.

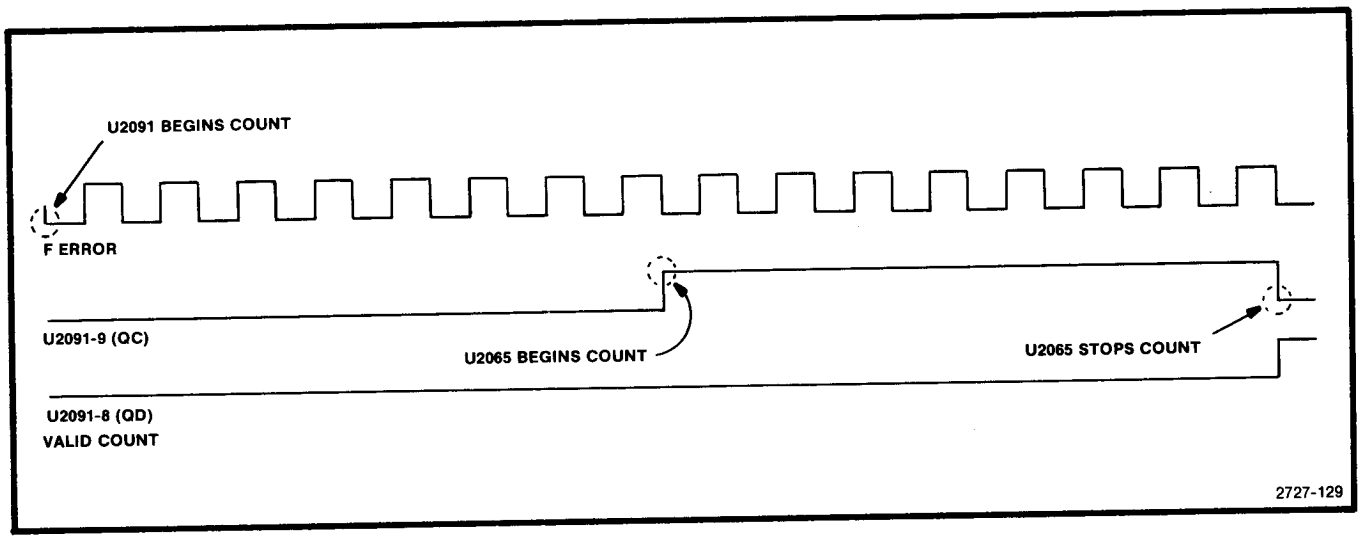


Fig. 5-1. Timing diagram for F ERROR signal.

Phaselock Sensor Circuits

This circuitry consists of transistors Q7030 and Q5030, single-shot U6028A, plus surrounding circuitry. The SEARCH signal from the Error Amplifier is applied to Q7030 for amplification, then applied to trigger the one-shot U6028A. The period of the SEARCH signal (when the 1st LO is not phaselocked) is shorter than the time constant of U6028A so the single-shot cannot return to its quiescent state. Thus when the microcomputer examines the D4 line, it is informed that the circuits are still in search condition and that phaselock has not yet occurred. The Q output of U6028A drives Q5030, which during search condition holds the UP and DOWN lines low, preventing the Service Request circuits from calling for a fine tuning routine. (See previous description on Service Request circuits.) When the instrument finally enters phaselock, the error amplifier stops oscillating (i.e., searching for a lock point), U6028A times out to the reset state, and the LOCK line from U6028A moves high. When the microcomputer later interrogates the board, it will be informed that the instrument is in phaselock. Also when the single-shot times out, Q5030 is cut off, permitting the UP and DOWN lines to move freely so that the service request circuits are once again in operation.

1st LO ERROR AMPLIFIER AND SYNTHESIZER ◇13◇ ◇14◇

The Synthesizer uses the 100 MHz reference frequency from the 3rd Converter to generate 50 MHz for the Phaselock Control, and 25 MHz plus a ÷ N frequency, determined by the ÷ N number, for the Offset Mixer. The ÷ N number produced by the Synthesizer, is determined by the microcomputer and ranges from 32 to 94 kHz.

The Error Amplifier:

1) integrates the error signals from the Offset Mixer and produces a correction voltage to pull the Control Oscillator to a frequency that is synchronous with the ÷ N signal;

2) generates a STROBE ENABLE to enable the strobe generator in the Strobe Driver circuit;

3) produces an UP or DOWN signal to alert the microcomputer that the drive current to the 1st LO FM coil is reaching its limit in holding the 1st LO in phaselock;

4) generates an F ERROR signal, from the outer loop ERROR 1 signal, to be used by the Phaselock Control in determining the proximity of the 1st LO frequency to the strobe line.

Synthesizer Circuits

The Synthesizer can be divided into the following functional blocks: the 100 MHz divider, the 50 MHz divider, and the ÷ N counter.

100 MHz Divider. This circuit consists of flip-flop U3030, and differential pair Q3040 and Q3041. The 100 MHz signal from the 3rd Converter stage is applied to the clock input of U3030. (One-half of U3030 is used to furnish a stable bias source for the clock input.) The signal from the Q output is applied to Q3041, from which it is sent to the Phaselock Control circuits. The signal from the complement output of U3030 is applied through Q3040 to U1040B, the 50 MHz divider.

50 MHz Divider. This circuit consists of U1040B. The 50 MHz from the collector of Q3040 is applied to the clock input of flip-flop U1040B which divides the signal to 25 MHz. The signal from the Q output is sent to the Offset Mixer circuits. The complement signal is applied to the ÷ N Counter.

÷ N Counter. This stage consists of two shift register/latches U2020 and U2030; three counters, U2010, U1020, and U1030; and flip-flop U1040A. The circuit is controlled by three signals from the microcomputer by way of the Phaselock Control circuits. The ÷ N Counter is used to furnish the 32 to 94 kHz reference frequency, which is applied to the Offset Mixer circuits. When power is first applied, and before phaselock is selected, this counter typically operates at about 6 kHz.

When phaselock operation is selected, the microcomputer sends data and a data clock to load a number into the latches, which accept and store serial data. The numbers that come from the microcomputer range from about 3300 to 3830, so the count remaining, until the counters overflow, is from about 265 to 795. When the number is loaded, the N LATCH signal transfers the number from the input shift registers to the output registers of U2020 and U2030 where they are available to the counter stages. This presets the counters to a predetermined value, as just mentioned. Once loaded, the counters count at a 25 MHz rate to accumulate the remaining number of digits until they are full. Then the TC output of U1030 moves high and U1040A changes state. This presets the N number in the counter stages for another count cycle. The TC output of U1030 is again simultaneously set low so the next cycle of the 25 MHz clocks U1040A back to the reset condition. The resultant output of U1040A is a series of positive pulses that range in period from 10 μs to 31 μs which is equivalent to 94 to 32 kHz. This signal is sent to the Offset Mixer for comparison with the difference frequency generated in the mixer circuit.

Error Amplifier

The Error Amplifier circuits consist of the digital control circuits, which decode the data from the microcomputer to drive other circuits on the board; the inner loop error voltage amplifier, which furnishes the tune voltage to the Controlled Oscillator; the search amplifier which drives the phaselock sensor circuits on the Phaselock Control board and the FM coil of the 1st LO; the window comparator which drives the service request circuits on the Phaselock Control board; and the error signal filter which filters and squares the ERROR 1 signal from the Phase Gate, and applies it to the multiplexer-divider circuits on the Phaselock Control board.

Digital Control Circuits. These consist of shift register U2025 and quad switch U2037. Data from the microcomputer is fed serially, by way of the Phaselock Control circuits into the shift register, then transferred to the output lines by the LATCH signal. Table 5-2 lists the purpose of the output lines.

Error Voltage Amplifier. This stage, which consists of differential amplifier U3075 (shown on Diagram 13) and surrounding components, compares the outputs of the phase/frequency detector on the Offset Mixer board, furnishing an oscillator tune voltage to the Controlled Oscillator. Refer to the Offset Mixer description that follows for a more detailed description of this circuit.

Search Amplifier. This circuit consists of amplifier U2048 and surrounding components. The ERROR 1 signal from the Phase Gate Detector and Error Amplifier is applied through LOOP GAIN adjustment R3082 to the inverting input of U2048. The signal (ERROR 1) is a result of the comparison of the 1st Local Oscillator frequency and the nearest multiple of the STROBE signal from the Strobe Driver circuit. The ERROR 1 signal varies from zero to about 500 kHz, and is up to four volts peak-to-peak in amplitude. The LOOP GAIN adjustment is set for best sensitivity with minimum hunting.

Amplifier U2048 is connected to operate as a low-pass filter/integrator for the incoming ERROR 1 signal. During search operation, however, the inverting input side of the amplifier causes the stage to operate as a Wien-bridge oscillator at about 25 Hz. At this point, the U2037 outputs are in the following states: Q1 line is high (contacts open) because the phaselock system is in search mode; Q2 is high (contacts closed, which allows U2048 to drive the FM coil); Q3 is high, allowing the lock bandwidth to be over 100 kHz wide (thus, the Wien-bridge circuitry has sufficient positive feedback to oscillate); Q4 is high, which enables the strobe; and Q5 is low because the system is in search mode. (Q1 and Q5 remain open during this part of the search operation to hold the window comparator disconnected.)

As the Strobe signal frequency is changed to be nearer the 1st LO frequency, the ERROR 1 signal decreases in frequency. Since the inverting side of U2048 is a low-pass filter, the decreasing frequency receives more amplification, until enough feedback occurs on the inverting side to suppress the oscillations on the non-inverting side (i.e., the negative feedback exceeds the positive feedback that normally sustains oscillations).

The SEARCH signal (once locked) is now essentially a dc level so the Phaselock Control circuits indicate to the microcomputer that lock has occurred; it in turn causes line Q3 to move low, closing the feedback path for the inverting side of U2048. This decreases the bandwidth, ensuring that the amplifier cannot break into oscillation until phaselock is broken. It also improves the close-in noise performance of the phaselock loop.

Table 5-2
U2025 OUTPUT LINES

Line	High	Low
Q1	Window disabled (QS low)	Wide window (QS low)
Q2	Lock (connected FM coil)	Unlock (disconnected FM coil)
Q3	Search (wide loop gain response)	Narrow loop gain response
Q4	Strobe enabled	Strobe disabled
Q5	Narrow window	Wide window (with Q1 low)

Window Comparator. This circuit consists of U1015 and the associated components, and is used to sense when U2048 has approached its operating limits. When the microcomputer causes the Q2 signal to close the path from U2048 to the FM coil, U2048 begins to furnish current to the coil which causes the 1st LO to track the stable strobe signal. That is, each time the 1st LO frequency drifts, the ERROR 1 signal changes and U2048 shifts the FM coil current to bring the 1st LO back to its original frequency. At the same time, the microcomputer causes lines Q1 and A5 to be low, closing the contacts that connect the output of U2048 to the input of the window comparator through a divider network. Now, as the 1st LO frequency drifts, the search amplifier will compensate for the drift. If the drift is excessive, however, U2048 will approach its design limits and will be unable to furnish any more current to the FM coil.

Window comparator U1015 is a dual comparator stage that senses a deviation of ±15 mV. For instance, if a frequency shift forces U2048 to move positive enough (approximately 3 V), the upper half of the comparator conducts, and the UP line goes high. This triggers the service request circuits on the Phaselock board, which in turn alerts the microcomputer, which then begins adjusting the TUNE voltage from the Center Frequency Control circuits. If the output drifts negative, the other half of U1015 conducts, causing reverse action to occur.

Ordinarily, the input to the window comparator is attenuated by R2043, which reduces the voltage applied to U1015 to 0.3% of the output from U2048. This allows U2048 to drift up and down without immediately triggering either comparator. When R2043 is in the circuit, it is called "wide window" operation. When phaselock is de-selected, the microcomputer selects narrow window (which bypasses R2043). The Center Frequency Control circuit is then instructed by the microcomputer to move the 1st LO frequency until the window comparator indicates that the FM coil current is near zero. This prevents the 1st LO frequency from shifting too far from the lock point when phaselock is cancelled.

Error Signal Filter. This circuit, which consists of active lowpass filter U2065 and Schmitt trigger U1035, filters and squares the incoming ERROR 1 signal for application to the Phaselock Control circuits. The ERROR 1 signal is applied through C2067 to an RC filter network that is a 500 kHz low-pass filter. After filtering, the signal is applied through ERROR COUNT BREAKPOINT adjustment R1061 to the input of U1035, a Schmitt trigger circuit. The squared output signal is then applied to the Phaselock Control circuits where it is used by the microcomputer for determining the relationship between 1st LO frequency and the strobe line.

1st LO CONTROLLED OSCILLATOR, OFFSET MIXER, AND STROBE DRIVER ◇14◇

Controlled Oscillator

The Controlled Oscillator is a voltage-controlled crystal oscillator whose frequency is controlled by the output of the Error Amplifier. The oscillator generates a reference signal that is used to stabilize the 1st LO frequency.

Refer to the block diagram adjacent to Diagram 14. The control voltage from the Error Amplifier, which is a function of the difference between the microcomputer controlled ÷ N signal and the Offset Mixer difference frequency, is applied to the Controlled Oscillator to regulate its frequency of operation. The circuit has two outputs: the first, which is part of the inner loop of the phaselock circuits, is fed to the Offset Mixer, where it is used to derive the difference frequency that is compared against the ÷ N signal. The second output, which is part of the outer loop, is fed to the Strobe Driver circuits, where it is divided down to become the STROBE signal that is compared against the 1st LO signal in the Phase Gate.

The Controlled Oscillator consists of five major circuits, four of which are connected in a positive feedback loop to sustain oscillation. These circuits are the resonator stage, the differential amplifier, the bandpass filter, the isolation amplifier, and the output amplifier. The resonator stage operates at a frequency of 25.032 MHz to 25.094 MHz. It presents a high impedance to ground at resonance, which reduces as the operating frequency moves away from the resonant point. The output signal from the resonator is fed to the differential amplifier, which splits the signal and sends it to the output amplifier and the bandpass filter. The output amplifier sends the signal to the Offset Mixer and the Strobe Driver, and reduces loading of the feedback loop. The bandpass filter strips the signal of any spurious responses or harmonics and feeds the signal to the isolation amplifier. This stage furnishes the positive feedback drive to the resonator stage and isolates the bandpass filter from the resonator stage.

The resonator stage consists of crystal Y1012, varactor diodes CR1011 and CR1012, and related components. The stage operates within a frequency range of 25.032 to 25.094 MHz, controlled by the voltage applied to varactor diodes CR1011 and CR1012. Feedback energy for sustaining oscillations comes from the isolation amplifier by way of coil L1025.

The resonator output signal is applied to a differential amplifier Q2033 and Q2041. The Q2033 side drives the output amplifier and serves to isolate the output load from the feedback loop. Gain from this side is less than one. The signal is fed from the collector of Q2041, following amplification, into the bandpass filter.

The bandpass filter consists of passive components, and is used to strip the signal of any frequency components more than about 40 kHz away from the center operating frequency, which is approximately 25.06 MHz. Capacitors C1041 and C1042 are adjusted at the factory to set the bandwidth and center frequency of the filter. The signal from the filter is sent to the isolation amplifier.

Transistor Q1028 and related components make up the isolation amplifier. The amplifier is a common-base configuration, in order to match the impedance of the filter to the resonator. Output current from the stage furnishes positive feedback for the resonator.

The output amplifier consists of transistors Q2025 and Q2026, which are connected as a differential pair. The signal from the collector of Q2026 furnishes the signal that drives one side of the Offset Mixer; the signal from the collector of Q2025 drives the input of the Strobe Driver circuit, for eventual application to the Phase Gate circuits.

Offset Mixer

The Offset Mixer consists of a ring diode mixer circuit, a differential amplifier, and a phase/frequency detector. For explanatory purposes, assume that the Controlled Oscillator frequency is at 25.06 MHz and the ÷ N signal is 50 kHz.

The 25.06 MHz signal from the Controlled Oscillator enters the board at pin N of the Offset Mixer assembly. It is applied to the base of transistor Q2021 which drives transformer T2010. The output of T2010 is connected across the ring diode mixer. The 24 MHz reference frequency is applied at pin K of the Offset Mixer and coupled through T1010 to the ring diode mixer. The four frequency components are picked off at the center tap of T2010. The two fundamental frequencies and the sum are blocked by a pi filter, and the 60 kHz difference is coupled across T2030 to a differential pair Q1020/Q1030, then amplified to TTL levels by amplifier Q1040 and applied to the clock input of flip-flop U1050B, part of the Phase/Frequency detector.

The Phase/Frequency detector consists of flip-flops U1050A and U1050B, NAND gate U2050B, and inverter U2050A. Now, if the loop had been locked, the two flip-flop clock input signals would have been edge-coincident. Pin 4 and 5 inputs of U2050B would have moved high and after the signal at TP1058 goes low, the NAND gate would have reset both flip-flops. The result would have been a series of pulses of equal amplitude and width from each of the flip-flops. This would cause equal voltages to be applied to the Error Amplifier, and the Controlled Oscillator frequency would shift.

It is assumed, however, that the ÷ N signal is 50 kHz and the difference frequency from the collector of Q1040 is 60 kHz, for this description. Thus, the output of Q1040 is leading the ÷ N signal. IC U1050B sets first placing a high at the inverting input of U3075 which pulls the output of U3075 low until U1050A sets. A short time later, U2050B resets both flip-flops and U3075 will switch back to balance until the next correction cycle. This continues to occur until the two signals applied to the Phase/Frequency Detector are edge-coincident.

The correction voltage in this example from U3075 is applied to the frequency-determining components of the Controlled Oscillator, and its frequency shifts downward. The frequency of the oscillator will continue to decrease until the output of U3075 is stable.

The Error Amplifier, which is part of the Error Amplifier assembly, is described here because it is an integral part of the inner loop. The stage consists of differential amplifier U3075 and surrounding components. As the signals driving the amplifier continue toward one direction, U3075 continues to drive the oscillator down in frequency. The circuit consisting of VR2065, CR3069, R2067, and C2072 clamps the output to prevent the varactor diode from becoming forward biased and stopping the oscillator.

Strobe Driver Circuit

The Strobe Driver circuit consists of ÷ 5 counter U1022, bandpass filter FL2064, source follower Q2091, and AND gate U1091A and U1091B.

The Controlled Oscillator signal is applied to the clock input of counter U1022 which is wired to divide the input signal by five. The STROBE ENABLE 1 line from the Error Amplifier permits the counter to operate when the line is low and is the means by which the microcomputer can shut off or turn on the strobe pulses. The output of the counter, which ranges from 5.006 MHz to 5.019 MHz, is coupled through an impedance matching network consisting of C2030, L1031, C2033, and C1032. This circuit raises the line impedance to about 8200 Ω. The signal is then passed through monolithic bandpass filter FL2064, through another impedance matching network, to the gate of Q2091. The signal is coupled from the source of Q2091 to the inputs of U1091A and U1091B, both of which are configured as buffers. U1091B drives the Phase Gate circuitry, and U1091A is reserved for future applications. Capacitors C1032 an C2105 are selected to provide maximum signal amplitude at TP2087.

2ND CONVERTER CIRCUITS

The 2072 MHz 2nd converter mixes the 2072 MHz from the first converter with the output from a cavity oscillator. This local oscillator is swept over a 7.5 MHz range. At the converter input, a four-cavity bandpass filter is used to pass only the 2072 MHz 1st IF signal and prevent unwanted signals generated within the 2nd Converter from passing back through to the 1st Converter. A diode mixer is used to mix the 2072 MHz IF input and the local oscillator signals to generate the 110 MHz second IF output. The 110 MHz output passes through a 110 MHz lowpass filter that blocks higher frequency signals from the mixer. This signal is then applied to a 110 MHz amplifier.

2ND CONVERTER

The 2072 MHz 2nd Converter converts the 2072 MHz signal output from the 1st Converter to 110 MHz for eventual application to the 3rd Converter. The assembly consists of a low-loss narrow-band four-cavity filter connected through an internal cable to a low conversion loss narrow-band diode mixer and a 110 MHz lowpass filter.

Four-Cavity Filter

The Four-Cavity (bandpass) Filter, which is depicted on Diagrams 10 and 15, is designed to pass only the 2072 MHz IF signal to the mixer and to reflect any other frequencies back to the 1st Converter for termination. In addition, the filter keeps the 2nd Converter LO and mixer products from entering the 1st Converter.

This filter is designed for a 1 dB bandwidth of 15 MHz and an insertion loss of 1.2 dB. Each end resonator is capacity coupled to external circuits through a coupling hat plugged into a 3 millimeter connector. Intercavity coupling is provided by coupling loops that protrude from the machined filter top. The resonant frequency of each cavity is determined primarily by the depth of a gap in the underside of the filter top, and is fine tuned with a tuning screw on the side of each cavity. All of the tight machining tolerances are confined to the top. Thus, the main cavity milling need not be a high precision part. When properly tuned, using a network analyzer, the filter return loss is greater than 25 dB from either end (in a 50 Ω system). Figure 5-2 shows a cross sectional view of the filter; Fig. 5-3 shows the equivalent electrical circuit.

Mixer Circuit

The Mixer circuit in the 2072 MHz 2nd Converter is of the single-balanced, two-diode type, and consists of the mixer, an operational amplifier bias circuit, a delay line, and a low-pass filter. In opertion, both diodes of the mixer are turned on and off by the output signal from the 2181 MHz Cavity 2nd Local Oscillator, through coaxial connector P183. Note that, although the diodes are connected for opposite polarity, both are turned on at the same time because of the 180° phase shift delay line in the input line to the upper deck. Also note that the diodes are matched and must both be replaced if one fails.

2072 MHz RF from the Four-Cavity Filter enters the mixer, where it is switched on and off at a 2182 MHz rate by the mixer diodes. Conduction of the diodes is conrolled by the much stronger 2181 MHz LO signal. Several mixing products result; one, the difference frequency of 110 MHz, is separated from the others by a low-pass filter for use as the IF output.

The two inductors and one capacitor at the output of the mixer form a lowpass filter that passes 110 MHz unattenuated to the 110 MHz Amplifier via coaxial connector P182. Capacitors at each of the three inputs to the mixer function as dc blocking capacitors to keep the diode bias from being impressed upon the RF and local oscillator lines.

The bias circuit, which consists of operational amplifier U1014 and the associated components, establishes the bias for the mixer diodes. Each diode has approximately 2 mA of forward bias. The IF SELECT signal from the Z Axis/RF Interface circuits (applied through feedthrough capacitor C182) is low. This causes the output from U1014A to be at +14 V and the output from U1014B to be −14 V. Diodes CR1014 and CR1018 are thereby reverse-biased. Thus, the series resistances of potentiometer R1019 and resistor R1014, and potentiometer R1010 and resistor R1017 provide forward bias to the diodes. The potentiometers provide for balancing the bias levels.

2ND LO PHASELOCK SYSTEM

The phaselocked 2nd LO provides +12 dBm 2182 MHz signal to the 2nd converter and a −12 dBm signal to the front-panel 2nd LO port. The 2nd LO is divided into an oscillator section and a phaselock section. The machined aluminum housing contains a microwave oscillator, a 2200 MHz reference, and a reference mixer. The sheet metal housing contains a 16-20 MHz phaselock system. The phaselock system serves to improve the noise performance and frequency stability of the microwave oscillator.

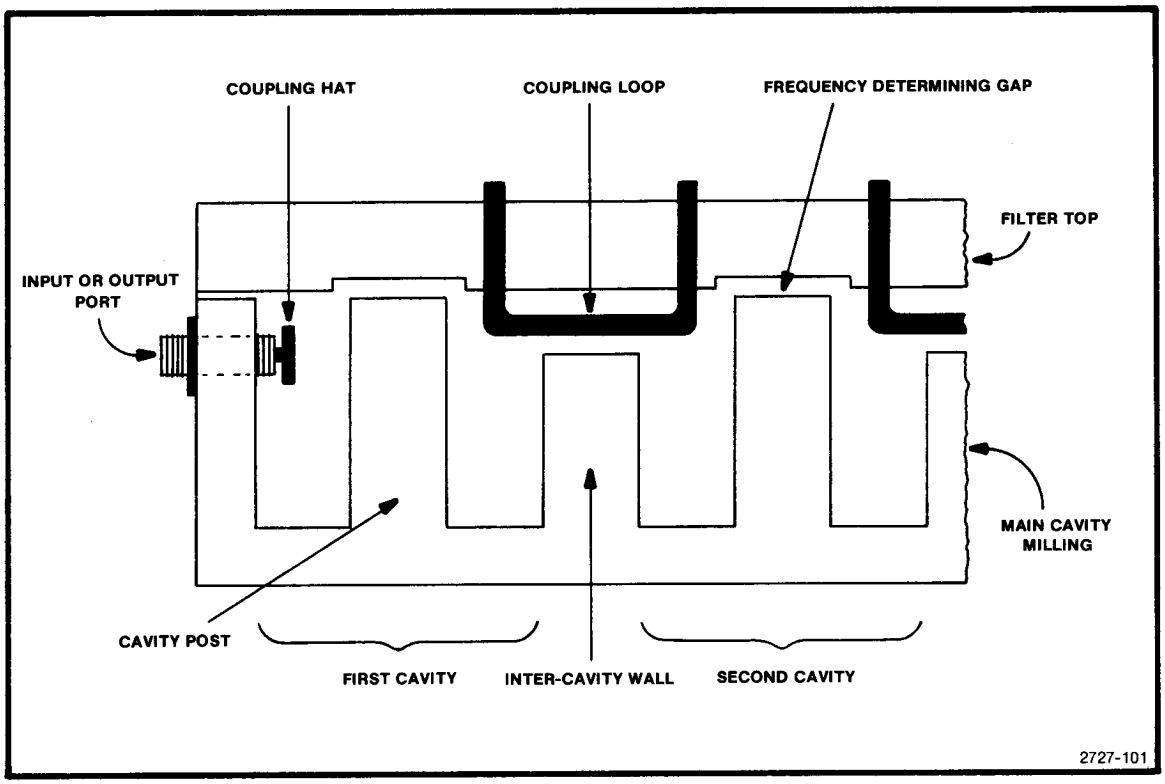


Fig. 5-2. Filter cross-section view.

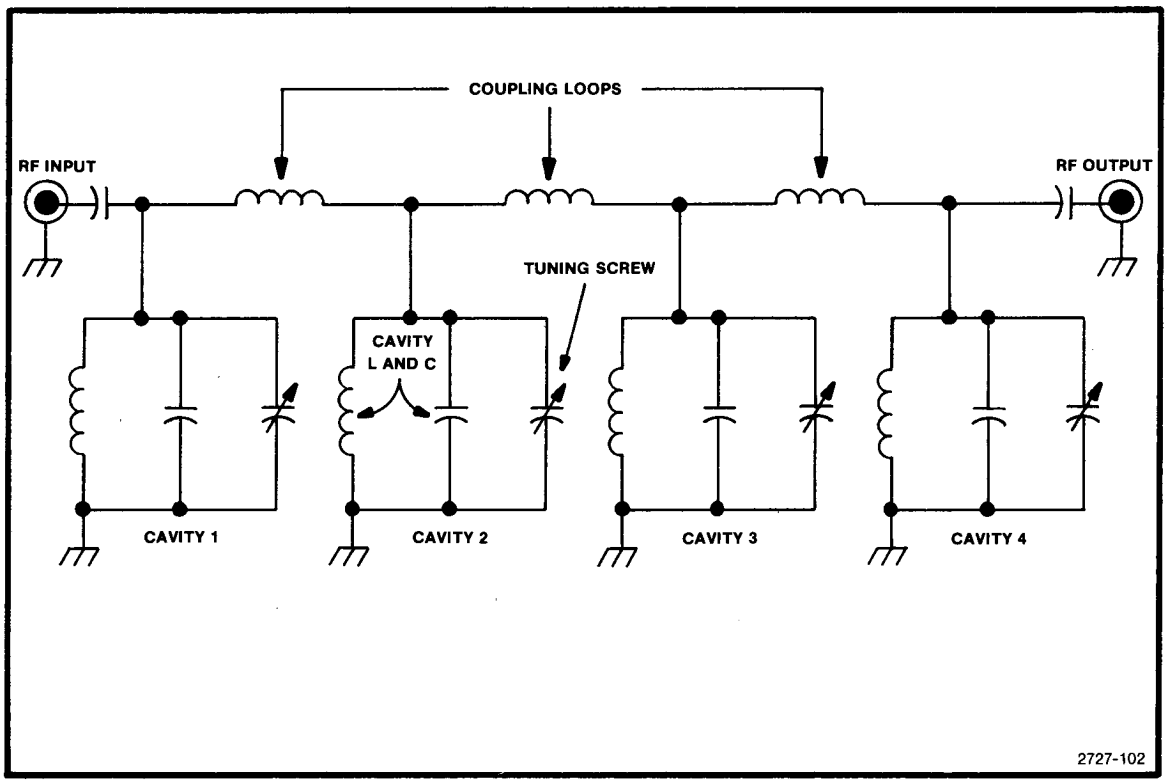


Fig. 5-3. Filter equivalent circuit.

The oscillator section applies the 100 MHz reference signal to a frequency comb generator. The comb generator uses the abrupt switching characteristics of a snap diode to generate harmonics from the 100 MHz input. The 2200 MHz bandpass filter rejects most of the unwanted harmonics, passing 2200 MHz to the reference mixer. 2182 MHz from the microstrip oscillator is also applied, giving an 18 MHz difference product as well as other high-frequency products. A 37 MHz lowpass filter rejects the unwanted products and passes the 18 MHz signal to the phaselock section. (The nominal 18 MHz frequency will change as the 2nd LO is tuned.)

The phaselock section amplifies this 18 MHz signal and applies it to one of the inputs of a phase/frequency detector. A 16-20 MHz voltage-controlled oscillator provides a stable reference for the other input of the phase/frequency detector. Any phase or frequency difference between the two inputs causes a differential voltage output from the detector. This voltage is amplified and used to control the tuning varactor of the microstrip oscillator. The detector forces the oscillator to tune until the difference frequency exactly matches the 18 MHz reference; this feedback loop causes the 2nd LO to always oscillate at 2200 MHz minus the reference frequency. Tuning the reference oscillator from 16 to 20 MHz tunes the 2nd LO from 2184 to 2180 MHz. The noise performance of the 2nd LO emulates the noise performance of the reference oscillator within the 200 kHz control bandwidth of the phaselock loop; outside the control bandwidth, the noise depends primarily upon the noise of the microstrip oscillator.

2182 MHz MICROSTRIP OSCILLATOR

This microwave oscillator is the 2nd LO of the 496/496P. It consists of a printed half-wave resonator driven by a common-emitter feedback amplifier (Q1021). The base of Q1021 is capacitively tapped into the resonator. The resonator serves as a tuned phase inverter and impedance transformer connected between the base and collector of Q1021. A bendable tab allows trimming of the base feedback capacitance of Q1021.

In normal operation, the RF feedback signal is detected by the base-emitter junction of Q1021, producing a dc voltage proportional to the amount of RF feedback. As feedback is increased, the base voltage becomes less positive. The base voltage of Q1021 may be monitored at test point TP1015 without significantly disturbing the microstrip oscillator.

The dc collector voltage and current of Q1021 is regulated by an active feedback circuit. Collector current is supplied to Q1021 through the resonator, which is biased at the midpoint through decoupling inductor L2023. Dc bias voltage on the resonator is sensed by Q2021, which compares the bias with the fraction of supply voltage determined by R2021 and R2022. If the resonator's dc voltage varies from +10 volts, the emitter current of Q2021 changes the dc base current provided to Q1021. The collector current of Q1021 changes, altering the collector voltage until Q2021 senses that the resonator is at +10 volts.

Transistor Q2021 normally acts as a bias current source for the Q1021 base (at high temperatures R2014 serves as a current sink). In the event of −12 volt supply failure, R2015 protects the base of Q1021 from excessive reverse bias. Decoupling and control of bias loop dynamics are provided by C2014. The bias is further stabilized by R2016 serving to swamp the negataive base resistance of Q1021.

The oscillator is tuned by a varactor diode (CR1028) connected to one end of the resonator. RF ground return for the varactor is provided by a printed capacitor that also helps linearize varactor tuning. Decoupling is provided by the lowpass elements in the tune line.

Three output taps are coupled to the resonator through printed capacitors under the resonator. One tap feeds the front-panel 2nd LO port through an 18 dB attenuator; the power level at the front-panel port is approximately −12 dBm. The other two taps pass LO power into 6 dB attenuators followed by buffer amplifiers. The 2nd Converter is driven by +12 dBm and the 220 MHz reference mixer is driven by +10 dBm.

Since the two buffers are nearly identical, only the 2nd Converter buffer is described. Gain is provided by a single common-emitter transistor (Q1011). A printed shunt capacitance and series inductance match the input impedance and printed series and shunt inductors match the output impedance. Out-of-band damping is provided by R1011 in series with a 1/4 wave shorted stub. Dc is blocked by C1014 and C1011. A 1/4 wave open stub is used at the output to reflect one of the 2nd Converter's image frequencies at 4254 MHz (the other buffer does not use or need this stub). Collector bias for Q1011 is provided through R1012, L1011, the 1/4 wave shorted stub, and R1011. The 1/4 wave shorted stub is grounded through C2011. Capacitors C2011, and C1013, and inductor L1011 are also used for decoupling. Collector voltage is a proportion of the −12 volt supply determined by R1013 and R2013; this controls the dc feedback between the collector-base junction of Q1011. The bias network is decoupled from the RF path by L1014. In the event of supply failure, CR2013 protects the base of Q1011 from excessive reverse bias.

2200 MHz REFERENCE BOARD (16)

This board generates a 2200 MHz output from the 100 MHz reference signal.

An input matching network consisting of L1034, L1025, C1036, C1029, and C1025 drives a differential amplifier using Q1024 and Q2024. The emitters of this amplifier are ac coupled through C2026, reducing low-frequency gain and ensuring balanced operation. Large current swings at the collectors are combined and boosted by T2015 to drive CR2014 in and out of conduction. Rapid removal of stored charge causes abrupt current changes each time CR2014 turns off, producing a 100 MHz signal with a very high harmonic content. This signal passes through a 3 dB attenuator. The 2200 MHz harmonic has an amplitude of −28 dBm after passing through the attenuator.

Dc base bias for Q2024 is set at +4 volts by the R2023, R2021 voltage divider, with Q1024's bias supplied through R2019. Each transistor has a quiescent collector current of 10 mA.

2200 MHz REFERENCE MIXER (16)

This board mixes the 2200 MHz reference signal with the 2182 MHz signal from the microstrip oscillator, producing an 18 MHz signal that is filtered to remove unwanted mixing products. CR1011 and CR1012 are the switching elements of the single-balanced mixer. CR1011 is fed with 2182 MHz from one of the microstrip oscillator's buffer amplifiers. A 1/2 wavelength delay line phase-shifts the oscillator driver by 180° before it reaches CR1012, causing both diodes to switch at the same time. A printed inductor at the center of the 1/2 wavelength delay line provides a ground return for the diodes.

The 2200 MHz reference signal enters the board through a printed bandpass filter with a 200 MHz bandwidth. This filter rejects the spectral lines below 2100 MHz and above 2300 MHz. Mixing the 2200 MHz and 2182 MHz signals produces the desired product at 18 MHz as well as a significant product at 82 MHz (this results from mixing 2100 MHz and 2182 MHz). A 7-element 37 MHz lowpass filter rejects all of the unwanted products and passes the 18 MHz product through feedthrough C2204, which connects to the 16-20 MHz phaselock circuit.

16-20 MHz PHASELOCK BOARD (17)

This board contains a voltage-controlled 18 MHz oscillator (with a tune shaping circuit), a phase-frequency detector, and a low-noise regulated power supply. The board acts as a phaselock control for the 2182 MHz microstrip oscillator.

The entire circuit board is shielded from magnetic fields, protecting the 18 MHz VCO and control circuitry from spurious signals. All power supply and control inputs enter the board through feedthrough capacitors (C220-C227) in the housing wall. Interconnections with the microwave circuitry are made through feedthroughs in the floor of the housing.

The +15, −15, and +9 volt supply inputs are re-regulated down to +12, −12, and +5.2 volts by regulators using quiet operational amplifiers. IC U2025 provides a stable −6.95 volt reference that is filtered by R2018 and C2015 and amplified by U2016B, producing the −12 volt supply. IC U2016B uses an emitter-follower (Q2024) to increase the current capability of the supply. Resistor R2013 ensures sufficient base drive, while collector resistor R2025 reduces power dissipation in Q2024. Diode CR2019 protects the base-emitter junction during power supply shutdown. Feedback resistors R2016 and R2017 set the gain of U2016B and control the −12, +12, and +5.2 supply voltages. The −12 volt supply is applied to inverting amplifier U2016A, producing the +12 volt supply, and inverting amplifier U1017, producing the +5.2 volt supply. The output circuitry for the +12 volt and +5.2 volt supplies are similar to the −12 volt supply.

Differential amplifier U2072A accepts the 2nd LO sweep voltages. One input senses the sweep voltage while the other input senses the ground potential at the Sweep board. Sweep sensitivity is adjusted by selecting resistor R2070. In wide spans, the sweep signal passes through parallel resistors R2082 and R2083. In narrow spans, R2082 may be switched out by Q2084, reducing the sweep sensitivity by a factor of ten. When the TTL signal to Q2076 is high, Q2076 is turned off, R2086 holds the gate of Q2084 to −15 volts, Q2084 is turned off, and R2082 is switched out. This reduces the sweep sensitivity. When the TTL signal is low, Q2076 saturates with the collector slightly above 0 volt, Q2084 turns on, and full sweep sensitivity is restored.

Amplifier U2072B accepts the 2nd LO tune voltage. The Tune board senses the ground potential of the 16-20 MHz Phaselock board and floats the tune voltage. Tune sensitivity is adjusted by selecting resistor R2072.

The sweep and tune signals combine the summing node input of a non-linear shaping amplifier. The non-linearity of the shaping amplifier compensates for the non-linear tuning of the reference oscillator varactor, giving a linear tuning characteristic from 16 to 20 MHz. The shaping function is produced by a resistor-diode array in the feedback loop of inverting amplifier U1073A.

All of the amplifier's feedback is through R1072 when the output swings to the negative limit. As the output voltage swings less negative, it sequentially passes the tap-point voltages of a series of voltage dividers connected between 0 volts (the summing node at pin 12) and a negative reference set by Q1047. If the output becomes positive with respect to a given divider tap, a corresponding diode in U2059 forward biases and connects the output to the tap, creating additional feedback through one leg of the divider to the summing node. This causes R2051, then R2052, then R2053 (and so on through R2056) to be connected in parallel with R1072 as the amplifier output becomes less negative. This progressively increases the feedback, causing the gain of U1073A to decrease.

Another series of dividers connected between the amplifier's output and a negative voltage reference causes the diodes in U1059 to sequentially conduct as the output becomes more positive. Resistors R2060, then R2061, then R2062 (and so on through R2065) are sequentially added in parallel with the existing feedback. Soft diode turn-on characteristics and a large number of breakpoints result in smooth gain changes. The non-linear amplifier's voltage-gain characteristic is controlled by the shaper reference voltage, which is set by R2049. Altering R2049 will make the breakpoints either closer together or further apart; in practice, this resistor is selected to correct the tolerance variations of the 18 MHz VCO varactor.

The forward drop of the shaper diodes gives U1073A an offset voltage. Temperature correction diodes CR1086, CR1087, and CR1088 correct this offset over a wide temperature range by summing a correction voltage through R1074. These diodes also compensate for the lack of series diode drop across R1072 and eliminate offsets at the summing input of U1073B. Selecting R1070 provides fine adjustment of the VCO's center frequency. IC U1073B is an inverting amplifier that increases the shaper output voltage swing to a level that can control the varactor of the 18 MHz VCO.

A differential amplifier with well-defined limiting characteristics is used for the 18 MHz VCO. Emitter degeneration is used to control loop gain. Transistors Q2096 and Q2087 form the differential pair of transistors, with the emitters coupled through C2091. Transformer T2092 provides ac feedback for the collector-base junction of Q2096 and also creates the majority of the resonator inductance. The total resonator inductance may be adjusted by trying different combinations of connections between taps on inductor T1091 and transformer T2092. These taps allow coarse adjustment of the VCO center frequency. The capacitor of the resonator is the varactor, CR1089. Capacitor C1088 completes the resonator ac path and acts as a dc block, allowing a bias voltage to be impressed on the varactor. Resistor R2092 and capacitor C2090 damp the Q2096 collector, preventing high frequency instability in the oscillator. Transistor Q2087 provides a buffered oscillator output.

A discrete two-stage amplifier provides an unsaturated voltage gain of approximately 43 dB for the 18 MHz signal from the 2200 MHz Reference Mixer board. Transistor Q1041 is the common-emitter first stage while Q1042 and Q1043 form the differential second stage. The differential stage limits the output swing to 0.8 volt to prevent overdriving the following ECL circuitry. Dc bias is maintained by Q1041, which has dc collector-base feedback via R1046 and the R1043, R1048 voltage divider. Transistor Q1043 receives its base bias through R1042. Each transistor operates with a 5 mA of quiescent current.

ECL line receivers U2041D and U2041B amplify and buffer the 18 MHz signals from the Reference Mixer and the VCO respectively. These two signals are then applied to the phase/frequency detector for comparison.

A pair of ECL D-type flip-flops (U2031A, U2031B) comprise the phase/frequency detector. The flip-flops drive a common reset line with a wired-AND output. The clock input of U2031B is driven with the signal from the 18 MHz VCO and the clock input of U2031A is driven with the signal from the 18 MHz signal from the Reference Mixer.

Both flip-flops are configured to reset together whenever both are set. If they are clocked with signals that exactly match in frequency and phase, then both flip-flops set simultaneously and then almost immediately reset. If the Reference Mixer signal has a slight phase lead, U2031A will remain set longer than U2031B. If the Reference Mixer signal has a slight phase lag, U2031B will set first and remain set the longest. The signal that has the phase lead will cause the associated flip-flop to be set a greater percentage of time than the lagging flip-flop. If there is a frequency difference between the two inputs, the flip-flop with the higher input frequency will be set more of the time than the other flip-flop. The ratio between the filtered output signals of the two flip-flops indicates whether the Reference Mixer signal leads, lags, or differs in frequency from the 18 MHz VCO signal.

The outputs of the flip-flops are lowpass filtered by C1031 and C1028 and applied to differential amplifier U1031. IC U1031 compares the outputs of the flip-flops and produces an output that controls the tuning of the 2182 MHz microstrip oscillator. The phaselock loop bandwidth is controlled by R1026, C1029, R1027, and C1026. The gain slope breaks to −12 dB/octave for frequencies below 16 kHz. Resistors R1033 and R1034 divide and offset the output of U1031 so the tune voltage ranges between 0 and −12.5 volts.

The output of divider R1033, R1034 is applied to the varactor of the 2182 MHz microstrip oscillator (2nd LO). This closes the phaselock loop, tuning the 2nd LO so that it closely tracks the 18 MHz VCO. When the 18 MHz VCO is tuned, U1031 simultaneously tunes the microstrip oscillator an equal amount. Within the loop bandwidth, the 2nd LO performance is determined by the 18 MHz VCO instead of the microstrip oscillator, giving a significant improvement in frequency stability and reduction of phase noise.

◈4 3RD CONVERTER CIRCUITS

The 110 MHz IF Amplifier and 3rd Converter accept the 110 MHz output from the 2nd Converter, amplify and convert the signal to a 10 MHz IF signal which is applied to the resolution circuits in the IF section. The 110 MHz signal is amplified in a three-stage gain block and applied to a three-section bandpass filter. This filter uses helical resonators and has a nominal bandwidth of 1 MHz. From the bandpass filter, the signal is applied to a mixer and heterodyned with a 100 MHz local oscillator signal to produce a 10 MHz third IF signal. The resulting signal, nominally at a level of −35 dBm at the top of the screen, then drives the Variable Resolution circuits.

Initial gain for the analyzer is provided by the 110 MHz IF Amplifier. This gain compensates for signal level losses in the three mixers. Three stages of amplification are used, plus a pin diode controlled attenuator that allows for adjustment of the gain. Typical gain for the amplifier is 21 dB. From the amplifier, the 110 MHz signal is applied to the 3rd Converter through a bandpass filter.

The filter is a three section unit using helical resonators. Its bandwidth of 1 MHz defines the broadest resolution bandwidth of the analyzer, provides good image rejection, and limits noise in the frequency spectrum in which desirable signals appear.

Consisting of a mixer, an oscillator, and various output amplifiers, the 3rd Converter converts the 110 MHz second IF signal into the 10 MHz third IF signal. The local oscillator is a crystal controlled circuit that generates a precise 100 MHz signal. This 100 MHz is applied to the mixer and to output amplifiers. The 100 MHz signal is used in the 2nd Converter and the phaselock section. It is also furnished to a front panel CAL OUT connector for external use.

The mixer is a diode ring type that is fed from balanced drivers which are driven by the 100 MHz oscillator. From the mixer, the output signal, at 10 MHz, is applied to the Variable Resolution section of the 3rd Converter.

110 MHz IF AMPLIFIER ◈18

The 110 MHz IF Amplifier consists of three stages of amplification and an attenuator. Since the first two mixers in the RF system offer no high frequency gain, it is important that this amplifier exhibit low noise characteristics. Also, it must be relatively free from third-order intermodulation distortion.

Signal input to the amplifier is from the 2nd Converter through coaxial connector P321. This signal is nominally 110 MHz and is applied to an impedance matching bandpass filter consisting of inductor L2044 and capacitor C325. The signal is injected into the parallel tuned circuit through a tap in the inductor and taken out at the high impedance side through another variable capacitor, C2047. Inductive input provides for converting to high impedance within the tuned circuit; the extra capacitor on the output provides for converting back to 50 Ω nominal. The primary tuning capacitor (C325) adjusts the resonant point; the output capacitor (C2047) is adjusted in combination with C325 for good impedance match at 110 MHz. This is done using a return loss bridge. The nominal return loss is 35 dB. The Q of the input filter is approximately 20.

From the input filter, the signal is applied to Q4053, the first stage of amplification. This is a broadband feedback amplifier to provide good input and output impedance and controlled gain. All feedback is through reactive components (transformer T3054) not resistive components. Thus, the impedance and gain can be controlled without significant noise problems.

The second amplifier stage, Q4037, is essentially the same as the first, with only minor bias differences. Gain through each of these stages is approximately 9 dB. The output is applied through a 3 dB attenuator, to preserve the impedance figure, to the bridged T adjustable attenuator. The 3 dB attenuator consists of resistors R2039, R2038, and R2043.

From the 3 dB attenuator, the signal is capacitively coupled through C2037 to the adjustable attenuator. This attenuator uses two PIN diodes (CR3030 and CR1029) in the mode in which the resistance to RF signal flow is controlled by the current through the diodes. Refer to Fig. 5-4 as an aid in understanding the following description.

With reference to Fig. 5-4, if resistor R1 were set to infinite resistance and resistor R2 were set to zero resistance, the RF signal path would be through R2 to ground, thereby producing infinite signal attenuation. If resistor R1 were set to zero resistance and resistor R2 were set to infinite resistance, the RF signal path would be through R1 to the load, thereby producing almost no attenuation. This, basically, is how the adjustable attenuator operates, except that resistors R1 and R2 are actually PIN diodes and the RF path resistance through these diodes is controlled by the current through the diodes in an inverse proportion (higher current results in less resistance to RF).

With reference to Diagram 18, resistors R3035 and R2030 establish a constant current of approximately 2 mA from the −15 volt supply to the diodes. This current is divided according to the bias on the diodes. The bias, in turn, is established by gain adjustment R1015, from the +15 volt supply. If R1015 is set low (near ground), diode CR3030 is reverse biased and the 2 mA flows through diode CR1029. This routes the RF signal through resistors R2032 and R3029 and capacitor C2029, with the impedance characteristics of CR1029 added for maximum attenuation.

If R1015 is set higher (nearer +15 V), diode CR3030 is forward biased and starts to conduct. Since the 2 mA supply current is relatively constant, this subtracts from the current through CR1029. Thus, the impedance of the diodes is relatively constant, resulting in a good impedance match over a broad range. Dependent upon the exact amount of current through CR3030, part of the RF signal path is through that diode to the output amplifier and part is through R2032 and diode CR1029 to ground. This results in reduced signal attenuation.

If R1015 is set to the positive limit, the entire 2 mA flows through CR3030. This routes the RF signal through CR3030 (which exhibits little resistance with high current) to the output amplifier with almost no attenuation. (The insertion loss is approximately 1 dB.)

From the adjustable attenuator, the signal is applied to the final amplifier Q3018. This stage is a broadband feedback amplifier that supplies relatively substantial output current and exhibits good intermodulation distortion performance. This is provided primarily through the large current capacity, by negative feedback through resistor R3014, and emitter degeneration through resistor R4029. These resistors are sized to provide a resonably good impedance match at 110 MHz. Nominal gain of the stage is 13 dB.

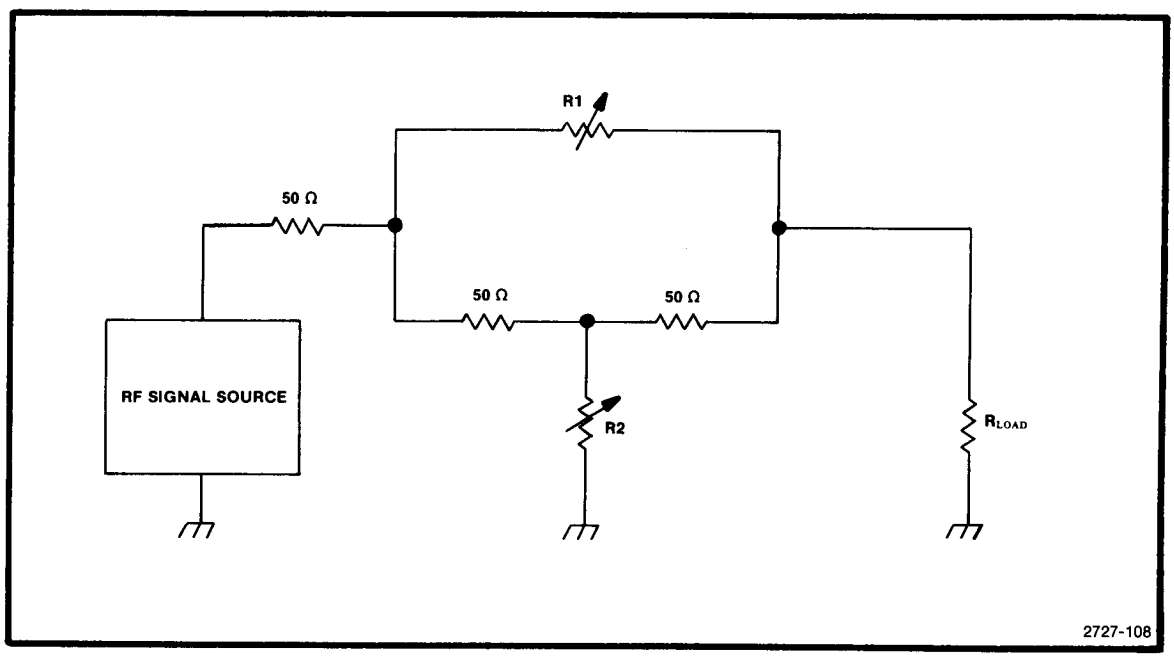


Fig. 5-4. Bridged T attenuator equivalent schematic.

With Gain potentiometer R1015 set for maximum gain (least attenuation) the gain of the 110 MHz IF Amplifier is approximately 26 to 27 dB.

The output signal from the 110 MHz IF Amplifier is applied to the 110 MHz Bandpass Filter.

110 MHz BANDPASS FILTER ⟨18⟩

The 10 MHz Bandpass Filter is a three-section filter using helical resonators, the major function of which is to determine the widest resolution of the analyzer. Another filter function is to provide image rejection (that is, to prevent the mixer from producing 10 MHz outputs from input signal of 90 MHz). Still another function is to limit the noise spectrum appearing at the 10 MHz IF circuits to those frequencies at which signals also appear.

Though the filter is a sealed unit, in the interest of system understanding, the following brief description is provided.

The filter consists of three small helical resonators enclosed in cans and tuned with multi-turn trimmer capacitors. For purposes of impedance matching, the filter is symmetrical. The end resonators are connected to external circuits by 10 pF capacitors attached to taps on the coils. Coupling between resonators is accomplished through holes in the resonator cans.

Adjustment of the filter for minimum attenuation is performed at calibration by setting the three trimmer capacitors. Insertion loss is on the order of 4 to 4.5 dB.

From the filter, the 110 MHz signal is applied to the 3rd Converter.

3RD CONVERTER ⟨19⟩

The 3rd Converter converts the 110 MHz IF signal to 10 MHz for application to the Variable Resolution circuits. It also generates the 100 MHz signal for the 3rd Converter, the front panel CAL OUT signal, and the 110 MHz reference for most of the phaselock loops in the analyzer. The circuits consist of an oscillator and driver, four identical reference output amplifiers, a mixer, and a calibrator output amplifier.

Oscillator/Driver Circuit

The oscillator Q3041 is of the Colpitts configuration with a 100 MHz microwave type crystal operating in the series resonant mode in the feedback loop. That the crystal is a microwave type indicates that it is not only a high-Q type, but that it is mounted at three points to alleviate mechanical vibration problems. (The components inside the dashed line immediately below crystal Y3036 in Diagram 19 are included for future use only and are not described here.) Tuning capacitor C3031 in the collector circuit serves to adjust for maximum output.

From the oscillator collector circuit, the output is RC coupled to driver stage Q2036. The driver is a feedback amplifier that provides output power on the order of +10 dBm to drive all of the reference amplifiers plus the mixer amplifier. The output is transformer coupled from the collector circuit.

Reference Amplifier Circuits

The reference output circuits consist of four identical low-gain common emitter amplifiers with relatively high levels of emitter degeneration. These are transistors Q4018, Q2015, Q3015, Q2016 and associated components. The primary purpose of these amplifiers is to provide isolation among the reference outputs and isolation of those outputs from the oscillator and mixer circuits. The output of each is approximately 0 dBm.

From amplifier Q4018, the output is applied to coaxial connector J2013. This output is not used by the 496/496P. From amplifier Q2015, the output is applied to coaxial connector J2012 and is applied to the 2nd LO. From amplifier Q3015, the output is applied to the 1st LO Phaselock Synthesizer circuits through coaxial connector J1023. From amplifier Q2016, the output is applied to coaxial connector J4027 and is reserved for future use. The Q2016 output is also coupled to the Calibrator Output Amplifier.

Mixer Circuit

The mixer circuit combines the 100 MHz oscillator frequency with the 110 MHz IF signal from the 110 MHz Bandpass Filter to produce the 10 MHz IF output signal. From transformer T2026 of the driver circuit (Q2036), the 100 MHz signal is applied to transformer T2041, which converts the single-ended driver output to a balanced signal to drive the push-pull amplifier that drives the mixer. This amplifier consists of transistors Q1048 and Q2046 and provides a balanced signal, coupled through transformer T3053 to diode ring mixer CR2054. The signal level of the 100 MHz, applied to the mixer, is approximately 100 milliwatts to provide adequate intermodulation distortion performance. The 110 MHz IF, through Bandpass Filter (FL36), is applied through coaxial connector J2058, the impedance matching LC circuit that consists of inductor L1055 and capacitor C1056, and transformer T1053, to the mixer.

The 10 MHz output from the center tap of T1053 is applied through a diplexer and coaxial connector J3057 to the Variable Resolution circuits. Loss through the mixer is typically 6 dB.

Calibration Output Amplifier

The calibrator output amplifier is a differential amplifier (Q2031 and Q1031) that is overdriven. With low levels of drive, this amplifier would operate as a small-signal amplifier. However, with the higher positive and negative levels from reference amplifier Q2016, the transistors are either driven hard or are not conducting at all. Since the transistors are overdriven, the current in the output side (Q1031) is the dc bias current when that side is conducting. Changing the bias current will therefore change the output voltage. Thus, the output is determined by internal dc levels, not input signal levels. Potentiometer R1045 provides for adjustment of that quiescent current.

The output frequency is stable and rich in harmonics. Thus, it provides a useful signal comb of 100 MHz markers to approximately 2 GHz. At 100 MHz, the output level is set by R1045 for −20 dBm which is applied to the front panel CAL OUT connector through coaxial connector J1015.

5 IF SECTION

The IF section receives the 10 MHz IF signal from the 3rd Converter, establishes the system resolution through selective filtering, levels the gain for all bands, and logarithmically amplifies and detects the signal to produce the video output to the Display section.

System resolution is selectable, under microcomputer control, among six bandwidths: 1 MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz, and 30 Hz. This selection is done in the Variable Resolution circuit block by two sets of filters. Bandpass filters are also included at the circuits input and output.

Significant gain is provided in the resolution circuit block by several stages of amplification. Also, the capability to add other gain steps under microcomputer control is provided by switching amplifier gain. These amplifiers, by being switched in combination, provide for 10, 20, 30, or 40 dB of additional gain.

In order that each division of signal change on the crt screen be equal to that for each other division and be equvalent to a similar signal level change in dB, a logarithmic amplification of the signal is required. This is done by a seven stage amplifier that produces an output that is proportional to the logarithm of the input. Thus, the screen displacement can be selectable as to amount of change per divisions, and can be proportional to the input level change. For instance, in the 10 dB per division mode, each division of displacement in the screen represents a signal level change of 10 dB regardless of whether it is at the top or bottom of the screen.

Following the logarithmic amplifier, an area detector produces a positive-going pulse output that is applied to the display section as the VIDEO signal.

Variable Resolution Circuits

20 21 22

The Variable Resolution (VR) circuits provide selection of resolution bandwidth under microcomputer control, and approximately 35 dB of system gain. It consists of two sets of filters and various gain leveling stages. Since the input to the VR circuits is nominally at −35 dBm and the Log Amplifier input must be 0 dBm for full screen, the VR circuits must provide the gain difference. Also, additional gain is required for operation in the 2 dB/DIV or the linear mode.

Physically, the VR section consists of two sub-assemblies that plug onto the analyzer mother board. The input circuits are in one sub-assembly; the output section and digital interface are in the other. Each of the sub-assemblies consists of boards that plug onto a four-layer mother board with a ground plane on both outside layers. Only power supply and control voltages travel through the mother board. All signal interconnection is via coaxial cable.

Circuits for the VR section are contained on three diagrams: 20, 21, and 22. The following paragraphs describe the circuits.

Input 20

The VR Input circuit receives the nominal −35 dBm 10 MHz signal from the 3rd Mixer through J693. This signal is applied to a two-pole, 1.2 MHz bandpass filter that augments the 1 MHz filter that precedes the 3rd Mixer and provides initial selectivity. This 1.2 MHz filter includes C1037 and C1031 and all of the components between. Filter tuning is provided by variable capacitors C1033 and C1026.

From the filter, the signal is applied to broadband feedback amplifier Q1023, which is biased at a relatively substantial output current (approximately 50 mA) to exhibit good intermodulation distortion performance. This performance is provided primarily through the large current capacity, by negative feedback through resistor R1025 and by emitter degeneration resistor R1023.

At the output of amplifier Q1023 is a 6 dB attenuator that provides a clean 50 Ω output to the 1st Filter Select circuits and reflects a 50 Ω termination back through the amplifier for proper termination of the 1.2 MHz bandpass filter. The output signal is transmitted via jumper B.

1st Filter Select 20

The VR 1st Filter Select circuit operates in conjunction with the 2nd Filter Select circuit to determine the overall system bandwidth through banks of switched filters that are selectable under control of the analyzer microcomputer. Data bits 0, 1, and 2 from the data bus are applied to decimal decoder IC U4035, which enables the selected filter by providing a low signal on the appropriate output pin. Bandwidth selections are 1 MHz to 100 Hz in decade steps with 30 Hz as the minimum bandwidth. The data bits select a filter bandwidth according to the following table.

Table 5-3
BANDWIDTH SELECTION

DB0	DB1	DB2	Bandwidth
1	0	0	1 MHz
0	1	0	100 kHz
1	1	0	10 kHz
1	0	0	1 kHz
1	0	1	100 Hz
0	1	1	30 Hz

Selection of filters is done by PIN diode switching. At the input and output of each filter is a series and a shunt diode. When a filter is selected, the series diodes are biased on and the shunt diodes are biased off. For the filters that are not selected (only one is on at a time), the diode conditions are opposite. Since the switching operation is the same for all filters, the following description of the 100 kHz filter selection is applicable to all with appropriate component designators.

If we assume a content of 010 for the three data bits, line 2 from U4035 will be low. This will turn on transistors Q3019 and Q3055, which operate as dc switches. With input switch Q3019 turned on, the current path is through R4012, L3012, CR3010, L3013, R3014, and Q3019. This current is determined by decoupling resistor R3014 and resistor R4012, which is common to all filters, and is sufficient to turn CR3010 on enough that it appears to be merely a resistor to RF. At the same time, the voltage drop across R4012 is sufficient to reverse-bias CR3012. The same operational situation exists for the filter output switch, Q3055. Resistors R3057 and R1067 establish the current to forward-bias CR3061 and reverse-bias CR3060.

Thus, the signal from the Input circuit via jumper B is applied through the selected filter and transmitted to the 10 dB Gain Steps circuit via jumper K. Nominal loss through the filter circuit is approximately 6 dB, with slight variations among the filters.

In the non-selected filter sections, the input and output switch transistors are turned off by the high outputs from decimal decoder U4035. The collectors are pullled toward −15 V by pulldown resistors, thus forward biasing the shunt diodes (input: CR3014, CR2013, CR2011, CR1013, and CR1011; output: CR3062, CR2066, CR2055, CR1055, and CR4065). Since one filter is always selected, the voltage drop across the common input and output resistors (R4012 and R1067, respectively) provides for back biasing the series diodes (input: CR3011, CR3012, CR2010, CR1012, and CR1010; output: CR4068, CR2062, CR2059, CR1059, and CR4064). Note that input and output switching is provided on the board for future use with 30 Hz resolution.

Design of the filter for each bandwidth is determined by the requirements of each band and ranges in complexity from no filter at all to a complex two-crystal arrangement.

In the 1 MHz section no filter is used, because this circuit section is preceded by two filters that accomplish the required function. The first is the 1 MHz filter between the 2nd and 3rd Converters; the second is the 1.2 MHz filter in the VR Input circuit. Instead of a filter, a 6 dB attenuator is contained in the 1 MHz selection circuit. This attenuator provides initial leveling to compensate for absence of filter loss.

The 100 kHz filter is a double-tuned LC circuit that is designed for a good time-domain response shape. Variable capacitors C3023 and C3035 provide for input and output adjustments. Impedance matching is accomplished at both input and output by series capacitors C3020 (input) and C3048 (output).

The 10 kHz filter uses a pair of two-pole monolithic crystal filters that are interconnected by variable shunt capacitor C2037. Input and output impedances are matched with broadband transformers T3026 and T3055. A 3 dB attenuator, consisting of R2027, R2026, and R2028, is included at the filter input.

The 1 kHz resolution filter consists of a single two-pole monolithic crystal filter, matched to the 50 Ω impedance with broadband transformers T2035 and T2055. A 2 dB attenuator, consisting of R2024, R2023, and R2025 is also part of the filter.

The 100 Hz filter uses a pair of high Q crystals in a balanced two-pole ladder configuration. These crystals are matched for both frequency and temperature characteristics. Input and output impedance matching is accomplished primarily by transformers T1025 and T1039. Two small capacitors in the same transformer circuit as the crystals (C1030 and C1035) are adjustable to cancel the parallel capacitance effect of the crystals. Also, a 2 dB attenuator is included at the filter input and consists of resistors R1026, R1028, and R1027.

The 30 Hz filter uses three matched high-Q crystals in a three-pole unbalanced ladder configuration. A small oven with thermal feedback keeps the crystals at a constant temperature while the instrument is operating. The filter is terminated with 50 Ω at both the input and output.

10 dB Gain Step <20>

The 10 dB Gain circuit provides 10 dB of signal gain when selected by the microcomputer. The circuit consists of three stages of amplification, one stage provides variable gain, the other two are fixed gain steps. The nominal input signal level from the 1st Filter Select circuit is −26 dBm for a resolution bandwidth of 100 kHz. (All levels listed in this description relate to the 100 kHz resolution.)

The input signal is applied through an impedance transformer, T3019, to the first amplifier stage consisting of a differential pair (Q3016 and Q2027) and an emitter follower output amplifier (Q1036). Negative feedback through R1031 and R2051, provide gain stabilization. An output resistor, R2035, increases the output impedance of the composite amplifier to approximately 50 Ω.

Gain of the input stage is fixed for all resolution bandwidths except 30 Hz. The gain for 30 Hz is set to a precise level by activating Q2015. Transistor Q2015 is biased on by a low on pin L. This adds R2025 (30 Hz level) across feedback resistor R2051. Adjustment R2025 sets the gain of the stage.

The output from the 1st stage is then applied to a common emiter stage (Q2043). Gain of this stage, when transistor Q4039 is turned on, is 10 dB. When the base of Q4039 is pulled low by data bit 0 from Q4035 on the VR mother board #1, the transistor saturates and shunts the emitter load resistor R3048 with R3038 and the 10 dB Gain adjustment R3035.

The output of Q2043 drives the input of the third amplifier stage. This stage operates the same as the first stage except for gain variation. Feedback resistor R1060 is shunted by PIN diode CR1053. As the current through the diode increases, the resistance decreases and the gain of the stage increases. Gain control of the stage is established by the setting of the front panel AMPL CAL adjustment. Gain range is about 14 dB.

Output impedance of the stage is 50 Ω, set by resistor R1064. Nominal output level is −5 dBm for a full screen display. This level may be as high as +5 dBm when MIN NOISE is active. 10 dB of gain is also removed from the Log Amplifier to reduce the noise level and must be supplied by the VR section.

20 dB Gain Steps <21>

The 20 dB Gain Steps circuit provides −6 dB, +4 dB, +14 dB, and +24 dB of gain in precise 10 dB steps. The nominal −5 dBm input is supplied through pin P from the 10 dB Gain Steps circuit. This signal is applied to a chain of three common-emitter amplifiers, each using emitter degeneration. Changing the emitter resistance is used to change amplifier gain under the direction of the microcomputer.

The nominal gain of the complete circuit is −6 dB, with Q2018, Q2042 and Q1062 biased off. This provides a nominal −11 dBm output. In this condition, control pins V and Y are high, causing switching transistors Q2018, Q2042, and Q1062 to be cut off.

When pin V is low, Q2018 and Q2042 are saturated, raising the total gain of the first two amplifiers 20 dB. Variable resistor R2025 is used to adjust the gain shift of the first stage (Q1025) while the gain shift of the second stage (Q1035) is fixed at +10 dB. This adjustment allows the gain shift to be exactly set to +20 dB.

When pin Y is low, Q1062 is saturated, raising the gain of the third amplifier (Q1043) by 10 dB. Variable resistor R1063 allows the gain shift to be exactly set to +10 dB.

Data bits 2, 1, and 0 control the gains of the 10 dB Gain Steps circuit and the 20 dB Gain Steps circuit. Bit 2 controls pin V, bit 1 controls pin Y, and bit 0 controls pin N. The data is decoded and stored in latches on the VR mother board #2. Table 5-4 shows the state of bits 2, 1, and 0 and the gain shifts of amplifier stages Q2043, Q1025, Q1035, and Q1043.

The output of the 20 dB Gain Steps circuit is attached to coaxial connector J2031. The signal is routed through a double coaxial cable to the Band Leveling circuit.

Band Leveling (21)

The two amplifiers in the VR Band Leveling circuit correct the gain variations caused by the front end.

The output level of this board is −2 dBm while the nominal input is −11 dBm. This input level occurs at 100 kHz resolution in Min Distortion mode.

The two amplifier blocks in this circuit are similar to the blocks in the 10 dB Gain Steps circuit. The block is a three-transistor circuit using a differential pair connected to an emitter-follower. The gain is controlled by altering the feedback network.

From the 20 dB Gain Steps circuit, the signal is applied through a double-shielded coaxial cable and J683. It is sent through input transformer T2013 to the first amplifier block.

The first block (Q2015, Q2014, and Q1025) has a gain range of 13.5 dB by using a PIN diode (CR2021) in the feedback loop. The bias for this diode comes from an array of variable resistors on the VR mother board #2, with the individual resistor selected by the microcomputer.

The second block is similar except that the gain change occurs in one step of approximately 12.5 dB. This gain step occurs only in the higher bands and is activated by the microcomputer through user-selected diodes on the VR mother board #2.

The output from the second amplifier block is applied through connector EE to the VR 2nd Filter Select circuit.

2nd Filter Select (22)

The VR 2nd Filter Select circuit operates in conjunction with the 1st Filter Select circuit to determine the overall system bandwidth through banks of switched filters that are selectable under control of the analyzer microcomputer. Data bits 0, 1, and 2 from the data bus are applied to decimal decoder U3070, which enables the selected filter by providing a low signal on the appropriate output pin. Bandwidth selections are 1 MHz to 100 Hz in decade steps, with a 30 Hz minimum bandwidth.

Note that, although the 2nd Filter Select circuit is similar to the 1st Filter Select circuit, no 30 Hz switching circuits are included on the board for future use. When 30 Hz resolution is selected, the 30 Hz bandwidth uses the 1 kHz filter in the 2nd Filter Select circuit. This can be seen in the connection between pins 6 and 7 on decimal decoder U3070, thus resulting in line 11 being low for both 1 kHz and 30 Hz bandwidth sections.

The data bits select a filter bandwidth as described in Table 5-5. Filter selection is accomplished as described for the 1st Filter Select circuit.

Table 5-4
GAIN STEP COMBINATIONS

Required Gain Addition	Data Bits			10 dB Gain Steps Circuit		20 dB Gain Steps Circuit			
	2	1	0	Q2043	Pin N	Q1025+Q1035	Pin V	Q1043	Pin Y
10 dB	0	0	1	10 dB	0	0 dB	1	0 db	1
20 dB	1	0	0	0 dB	1	20 dB	0	0 dB	1
30 dB	1	0	1	10 dB	0	20 dB	0	0 dB	1
40 dB	1	1	1	10 dB	0	20 dB	0	10 db	0

Thus, the signal from the Band Leveling circuit via jumper EE is applied through the selected filter and transmitted to the Post VR Amplifier circuit via jumper JJ. Nominal loss through the filter circuit is approximately 14 dB, with internal adjustment compensation for slight variations among the filters. The output level is nominally −16 dBm.

Switching in the other, non-selected filter sections, is accomplished as described in the 1st Filter Select circuit paragraphs. Also as described in those paragraphs, the design of the filter for each bandwidth is determined by the requirements for each band and ranges from no filter at all to a complex two crystal arrangement. An important design difference is that the 2nd Filter Select circuit contains a variable resistor in the attenuator that follows the input switch in all except the 100 kHz circuit. The purpose of this adjustment is to allow calibration of all other circuits to match the 100 kHz circuit. Thus, the calibration is required only to remove variations between the filters by adjustments R1065, R3035, R3025, and R3015.

It is in the 1 MHz section that no filter is used. This is because this circuit section is preceded by the 1 MHz (wide) filter between the 2nd and 3rd Converters and the 1.2 MHz filter in the VR Input circuit. Those filters accomplish the required function. Thus, instead of a filter, an attenuator that includes the calibration adjustment is contained in the 1 MHz selection circuit. This attenuator compensates (offsets) the gain loss associated with a filter in the other resolution circuits.

The 100 kHz filter is a double-tuned LC circuit that is designed for a good time-domain response shape. Variable capacitors C2050 and C5055 provide for filter tuning. A 6 dB attenuator (resistors R2048, R2047, and R2049) is included at the filter input. This attenuator and the filter form a reference to which the levels of the other circuits are calibrated. Impedance matching is accomplished at both input and output by series capacitors C1047 and C6052.

The 10 kHz filter uses a two-pole monolithic crystal filter. The impedances at the input and output are matched to 50 Ω by T4044 and T7050. An attenuator that contains the calibration adjustment is included at the filter input for filter variation compensation.

The 1 kHz filter also uses a two-pole monolithic crystal filter with impedance matching transformers T4030 and T7038 at the input and output. An attenuator that contains the calibration adjustment is included at the filter input for filter variation compensation.

The 100 Hz filter uses a pair of high-Q crystals in a balanced two-pole ladder configuration. These crystals are matched for both frequency and temperature characteristics. Input and output impedance matching is accomplished primarily by transformers T4019 and T7015. Two small capacitors in the same transformer circuit as the crystals (C6011 and C7011) are adjustable to cancel the parallel capacitance effect of the crystals. An attenuator that contains the calibration adjustment is included at the filter input for filter variation compensation.

Table 5-6

PROGRESSION OF GAIN REDUCTION

Input Level	Point 1	Point 2	Point 3	Point 4
		Beyond Logging Range		
X − 10 dB	0.00316	0.01	0.0316	0.1
				0.216
X Level	0.01	0.0316	0.1	0.316
				0.684
X + 10 dB	0.0316	0.1	0.316	1.0
			0.684	0.684
X + 20 dB	0.1	0.316	1.0	1.684
		0.684	0.684	0.684
X + 30 dB	0.316	1.0	1.684	2.368
	0.684	0.684	0.684	0.684
X + 40 dB	1.0	1.684	2.368	3.052
X + 50 dB	3.16	Beyond Logging Range		

Post VR Amplifier (22)

The Post VR Amplifier circuit provides the final VR system gain to bring the signal to the required output level and provides the final bandpass filtering to assure clean performance. The circuit consists of two stages of gain followed by a filter.

From the 2nd Filter Select circuit, the signal is applied through jumper JJ to the input of common emitter amplifier transistor Q2056. The circuit includes potentiometer R2038 in the emitter circuit to allow for adjusting the post VR amplifier gain. The output is transformer coupled by T1059 to the base of feedback amplifier transistor Q1048. This circuit includes emitter degeneration through resistor R2042 and collector-to-base feedback through resistor R1052. The collector feedback is used in this instance to help provide a well-defined output impedance of 50 Ω. Input impedance to this stage is defined by transformer T1059 and resistor R1058 across the primary.

This final VR amplifier stage is biased for relatively high output current. This is required because the VR system is sometimes driven at an increased output level of +10 dBm, and more current is required to prevent gain compression. A higher output level is required in low noise or low intermodulation distortion operation to compensate for the 10 dB of gain that is switched out of the Log Amplifier.

From the final amplifier, the signal is applied through the 1.2 MHz bandpass filter that consists of capacitors C2033 and C2018 and the components between. This filter is a double-tuned design and has an insertion loss of approximately 2 dB.

As an aid to understanding the overall VR system functions, it is helpful to understand some aspects of filter design. When designing a wide-bandpass filter, on the order of ten percent or greater, stop-band attenuation becomes a severe problem in two-pole filters. The result is that a given filter design will degenerate into either a high-pass or a low-pass filter. The design of the filter in the Post VR Amplifier circuit degenerates into a low-pass unit. However, since the VR system includes a bandpass filter at both the input and the output, and since the input filter in the VR Input circuit degenerates into a high-pass unit, the overall VR system exhibits clean stop-band performance.

The output signal from the filter is applied through coaxial connector J682 to the Log Amplifier. The output level is nominally at 0 dBm.

Digital Control (21)

The Digital Control circuits provide address and data decoding for the bandwidth and gain step selection and provide the control signals to the other sections of the VR system to accomplish those tasks.

Address and data valid lines from the analyzer address bus are applied to address decoder U4022 through connector P1049 pins 9, 10, 12, 13, 14, and 20. Data bit 7 is also applied through P1049 pin 7 as a supplemental address bit to select between the latch that stores data for bandwidth selection, and the latch that stores data for band identification and gain step selection.

Data lines from the analyzer data bus are applied through connector P1044 pins 1, 2, 3, 4, 5, 6, and 8 to data latches U3010 and U3017. Note that only data bits 0, 1, and 2 are applied to latch U3010.

Latch U3010 stores the data that selects among the filters in the 1st and 2nd Filter Select circuits. Outputs from pins 2, 19, and 16 of U3010 are applied to the decimal decoders in the filter select circuits through edge connector pins G, F, and E to control the filter selection. Decoding is done within the filter select circuits because it results in fewer lines between circuits and provides extra buffering to reduce noise transmission between circuits.

Latch U3017 stores the data that select among the various gain steps. Outputs from pins 2, 5, and 6 (corresponding to data bits 0, 1, and 2) are applied to inverter transistors Q4035, Q3035, and Q4037, respectively. From Q4035, the output signal is applied through connector P1049 pin 32 to the 10 dB Gain Steps circuit to control gain switching. From Q3035, the output signal is applied through edge connector pin 25 to the 20 dB Gain Steps circuit to control switching of the 10 dB gain switch; from Q4037, the output signal is applied through edge connector pin 27 to the 20 dB Gain Steps circuit to control switching of the 20 dB gain step.

5 Volt Regulator

The 5 Volt Regulator circuit (U3041) supplies the required 5 volt source for use in several sections of the VR system. This is required because of noise in the 5 volt supply.

LOGARITHMIC AMPLIFIER AND DETECTOR 23

Refer to the block diagram adjacent to Diagram 23. The Logarithmic (Log) Amplifier and Detector accepts input signals from the VR circuits, with a dynamic range to 90 dB. It then amplifies these signals so the output is proportional to the logarithm of the input, and applies the signals to a linear detector to produce the video output signal. By controlling the compression curve characteristics, each dB of change in the input signal level results in an equal increment of change in the output. Thus, in the 10 dB/division mode, each division of displacement on the screen represents 10 dB of input signal level change.

Log Amplifier

The Log Amplifier circuits logarithmically amplify the input signal from the VR circuits and apply the output signal to the Detector circuit. These circuits consist of seven ac coupled amplifier stages. Each stage has two gain values that depend on signal amplitude. In addition, the first three stages have an extra automatically selected gain value. The combined circuits provide high gain for low-level signals and low gain for high-level signals. For the output signal to be proportional to the logarithm of the input, more gain is required for a change from −90 dBm to −89 dBm than a change from −1 dBm to 0 dBm. Thus, for a given stage of the seven, the gain starts at approximately 10 dB for a low-level signal and decreases to unity as the input signal level increases. In the first three stages, the gain becomes less than unity as the signal amplitude further increases.

Input signal levels nominally range between −90 dBm and 0 dBm. As the signal level increases, the gain decrease begins with the final stage and proceeds in succession back through the remaining six stages to the first. Since each stage produced approximately 10 dB of gain initially, and that gain was reduced to unity, the total gain reduction is 70 dB. With further increases in input signal level, three more gain change steps take place. The gain of the first three stages is reduced below unity approximately 7 dB for each stage. This reduction starts with the first stage and proceeds to the third, to provide an additional gain reduction of approximately 20 dB.

Thus, as the input signal increases from −90 dBm to +10 dBm, the gain through the amplifier decreases logarithmically so that the output signal is exactly proportional to the logarithm of the input. This is accomplished through a system of series diode limiting in each stage, with a second set of diodes for extra limiting in each of the first three stages. Refer to Diagram 23 while reading the following.

The following description of a simple three-stage log amplifier with one gain step in each stage is provided as an aid to understanding the concept of a logarithmic amplifier. For the example amplifier shown in the following three figures and described in the text, the gain of each stage is 3.16 V (10 dB) up to an output level of 1 volt peak, then unity for output levels greater than 1 volt peak; that is, each stage uses one breakpoint. The breakpoint voltage is used for ease of illustration; the actual breakpoint voltage is significantly lower.

Figure 5-5 illustrates the amplifier and the input signal source. For purposes of discussion, assume that the source has a step attenuator at the output that will allow incrementing the input signal in 10 dB steps. Table 5-5 shows the progression of gain reduction above 1 volt at each amplifier stage output. Note that with each input level change of 10 dB, the output change at point 4 is 0.684 volt. The gain curve for one stage is illustrated in Fig. 5-6. Also note, when the level at point 1 is increased beyond 1 volt it is beyond the logging range of the amplifier. Similarly, if the input level is decreased 10 dB below the nominal minimum input level, the output increment is different. A curve of the ends of the logging range is shown in Fig. 5-7.

From the VR circuits, the signal is applied to input preamplifier Q3105 in the Log Amplifier circuits through coaxial connector P621. The input preamplifier provides transfer from 50 Ω input to the high impedance input of the 1st amplifier stage. The input signal is also applied to transistor Q2105, a common-base amplifier, that acts as a buffer to supply the 10 MHz IF signal to the rear panel connector.

From the input preamplifier, the signal is applied to the first of seven cascaded amplifiers that consist of Q3100/Q1095, Q3090/Q1080, Q3075/Q1020, Q3055/Q1050, Q3045/Q1035, Q3030/Q1025, and Q3015/Q6010, plus the associated circuitry. These stages are similar, except that the first three contain an extra set of diodes for a second gain step. The following description of the last stage is typical. The second step gain change in the first three stages is described afterward.

When the input level to transistor Q3015 is less than approximately 60 millivolts peak-to-peak, the transistor conducts enough to maintain forward bias on both series limiting diodes, CR4015 and CR4012. The RF signal path at that level is through the diodes, capacitor C5014, and resistors R4010H, R4010B, R4015, and R4010D, to common-base amplifier Q6010. The gain of the stage is approximately 10 dB under these conditions. As the input signal voltage increases, more current flows through CR4015, to increase the reverse bias of CR4012. This sharply reduces the stage gain to unity. The signal current

then flows only in R4010B, R4015, and R4010D. This change takes place during the positive-going portion of each cycle. The opposite occurs during the negative-going portion of the signal above the minimum input level. As the input signal increases beyond the point at which the gain of the final stage decreases to unity, the same sequence occurs in the preceding stage, Q3030/Q1025, and so on in succession, back to the first stage, Q3100/Q1095.

Signal levels above this point activate the second tier of gain reduction in the first three stages. Each stage incorporates a second set of diodes that reduces the gain by another 7 dB. In the first tier of gain reduction, reduction started at the last stage and proceeded to the first; in the second tier, the reduction starts at the first stage and proceeds to the third.

In the first stage, diodes CR3089 and CR2087, are forward biased when the stage is in the unity gain mode. Limiting occurs in the same manner as described above with a further increase in input signal level, and results in less than unity gain through the stage (approximately 1/3). The one, two, three reduction sequence is established by the values of pull-down resistors R3082, R2076, and R2066.

Detector

The Detector circuit detects and filters the Log Amplifier circuit output signal and produces the VIDEO signal that is transmitted to the Video Amplifier circuits. The circuit consists of an operational amplifier with a diode detector in the feedback path and a low-pass filter at the output.

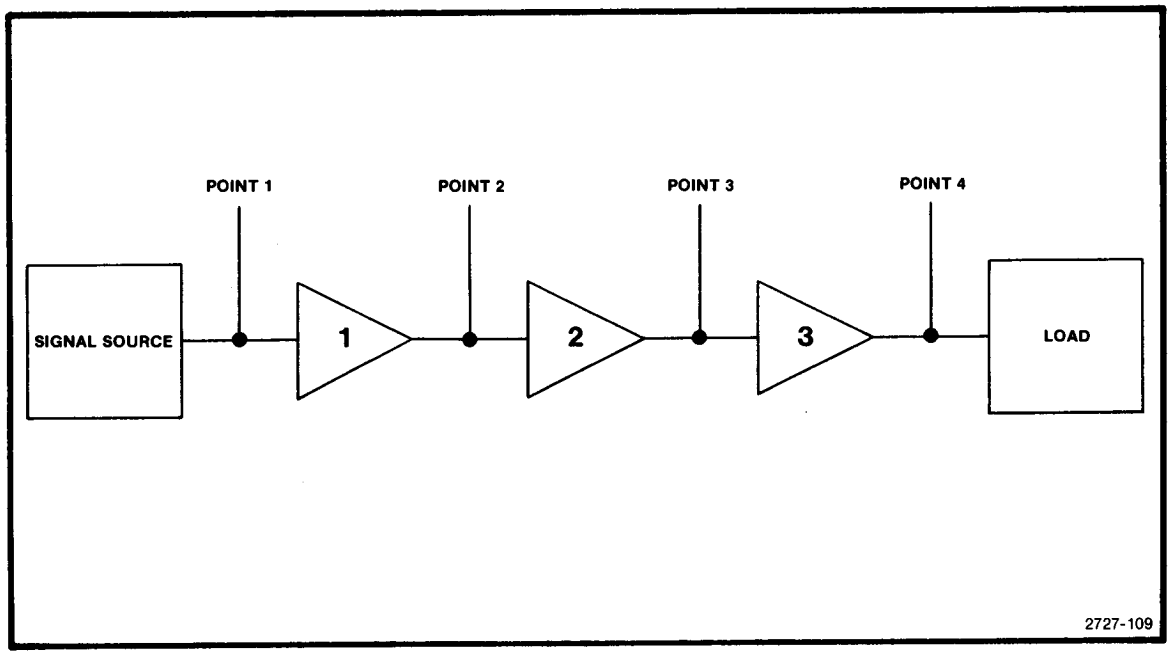


Fig. 5-5. Three-stage log amplifier.

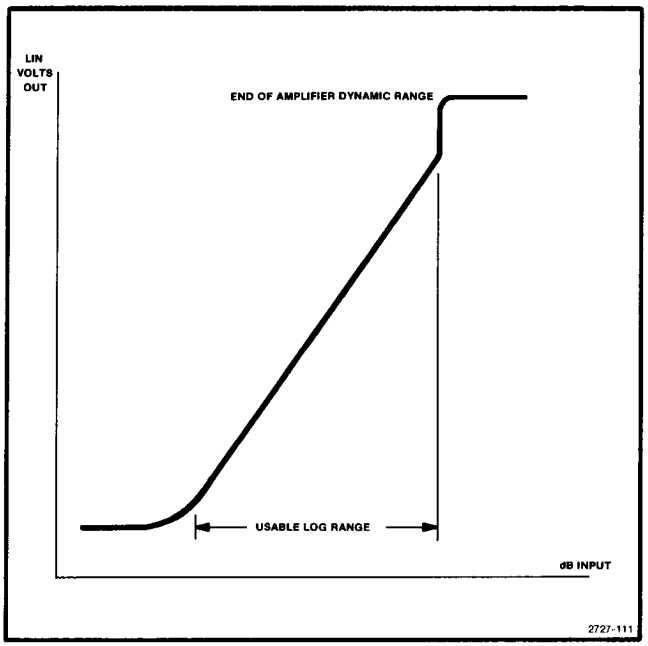


Fig. 5-6. Log amplifier gain curve showing breakpoint.

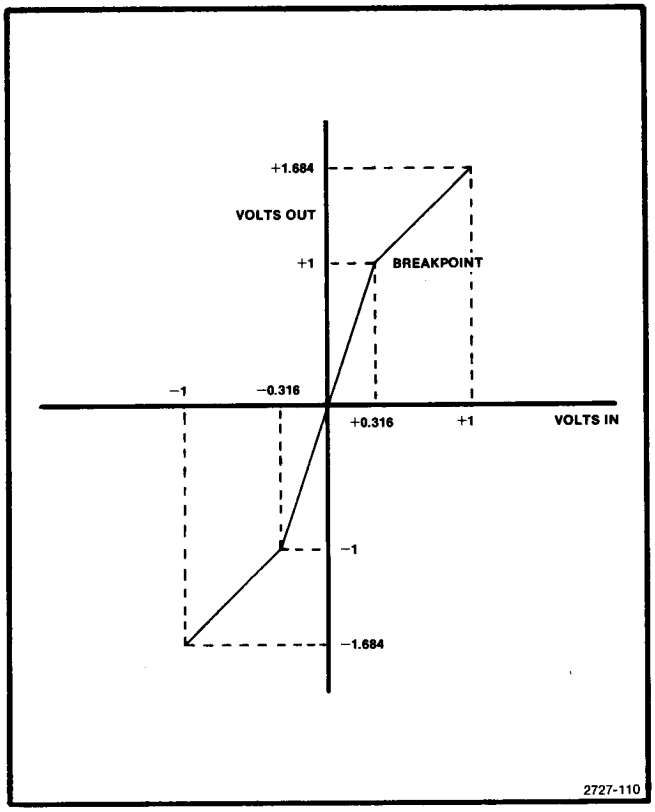


Fig. 5-7. Ends of logging range.

Actually, the circuit called an operational amplifier is not easily recognized as such. It is made up of grounded emitter amplifier Q4025 and a differential amplifier consisting of Q4030 and Q4035. The summing node for the negative input is the base of Q4025 (the positive input is at the grounded emitter of Q4025). Also, the differential amplifier is designed for high impedance output to allow the current that is available from Q4025 to drive the operational amplifier very rapidly during the period when both detector diodes (CR5033 and CR5027) are effectively open circuited; that is, when the output is near 0 volt. When neither diode is conducting, it is necessary that the output change rapidly through that zone. Note that the network consisting of resistors R5032, R5029, R5020, and capacitor C5029 is included to stabilize the dc operating point.

Figure 5-8 shows a simplified schematic diagram of the detector circuit. As shown in this diagram, two detector diodes (CR5033 and CR5027) are used, but only the positive half cycle is taken as the output (from CR5027). The output from the collector of transistor Q4035 is applied to the diodes through capacitor C5035. Ac coupling is used on both sides of the detector to prevent temperature coefficient effects of the operational amplifier from affecting the detector output. This isolation provides that the detector charges and discharges capacitors C5035 and C5024 by the current induced in each half cycle of the signal without changing voltage level.

This detector operates as an area (average) detector despite the fact that the Log Amplifier circuits operate on peak principles. It is possible to use an average detector because of some very selective tailoring in the Log Amplifier circuits. For instance, resistor example R5021 in the final log amplifier stage is sized to reduce the amount of current standing in the final stage output diodes, thus tapering the curve very slightly to improve linearity at the lower end of the curve. Log Gain adjustment R4020, in the final amplifier stage, is adjusted for increased linearity at the top of the curve.

As shown in the diagram, the positive-going output signal, from the detector, is applied through a low-pass filter consisting of capacitors C7024, C7014, C7021, C7011, and inductors L6011, L8021, to the Video Amplifier.

6 DISPLAY SECTION

FUNCTIONAL DESCRIPTION

The display section performs several functions:

1) it accepts the VIDEO signal from the IF section, and processes the signal, and provides the vertical crt plate drive signals;

2) it processes the sweep voltages from the sweep section and produces the horizontal crt plate drive voltage. If Digital Storage is selected, vertical and horizontal signals are further processed by that circuit group;

3) it accepts character information from the instrument data bus and generates crt plate drive signals to display alpha and numeric characters;

4) it accepts control levels from front panel beam controls and generates unblanking signals to control display presence, brightness, and focus.

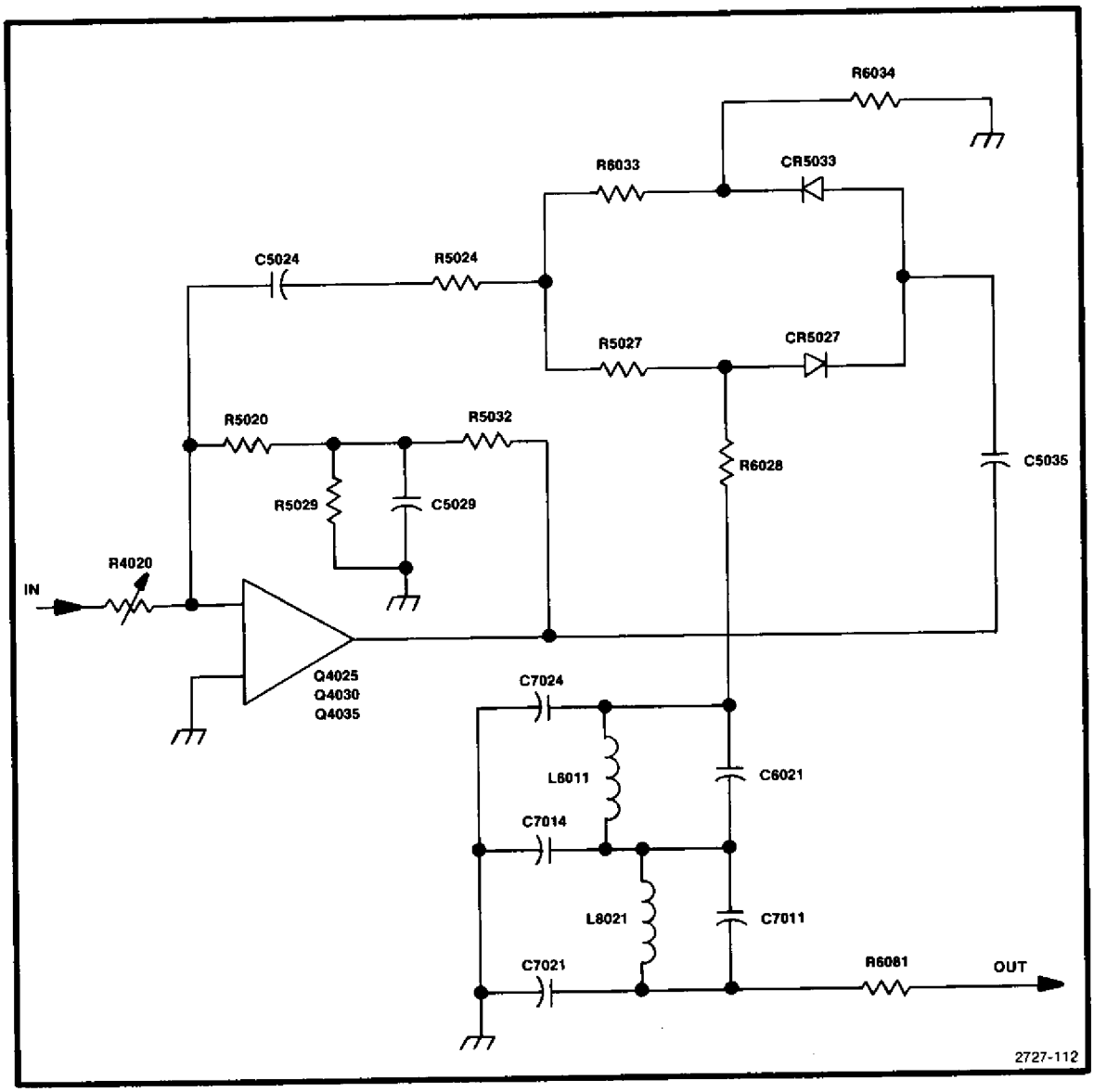


Fig. 5-8. Simplified detector circuit.

The 10 MHz output from the center tap of T1053 is applied through a diplexer and coaxial connector J3057 to the Variable Resolution circuits. Loss through the mixer is typically 6 dB.

Calibration Output Amplifier

The calibrator output amplifier is a differential amplifier (Q2031 and Q1031) that is overdriven. With low levels of drive, this amplifier would operate as a small-signal amplifier. However, with the higher positive and negative levels from reference amplifier Q2016, the transistors are either driven hard or are not conducting at all. Since the transistors are overdriven, the current in the output side (Q1031) is the dc bias current when that side is conducting. Changing the bias current will therefore change the output voltage. Thus, the output is determined by internal dc levels, not input signal levels. Potentiometer R1045 provides for adjustment of that quiescent current.

The output frequency is stable and rich in harmonics. Thus, it provides a useful signal comb of 100 MHz markers to approximately 2 GHz. At 100 MHz, the output level is set by R1045 for −20 dBm which is applied to the front panel CAL OUT connector through coaxial connector J1015.

5 IF SECTION

The IF section receives the 10 MHz IF signal from the 3rd Converter, establishes the system resolution through selective filtering, levels the gain for all bands, and logarithmically amplifies and detects the signal to produce the video output to the Display section.

System resolution is selectable, under microcomputer control, among six bandwidths: 1 MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz, and 30 Hz. This selection is done in the Variable Resolution circuit block by two sets of filters. Bandpass filters are also included at the circuits input and output.

Significant gain is provided in the resolution circuit block by several stages of amplification. Also, the capability to add other gain steps under microcomputer control is provided by switching amplifier gain. These amplifiers, by being switched in combination, provide for 10, 20, 30, or 40 dB of additional gain.

In order that each division of signal change on the crt screen be equal to that for each other division and be equvalent to a similar signal level change in dB, a logarithmic amplification of the signal is required. This is done by a seven stage amplifier that produces an output that is proportional to the logarithm of the input. Thus, the screen displacement can be selectable as to amount of change per divisions, and can be proportional to the input level change. For instance, in the 10 dB per division mode, each division of displacement in the screen represents a signal level change of 10 dB regardless of whether it is at the top or bottom of the screen.

Following the logarithmic amplifier, an area detector produces a positive-going pulse output that is applied to the display section as the VIDEO signal.

Variable Resolution Circuits

20 21 22

The Variable Resolution (VR) circuits provide selection of resolution bandwidth under microcomputer control, and approximately 35 dB of system gain. It consists of two sets of filters and various gain leveling stages. Since the input to the VR circuits is nominally at −35 dBm and the Log Amplifier input must be 0 dBm for full screen, the VR circuits must provide the gain difference. Also, additional gain is required for operation in the 2 dB/DIV or the linear mode.

Physically, the VR section consists of two sub-assemblies that plug onto the analyzer mother board. The input circuits are in one sub-assembly; the output section and digital interface are in the other. Each of the sub-assemblies consists of boards that plug onto a four-layer mother board with a ground plane on both outside layers. Only power supply and control voltages travel through the mother board. All signal interconnection is via coaxial cable.

Circuits for the VR section are contained on three diagrams: 20, 21, and 22. The following paragraphs describe the circuits.

Input 20

The VR Input circuit receives the nominal −35 dBm 10 MHz signal from the 3rd Mixer through J693. This signal is applied to a two-pole, 1.2 MHz bandpass filter that augments the 1 MHz filter that precedes the 3rd Mixer and provides initial selectivity. This 1.2 MHz filter includes C1037 and C1031 and all of the components between. Filter tuning is provided by variable capacitors C1033 and C1026.

From the filter, the signal is applied to broadband feedback amplifier Q1023, which is biased at a relatively substantial output current (approximately 50 mA) to exhibit good intermodulation distortion performance. This performance is provided primarily through the large current capacity, by negative feedback through resistor R1025 and by emitter degeneration resistor R1023.

At the output of amplifier Q1023 is a 6 dB attenuator that provides a clean 50 Ω output to the 1st Filter Select circuits and reflects a 50 Ω termination back through the amplifier for proper termination of the 1.2 MHz bandpass filter. The output signal is transmitted via jumper B.

1st Filter Select 20

The VR 1st Filter Select circuit operates in conjunction with the 2nd Filter Select circuit to determine the overall system bandwidth through banks of switched filters that are selectable under control of the analyzer microcomputer. Data bits 0, 1, and 2 from the data bus are applied to decimal decoder IC U4035, which enables the selected filter by providing a low signal on the appropriate output pin. Bandwidth selections are 1 MHz to 100 Hz in decade steps with 30 Hz as the minimum bandwidth. The data bits select a filter bandwidth according to the following table.

Table 5-3
BANDWIDTH SELECTION

DB0	DB1	DB2	Bandwidth
1	0	0	1 MHz
0	1	0	100 kHz
1	1	0	10 kHz
1	0	0	1 kHz
1	0	1	100 Hz
0	1	1	30 Hz

Selection of filters is done by PIN diode switching. At the input and output of each filter is a series and a shunt diode. When a filter is selected, the series diodes are biased on and the shunt diodes are biased off. For the filters that are not selected (only one is on at a time), the diode conditions are opposite. Since the switching operation is the same for all filters, the following description of the 100 kHz filter selection is applicable to all with appropriate component designators.

If we assume a content of 010 for the three data bits, line 2 from U4035 will be low. This will turn on transistors Q3019 and Q3055, which operate as dc switches. With input switch Q3019 turned on, the current path is through R4012, L3012, CR3010, L3013, R3014, and Q3019. This current is determined by decoupling resistor R3014 and resistor R4012, which is common to all filters, and is sufficient to turn CR3010 on enough that it appears to be merely a resistor to RF. At the same time, the voltage drop across R4012 is sufficient to reverse-bias CR3012. The same operational situation exists for the filter output switch, Q3055. Resistors R3057 and R1067 establish the current to forward-bias CR3061 and reverse-bias CR3060.

Thus, the signal from the Input circuit via jumper B is applied through the selected filter and transmitted to the 10 dB Gain Steps circuit via jumper K. Nominal loss through the filter circuit is approximately 6 dB, with slight variations among the filters.

In the non-selected filter sections, the input and output switch transistors are turned off by the high outputs from decimal decoder U4035. The collectors are pullled toward −15 V by pulldown resistors, thus forward biasing the shunt diodes (input: CR3014, CR2013, CR2011, CR1013, and CR1011; output: CR3062, CR2066, CR2055, CR1055, and CR4065). Since one filter is always selected, the voltage drop across the common input and output resistors (R4012 and R1067, respectively) provides for back biasing the series diodes (input: CR3011, CR3012, CR2010, CR1012, and CR1010; output: CR4068, CR2062, CR2059, CR1059, and CR4064). Note that input and output switching is provided on the board for future use with 30 Hz resolution.

Design of the filter for each bandwidth is determined by the requirements of each band and ranges in complexity from no filter at all to a complex two-crystal arrangement.

In the 1 MHz section no filter is used, because this circuit section is preceded by two filters that accomplish the required function. The first is the 1 MHz filter between the 2nd and 3rd Converters; the second is the 1.2 MHz filter in the VR Input circuit. Instead of a filter, a 6 dB attenuator is contained in the 1 MHz selection circuit. This attenuator provides initial leveling to compensate for absence of filter loss.

The 100 kHz filter is a double-tuned LC circuit that is designed for a good time-domain response shape. Variable capacitors C3023 and C3035 provide for input and output adjustments. Impedance matching is accomplished at both input and output by series capacitors C3020 (input) and C3048 (output).

The 10 kHz filter uses a pair of two-pole monolithic crystal filters that are interconnected by variable shunt capacitor C2037. Input and output impedances are matched with broadband transformers T3026 and T3055. A 3 dB attenuator, consisting of R2027, R2026, and R2028, is included at the filter input.

The 1 kHz resolution filter consists of a single two-pole monolithic crystal filter, matched to the 50 Ω impedance with broadband transformers T2035 and T2055. A 2 dB attenuator, consisting of R2024, R2023, and R2025 is also part of the filter.

The 100 Hz filter uses a pair of high Q crystals in a balanced two-pole ladder configuration. These crystals are matched for both frequency and temperature characteristics. Input and output impedance matching is accomplished primarily by transformers T1025 and T1039. Two small capacitors in the same transformer circuit as the crystals (C1030 and C1035) are adjustable to cancel the parallel capacitance effect of the crystals. Also, a 2 dB attenuator is included at the filter input and consists of resistors R1026, R1028, and R1027.

The 30 Hz filter uses three matched high-Q crystals in a three-pole unbalanced ladder configuration. A small oven with thermal feedback keeps the crystals at a constant temperature while the instrument is operating. The filter is terminated with 50 Ω at both the input and output.

10 dB Gain Step 

The 10 dB Gain circuit provides 10 dB of signal gain when selected by the microcomputer. The circuit consists of three stages of amplification, one stage provides variable gain, the other two are fixed gain steps. The nominal input signal level from the 1st Filter Select circuit is −26 dBm for a resolution bandwidth of 100 kHz. (All levels listed in this description relate to the 100 kHz resolution.)

The input signal is applied through an impedance transformer, T3019, to the first amplifier stage consisting of a differential pair (Q3016 and Q2027) and an emitter follower output amplifier (Q1036). Negative feedback through R1031 and R2051, provide gain stabilization. An output resistor, R2035, increases the output impedance of the composite amplifier to approximately 50 Ω.

Gain of the input stage is fixed for all resolution bandwidths except 30 Hz. The gain for 30 Hz is set to a precise level by activating Q2015. Transistor Q2015 is biased on by a low on pin L. This adds R2025 (30 Hz level) across feedback resistor R2051. Adjustment R2025 sets the gain of the stage.

The output from the 1st stage is then applied to a common emiter stage (Q2043). Gain of this stage, when transistor Q4039 is turned on, is 10 dB. When the base of Q4039 is pulled low by data bit 0 from Q4035 on the VR mother board #1, the transistor saturates and shunts the emitter load resistor R3048 with R3038 and the 10 dB Gain adjustment R3035.

The output of Q2043 drives the input of the third amplifier stage. This stage operates the same as the first stage except for gain variation. Feedback resistor R1060 is shunted by PIN diode CR1053. As the current through the diode increases, the resistance decreases and the gain of the stage increases. Gain control of the stage is established by the setting of the front panel AMPL CAL adjustment. Gain range is about 14 dB.

Output impedance of the stage is 50 Ω, set by resistor R1064. Nominal output level is −5 dBm for a full screen display. This level may be as high as +5 dBm when MIN NOISE is active. 10 dB of gain is also removed from the Log Amplifier to reduce the noise level and must be supplied by the VR section.

20 dB Gain Steps 

The 20 dB Gain Steps circuit provides −6 dB, +4 dB, +14 dB, and +24 dB of gain in precise 10 dB steps. The nominal −5 dBm input is supplied through pin P from the 10 dB Gain Steps circuit. This signal is applied to a chain of three common-emitter amplifiers, each using emitter degeneration. Changing the emitter resistance is used to change amplifier gain under the direction of the microcomputer.

The nominal gain of the complete circuit is −6 dB, with Q2018, Q2042 and Q1062 biased off. This provides a nominal −11 dBm output. In this condition, control pins V and Y are high, causing switching transistors Q2018, Q2042, and Q1062 to be cut off.

When pin V is low, Q2018 and Q2042 are saturated, raising the total gain of the first two amplifiers 20 dB. Variable resistor R2025 is used to adjust the gain shift of the first stage (Q1025) while the gain shift of the second stage (Q1035) is fixed at +10 dB. This adjustment allows the gain shift to be exactly set to +20 dB.

When pin Y is low, Q1062 is saturated, raising the gain of the third amplifier (Q1043) by 10 dB. Variable resistor R1063 allows the gain shift to be exactly set to +10 dB.

Data bits 2, 1, and 0 control the gains of the 10 dB Gain Steps circuit and the 20 dB Gain Steps circuit. Bit 2 controls pin V, bit 1 controls pin Y, and bit 0 controls pin N. The data is decoded and stored in latches on the VR mother board #2. Table 5-4 shows the state of bits 2, 1, and 0 and the gain shifts of amplifier stages Q2043, Q1025, Q1035, and Q1043.

The output of the 20 dB Gain Steps circuit is attached to coaxial connector J2031. The signal is routed through a double coaxial cable to the Band Leveling circuit.

Band Leveling (21)

The two amplifiers in the VR Band Leveling circuit correct the gain variations caused by the front end.

The output level of this board is −2 dBm while the nominal input is −11 dBm. This input level occurs at 100 kHz resolution in Min Distortion mode.

The two amplifier blocks in this circuit are similar to the blocks in the 10 dB Gain Steps circuit. The block is a three-transistor circuit using a differential pair connected to an emitter-follower. The gain is controlled by altering the feedback network.

From the 20 dB Gain Steps circuit, the signal is applied through a double-shielded coaxial cable and J683. It is sent through input transformer T2013 to the first amplifier block.

The first block (Q2015, Q2014, and Q1025) has a gain range of 13.5 dB by using a PIN diode (CR2021) in the feedback loop. The bias for this diode comes from an array of variable resistors on the VR mother board #2, with the individual resistor selected by the microcomputer.

The second block is similar except that the gain change occurs in one step of approximately 12.5 dB. This gain step occurs only in the higher bands and is activated by the microcomputer through user-selected diodes on the VR mother board #2.

The output from the second amplifier block is applied through connector EE to the VR 2nd Filter Select circuit.

2nd Filter Select (22)

The VR 2nd Filter Select circuit operates in conjunction with the 1st Filter Select circuit to determine the overall system bandwidth through banks of switched filters that are selectable under control of the analyzer microcomputer. Data bits 0, 1, and 2 from the data bus are applied to decimal decoder U3070, which enables the selected filter by providing a low signal on the appropriate output pin. Bandwidth selections are 1 MHz to 100 Hz in decade steps, with a 30 Hz minimum bandwidth.

Note that, although the 2nd Filter Select circuit is similar to the 1st Filter Select circuit, no 30 Hz switching circuits are included on the board for future use. When 30 Hz resolution is selected, the 30 Hz bandwidth uses the 1 kHz filter in the 2nd Filter Select circuit. This can be seen in the connection between pins 6 and 7 on decimal decoder U3070, thus resulting in line 11 being low for both 1 kHz and 30 Hz bandwidth sections.

The data bits select a filter bandwidth as described in Table 5-5. Filter selection is accomplished as described for the 1st Filter Select circuit.

Table 5-4
GAIN STEP COMBINATIONS

Required Gain Addition	Data Bits			10 dB Gain Steps Circuit		20 dB Gain Steps Circuit			
	2	1	0	Q2043	Pin N	Q1025+Q1035	Pin V	Q1043	Pin Y
10 dB	0	0	1	10 dB	0	0 dB	1	0 db	1
20 dB	1	0	0	0 dB	1	20 dB	0	0 dB	1
30 dB	1	0	1	10 dB	0	20 dB	0	0 dB	1
40 dB	1	1	1	10 dB	0	20 dB	0	10 db	0

Thus, the signal from the Band Leveling circuit via jumper EE is applied through the selected filter and transmitted to the Post VR Amplifier circuit via jumper JJ. Nominal loss through the filter circuit is approximately 14 dB, with internal adjustment compensation for slight variations among the filters. The output level is nominally −16 dBm.

Switching in the other, non-selected filter sections, is accomplished as described in the 1st Filter Select circuit paragraphs. Also as described in those paragraphs, the design of the filter for each bandwidth is determined by the requirements for each band and ranges from no filter at all to a complex two crystal arrangement. An important design difference is that the 2nd Filter Select circuit contains a variable resistor in the attenuator that follows the input switch in all except the 100 kHz circuit. The purpose of this adjustment is to allow calibration of all other circuits to match the 100 kHz circuit. Thus, the calibration is required only to remove variations between the filters by adjustments R1065, R3035, R3025, and R3015.

It is in the 1 MHz section that no filter is used. This is because this circuit section is preceded by the 1 MHz (wide) filter between the 2nd and 3rd Converters and the 1.2 MHz filter in the VR Input circuit. Those filters accomplish the required function. Thus, instead of a filter, an attenuator that includes the calibration adjustment is contained in the 1 MHz selection circuit. This attenuator compensates (offsets) the gain loss associated with a filter in the other resolution circuits.

The 100 kHz filter is a double-tuned LC circuit that is designed for a good time-domain response shape. Variable capacitors C2050 and C5055 provide for filter tuning. A 6 dB attenuator (resistors R2048, R2047, and R2049) is included at the filter input. This attenuator and the filter form a reference to which the levels of the other circuits are calibrated. Impedance matching is accomplished at both input and output by series capacitors C1047 and C6052.

The 10 kHz filter uses a two-pole monolithic crystal filter. The impedances at the input and output are matched to 50 Ω by T4044 and T7050. An attenuator that contains the calibration adjustment is included at the filter input for filter variation compensation.

The 1 kHz filter also uses a two-pole monolithic crystal filter with impedance matching transformers T4030 and T7038 at the input and output. An attenuator that contains the calibration adjustment is included at the filter input for filter variation compensation.

The 100 Hz filter uses a pair of high-Q crystals in a balanced two-pole ladder configuration. These crystals are matched for both frequency and temperature characteristics. Input and output impedance matching is accomplished primarily by transformers T4019 and T7015. Two small capacitors in the same transformer circuit as the crystals (C6011 and C7011) are adjustable to cancel the parallel capacitance effect of the crystals. An attenuator that contains the calibration adjustment is included at the filter input for filter variation compensation.

Table 5-6

PROGRESSION OF GAIN REDUCTION

Input Level	Point 1	Point 2	Point 3	Point 4	
		Beyond Logging Range			
X 10 dB	0.00316	0.01	0.0316	0.1	0.216
X Level	0.01	0.0316	0.1	0.316	0.684
X + 10 dB	0.0316	0.1	0.316	1.0	0.684
X + 20 dB	0.1	0.316	1.0 (0.684)	1.684	0.684
X + 30 dB	0.316	1.0 (0.684)	1.684 (0.684)	2.368	0.684
X + 40 dB	1.0 (0.684)	1.684 (0.684)	2.368 (0.684)	3.052	0.684
X + 50 dB	3.16	Beyond Logging Range			

Post VR Amplifier (22)

The Post VR Amplifier circuit provides the final VR system gain to bring the signal to the required output level and provides the final bandpass filtering to assure clean performance. The circuit consists of two stages of gain followed by a filter.

From the 2nd Filter Select circuit, the signal is applied through jumper JJ to the input of common emitter amplifier transistor Q2056. The circuit includes potentiometer R2038 in the emitter circuit to allow for adjusting the post VR amplifier gain. The output is transformer coupled by T1059 to the base of feedback amplifier transistor Q1048. This circuit includes emitter degeneration through resistor R2042 and collector-to-base feedback through resistor R1052. The collector feedback is used in this instance to help provide a well-defined output impedance of 50 Ω. Input impedance to this stage is defined by transformer T1059 and resistor R1058 across the primary.

This final VR amplifier stage is biased for relatively high output current. This is required because the VR system is sometimes driven at an increased output level of +10 dBm, and more current is required to prevent gain compression. A higher output level is required in low noise or low intermodulation distortion operation to compensate for the 10 dB of gain that is switched out of the Log Amplifier.

From the final amplifier, the signal is applied through the 1.2 MHz bandpass filter that consists of capacitors C2033 and C2018 and the components between. This filter is a double-tuned design and has an insertion loss of approximately 2 dB.

As an aid to understanding the overall VR system functions, it is helpful to understand some aspects of filter design. When designing a wide-bandpass filter, on the order of ten percent or greater, stop-band attenuation becomes a severe problem in two-pole filters. The result is that a given filter design will degenerate into either a high-pass or a low-pass filter. The design of the filter in the Post VR Amplifier circuit degenerates into a low-pass unit. However, since the VR system includes a bandpass filter at both the input and the output, and since the input filter in the VR Input circuit degenerates into a high-pass unit, the overall VR system exhibits clean stop-band performance.

The output signal from the filter is applied through coaxial connector J682 to the Log Amplifier. The output level is nominally at 0 dBm.

Digital Control (21)

The Digital Control circuits provide address and data decoding for the bandwidth and gain step selection and provide the control signals to the other sections of the VR system to accomplish those tasks.

Address and data valid lines from the analyzer address bus are applied to address decoder U4022 through connector P1049 pins 9, 10, 12, 13, 14, and 20. Data bit 7 is also applied through P1049 pin 7 as a supplemental address bit to select between the latch that stores data for bandwidth selection, and the latch that stores data for band identification and gain step selection.

Data lines from the analyzer data bus are applied through connector P1044 pins 1, 2, 3, 4, 5, 6, and 8 to data latches U3010 and U3017. Note that only data bits 0, 1, and 2 are applied to latch U3010.

Latch U3010 stores the data that selects among the filters in the 1st and 2nd Filter Select circuits. Outputs from pins 2, 19, and 16 of U3010 are applied to the decimal decoders in the filter select circuits through edge connector pins G, F, and E to control the filter selection. Decoding is done within the filter select circuits because it results in fewer lines between circuits and provides extra buffering to reduce noise transmission between circuits.

Latch U3017 stores the data that select among the various gain steps. Outputs from pins 2, 5, and 6 (corresponding to data bits 0, 1, and 2) are applied to inverter transistors Q4035, Q3035, and Q4037, respectively. From Q4035, the output signal is applied through connector P1049 pin 32 to the 10 dB Gain Steps circuit to control gain switching. From Q3035, the output signal is applied through edge connector pin 25 to the 20 dB Gain Steps circuit to control switching of the 10 dB gain switch; from Q4037, the output signal is applied through edge connector pin 27 to the 20 dB Gain Steps circuit to control switching of the 20 dB gain step.

5 Volt Regulator

The 5 Volt Regulator circuit (U3041) supplies the required 5 volt source for use in several sections of the VR system. This is required because of noise in the 5 volt supply.

LOGARITHMIC AMPLIFIER AND DETECTOR 23

Refer to the block diagram adjacent to Diagram 23. The Logarithmic (Log) Amplifier and Detector accepts input signals from the VR circuits, with a dynamic range to 90 dB. It then amplifies these signals so the output is proportional to the logarithm of the input, and applies the signals to a linear detector to produce the video output signal. By controlling the compression curve characteristics, each dB of change in the input signal level results in an equal increment of change in the output. Thus, in the 10 dB/division mode, each division of displacement on the screen represents 10 dB of input signal level change.

Log Amplifier

The Log Amplifier circuits logarithmically amplify the input signal from the VR circuits and apply the output signal to the Detector circuit. These circuits consist of seven ac coupled amplifier stages. Each stage has two gain values that depend on signal amplitude. In addition, the first three stages have an extra automatically selected gain value. The combined circuits provide high gain for low-level signals and low gain for high-level signals. For the output signal to be proportional to the logarithm of the input, more gain is required for a change from −90 dBm to −89 dBm than a change from −1 dBm to 0 dBm. Thus, for a given stage of the seven, the gain starts at approximately 10 dB for a low-level signal and decreases to unity as the input signal level increases. In the first three stages, the gain becomes less than unity as the signal amplitude further increases.

Input signal levels nominally range between −90 dBm and 0 dBm. As the signal level increases, the gain decrease begins with the final stage and proceeds in succession back through the remaining six stages to the first. Since each stage produced approximately 10 dB of gain initially, and that gain was reduced to unity, the total gain reduction is 70 dB. With further increases in input signal level, three more gain change steps take place. The gain of the first three stages is reduced below unity approximately 7 dB for each stage. This reduction starts with the first stage and proceeds to the third, to provide an additional gain reduction of approximately 20 dB.

Thus, as the input signal increases from −90 dBm to +10 dBm, the gain through the amplifier decreases logarithmically so that the output signal is exactly proportional to the logarithm of the input. This is accomplished through a system of series diode limiting in each stage, with a second set of diodes for extra limiting in each of the first three stages. Refer to Diagram 23 while reading the following.

The following description of a simple three-stage log amplifier with one gain step in each stage is provided as an aid to understanding the concept of a logarithmic amplifier. For the example amplifier shown in the following three figures and described in the text, the gain of each stage is 3.16 V (10 dB) up to an output level of 1 volt peak, then unity for output levels greater than 1 volt peak; that is, each stage uses one breakpoint. The breakpoint voltage is used for ease of illustration; the actual breakpoint voltage is significantly lower.

Figure 5-5 illustrates the amplifier and the input signal source. For purposes of discussion, assume that the source has a step attenuator at the output that will allow incrementing the input signal in 10 dB steps. Table 5-5 shows the progression of gain reduction above 1 volt at each amplifier stage output. Note that with each input level change of 10 dB, the output change at point 4 is 0.684 volt. The gain curve for one stage is illustrated in Fig. 5-6. Also note, when the level at point 1 is increased beyond 1 volt it is beyond the logging range of the amplifier. Similarly, if the input level is decreased 10 dB below the nominal minimum input level, the output increment is different. A curve of the ends of the logging range is shown in Fig. 5-7.

From the VR circuits, the signal is applied to input preamplifier Q3105 in the Log Amplifier circuits through coaxial connector P621. The input preamplifier provides transfer from 50 Ω input to the high impedance input of the 1st amplifier stage. The input signal is also applied to transistor Q2105, a common-base amplifier, that acts as a buffer to supply the 10 MHz IF signal to the rear panel connector.

From the input preamplifier, the signal is applied to the first of seven cascaded amplifiers that consist of Q3100/Q1095, Q3090/Q1080, Q3075/Q1020, Q3055/Q1050, Q3045/Q1035, Q3030/Q1025, and Q3015/Q6010, plus the associated circuitry. These stages are similar, except that the first three contain an extra set of diodes for a second gain step. The following description of the last stage is typical. The second step gain change in the first three stages is described afterward.

When the input level to transistor Q3015 is less than approximately 60 millivolts peak-to-peak, the transistor conducts enough to maintain forward bias on both series limiting diodes, CR4015 and CR4012. The RF signal path at that level is through the diodes, capacitor C5014, and resistors R4010H, R4010B, R4015, and R4010D, to common-base amplifier Q6010. The gain of the stage is approximately 10 dB under these conditions. As the input signal voltage increases, more current flows through CR4015, to increase the reverse bias of CR4012. This sharply reduces the stage gain to unity. The signal current

then flows only in R4010B, R4015, and R4010D. This change takes place during the positive-going portion of each cycle. The opposite occurs during the negative-going portion of the signal above the minimum input level. As the input signal increases beyond the point at which the gain of the final stage decreases to unity, the same sequence occurs in the preceding stage, Q3030/Q1025, and so on in succession, back to the first stage, Q3100/Q1095.

Signal levels above this point activate the second tier of gain reduction in the first three stages. Each stage incorporates a second set of diodes that reduces the gain by another 7 dB. In the first tier of gain reduction, reduction started at the last stage and proceeded to the first; in the second tier, the reduction starts at the first stage and proceeds to the third.

In the first stage, diodes CR3089 and CR2087, are forward biased when the stage is in the unity gain mode. Limiting occurs in the same manner as described above with a further increase in input signal level, and results in less than unity gain through the stage (approximately 1/3). The one, two, three reduction sequence is established by the values of pull-down resistors R3082, R2076, and R2066.

Detector

The Detector circuit detects and filters the Log Amplifier circuit output signal and produces the VIDEO signal that is transmitted to the Video Amplifier circuits. The circuit consists of an operational amplifier with a diode detector in the feedback path and a low-pass filter at the output.

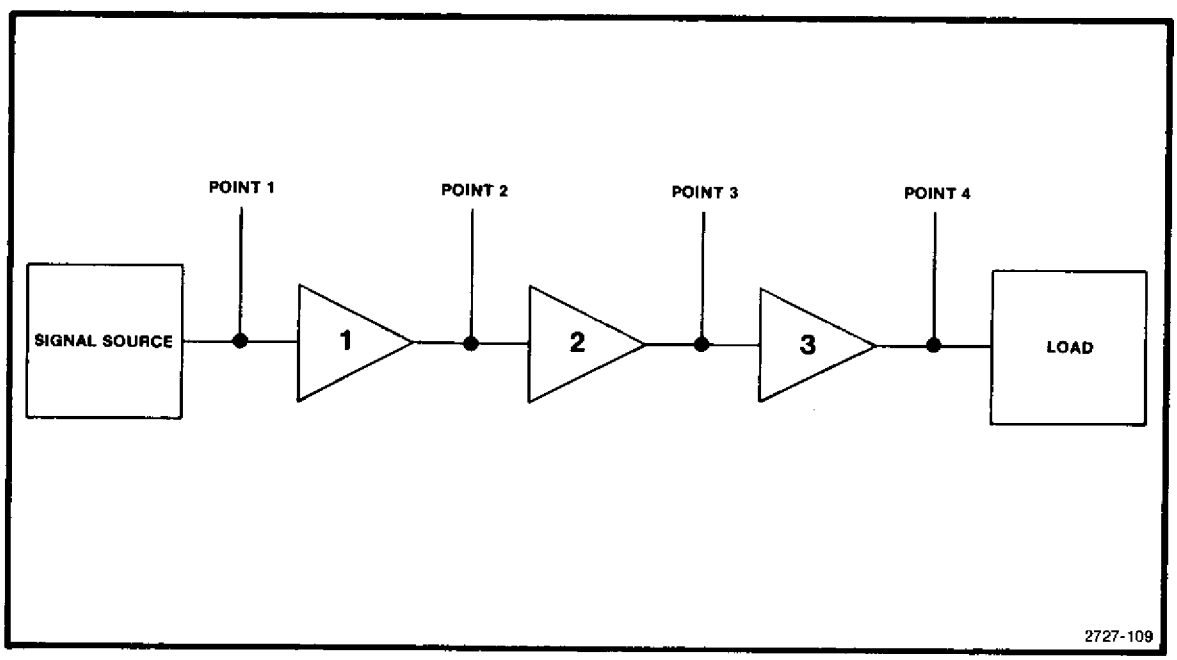


Fig. 5-5. Three-stage log amplifier.

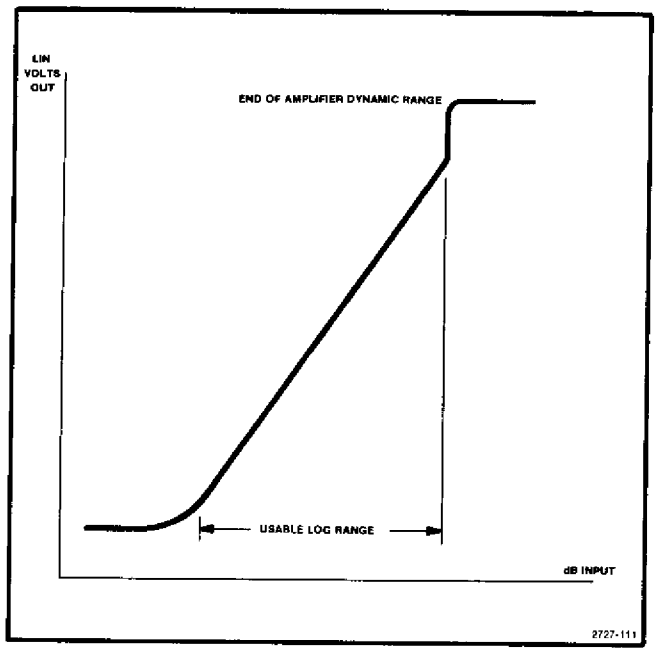


Fig. 5-6. Log amplifier gain curve showing breakpoint.

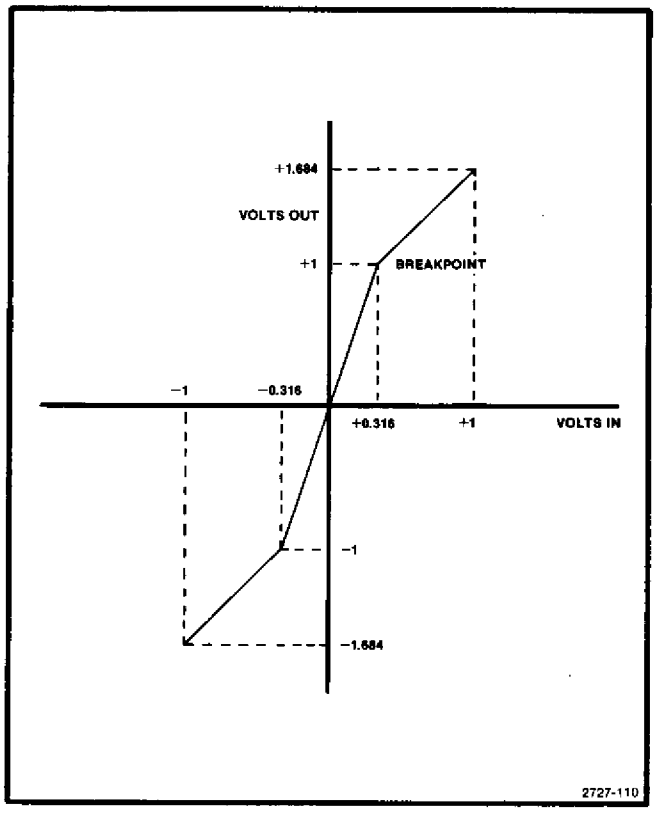


Fig. 5-7. Ends of logging range.

Actually, the circuit called an operational amplifier is not easily recognized as such. It is made up of grounded emitter amplifier Q4025 and a differential amplifier consisting of Q4030 and Q4035. The summing node for the negative input is the base of Q4025 (the positive input is at the grounded emitter of Q4025). Also, the differential amplifier is designed for high impedance output to allow the current that is available from Q4025 to drive the operational amplifier very rapidly during the period when both detector diodes (CR5033 and CR5027) are effectively open circuited; that is, when the output is near 0 volt. When neither diode is conducting, it is necessary that the output change rapidly through that zone. Note that the network consisting of resistors R5032, R5029, R5020, and capacitor C5029 is included to stabilize the dc operating point.

Figure 5-8 shows a simplified schematic diagram of the detector circuit. As shown in this diagram, two detector diodes (CR5033 and CR5027) are used, but only the positive half cycle is taken as the output (from CR5027). The output from the collector of transistor Q4035 is applied to the diodes through capacitor C5035. Ac coupling is used on both sides of the detector to prevent temperature coefficient effects of the operational amplifier from affecting the detector output. This isolation provides that the detector charges and discharges capacitors C5035 and C5024 by the current induced in each half cycle of the signal without changing voltage level.

This detector operates as an area (average) detector despite the fact that the Log Amplifier circuits operate on peak principles. It is possible to use an average detector because of some very selective tailoring in the Log Amplifier circuits. For instance, resistor example R5021 in the final log amplifier stage is sized to reduce the amount of current standing in the final stage output diodes, thus tapering the curve very slightly to improve linearity at the lower end of the curve. Log Gain adjustment R4020, in the final amplifier stage, is adjusted for increased linearity at the top of the curve.

As shown in the diagram, the positive-going output signal, from the detector, is applied through a low-pass filter consisting of capacitors C7024, C7014, C7021, C7011, and inductors L6011, L8021, to the Video Amplifier.

6 DISPLAY SECTION

FUNCTIONAL DESCRIPTION

The display section performs several functions:

1) it accepts the VIDEO signal from the IF section, and processes the signal, and provides the vertical crt plate drive signals;

2) it processes the sweep voltages from the sweep section and produces the horizontal crt plate drive voltage. If Digital Storage is selected, vertical and horizontal signals are further processed by that circuit group;

3) it accepts character information from the instrument data bus and generates crt plate drive signals to display alpha and numeric characters;

4) it accepts control levels from front panel beam controls and generates unblanking signals to control display presence, brightness, and focus.

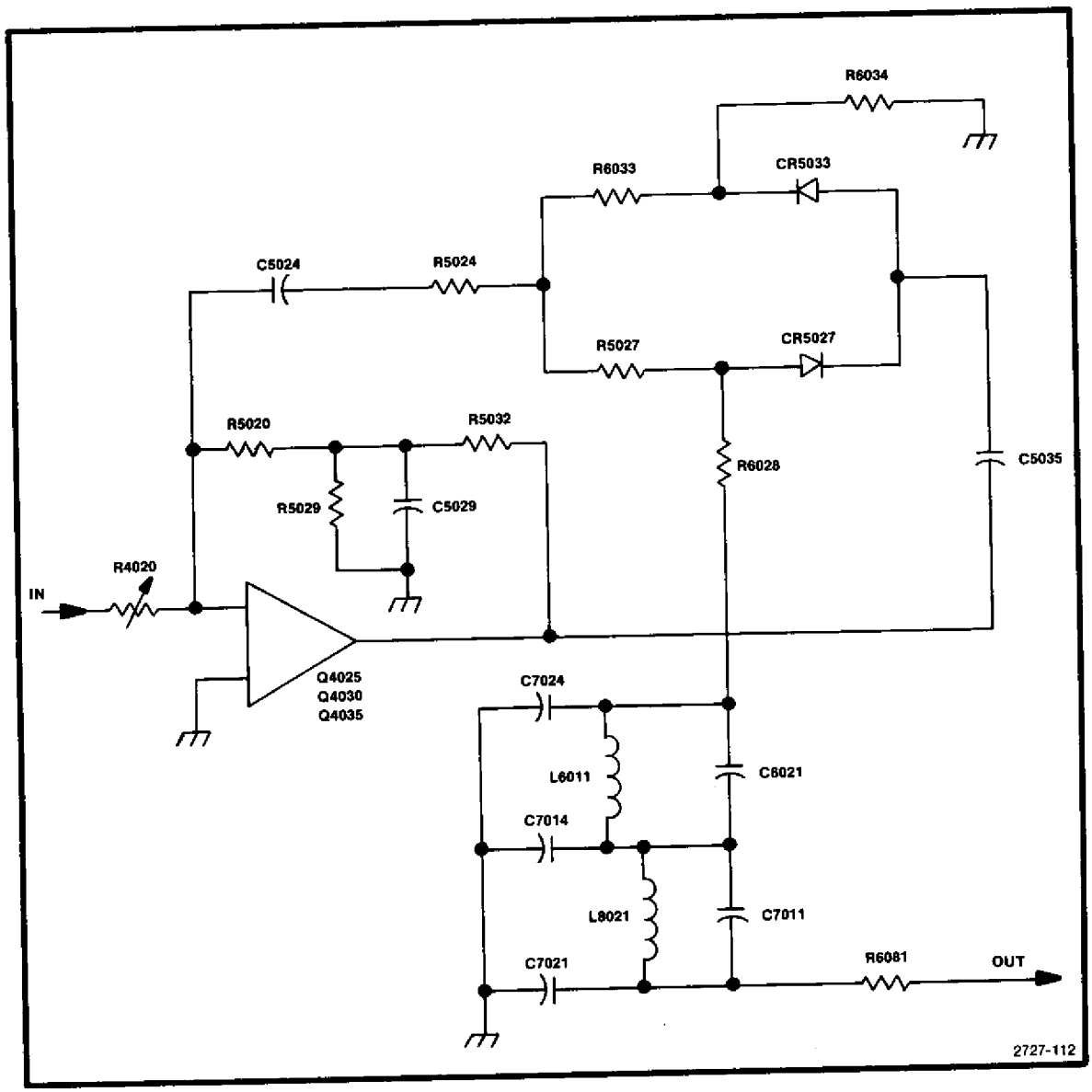


Fig. 5-8. Simplified detector circuit.

Video signals from the IF section are applied to the Video Amplifier. In the logarithmic mode, the signal is amplified linearly and applied to the Video Processor. In the linear mode, amplification is exponential to convert the logarithmic characteristic to linear function. In either mode baseline compensation, from the Video Processor, is applied to the video signal to compensate for any unflatness in the front-end response. Also at the output of the Video Amplifier, a pulse stretch circuit alters narrow pulses so data can be displayed by the Digital Storage logic.

From the Video Amplifier, the output is applied to the Video Processor. Three functions are performed by the Video Processor. The first is unflatness compensation for front-end response variations. Video filtering, the second function performed by this circuit block, allows for selection of six video bandwidths (30 kHz, 3 kHz, 300 Hz, 30 Hz, 3 Hz, and 0.3 Hz) under control of the instrument microcomputer. The third function is out-of-band blanking. This blanks the upper and lower ends of the local oscillator swept frequency range to provide a selected window for the display. This is also controlled by the microcomputer.

The Digital Storage logic provides operator selection of various display modes for observing the signals from the Video Processor. These modes are: MAX HOLD, SAVE A, B—SAVE A, VIEW A, and VIEW B and signal averaging or peak level display. The circuit block consists basically of:

1) vertical circuits that digitize signals at 512 points across the display and store those digitized data for display or processing, and

2) horizontal circuits that translate the sweep signal into memory address into which the signal data are stored. The stored signals are then used for the various processing as required by operator display selection, and for recreation of the display. From the Digital Storage logic, horizontal and vertical signals for the recreated displays are applied to the Deflection Amplifiers.

The Deflection Amplifiers receive vertical signals from the Digital Storage, or the Video Processor, and sweep voltage from the Sweep section, along with readout data from the Crt Readout circuits and produce signals to drive the crt for the display. The Digital Storage or Video Processor vertical outputs may be selected. Likewise, horizontal signals from either the Digital Storage logic or the Sweep section can be selected. During the display segments in which digital crt readout is required, the Deflection Amplifiers input signals are supplied by the Crt Readout logic. The amplifier contains the switching circuits to perform the above selection functions, and amplifier stages to produce the plate drive signals.

Crt readout data is controlled by the Crt Readout logic. These circuits generate letters and numbers for display under control of the microcomputer. Using data received from the data bus, a character memory and generator circuit derives each character. Digital signals, describing each character, are then translated into deflection signals by digital-to-analog converters. These signals are applied to the switching logic in the Deflection Amplifiers.

Beam intensity, nominally from the front panel, is implemented in the Z-Axis logic. Unblanking for display of either signals or readout data, and baseline clipping is also implemented in the Z-Axis logic. Control of unblanking is by signals from the Sweep section, the Crt Readout logic, the Deflection Amplifiers, and the Digital Storage logic.

VIDEO AMPLIFIER 24

Refer to the block diagram adjacent to Diagram 24. The Video Amplifier circuits provide for the selection of either logarithmic or linear display mode, for the selection of dB per division in logarithmic mode, for selection of pulse stretching in narrow peak signal operations, and for offsetting the signal amplitude during the signal identify mode. These circuits consist of the log mode amplification and dB/div switching circuits, the linear mode amplification and gain control circuits, the pulse stretch circuit, and the various digital control circuits.

Log Mode

The Log Mode circuits accept the VIDEO signal from the Log Amplifier and process that signal to add offset for selecting the segment of the log amplifier gain curve to be displayed. It also allows for selection, under program control in the 496P, of display gain steps of 1 to 15 dB per division on the screen. (Only 2 dB and 10 dB/Div are selectable from the front panel. The 496P can select all steps under program control.)

The signal from the Log Amplifier is applied to preamplifier U4090A. The VIDEO 1 signal from the Video Processor is also applied to U4090A. This signal compensates for flatness errors in the front-end circuits by offsetting the VIDEO signal in the opposite direction equal to the unflatness. The two signals are summed at the input of U4090B with the reference level set by Input Reference Level potentiometer R4071 (this reference level will be described later) and with the output from digital-to-analog converter U5041.

Converter U5041 converts the microcomputer commands to an offset signal which selects that portion of the Log Amplifier curve on which to place the display. The concept for this offset is as follows (refer to Fig. 5-9).

If the display is in dB/div, changing the POSITION control, which is located after the log amplifier, is the same as changing the signal level, or gain, before the log amplifier. Thus, instead of using a large amount of linear gain change before the log amplifier, a digital-to-analog converter is used to effectively move the display up or down the log curve. This process is called "offset" and it accomplishes the same effect as moving the POSITION control, except that the display on screen does not change, only the signal level required to reach the reference level changes.

Since the non-programmable 496 allows selection of either 10 dB per division or 2 dB per division, and the programmable 496P allows selection of 1 to 15 dB per division, the system must allow the gain to change while keeping the top of the screen constant, and must allow any 16 dB segment (in 2 dB/div mode) to be displayed. Nominally, the Log Amplifier operates with 0 dB or at the top of the screen.

The output of preamplifier U4090A is equivalent to 20 mV/dB. Full screen is always 2.2 V. At 2.2 V, the output of variable gain log amplifier U4090B is 0 volt, the only voltage at which the resistors in the switching network in the feedback circuit of preamplifier U4090B can be switched without changing the output voltage. (The switching network will be described later.) The 2.2 volt output of U4090A is adjusted during calibration to full screen by Input Ref Lvl (input reference level) potentiometer R4071.

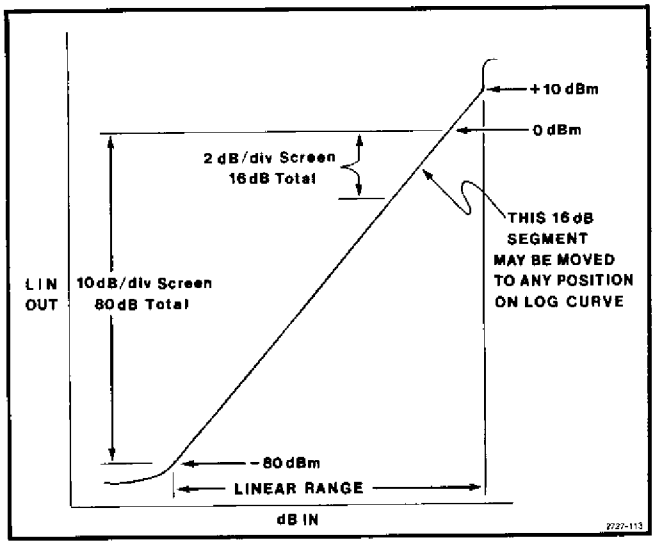


Fig. 5-9. Selection of display position on log scale.

From U4090B, the output signal is applied through FET Q5090 (if that transistor has been turned on by data bit 6 when 6 is high or a 1) to output operational amplifier U4090C, then through emitter follower Q4100 to the Video Processor via the front panel LOG CAL potentiometer. The Output Ref Lvl (output reference level) potentiometer, R4081 in the input circuit to U4090C, is used to adjust the output to provide a full screen display after Input Reference Level potentiometer R4071 is set for no change in the output of U4090B when switching from 10 to 2 dB or vice versa.

As an aid to understanding the system operation, it is probably useful to understand the basic calibration sequence that includes the above two controls. The sequence is as follows:

1) the digital-to-analog converter output voltage is calibrated by adjusting the front panel AMPL CAL control so that the output is appropriate for 10 dB per division;

2) the Log Amplifier detector circuit gain is adjusted so the Log Amplifier output agrees with the digital-to-analog converter output;

3) input Ref Lvl potentiometer R4071, is adjusted for no change in output level from U4090B when alternately pressing the 10 dB and 2 dB selector switches on the front panel;

4) output Reference Level potentiometer R4081 is adjusted for a full screen display.

The gain switching network provides for switching 15 resistance values into the feedback path of variable gain log amplifier U4090B, and consists of four FET switches (Q4075, Q4070, Q5070, and Q5075) and four resistors (R7071, R6074, R6073, and R6082). The FET switches, controlled by data bits 1, 2, 3, and 4 from the analyzer data bus, connect feedback resistors for U4090B in 15 value combinations as determined by the binary content of the four data bits.

In the non-programmable 496, only the 10 dB per division and the 2 dB per division selections are available and are controlled by front panel switches through the analyzer microcomputer In the programmable 496P, the full 15 combinations are selectable through program control.

Linear Mode

The Linear Mode circuits accept the output from log preamplifier U4090A and rescale the signal level to linear values. Since no switching is provided in the Log Amplifier (that is, all signals are logarithmically scaled), to operate the system in linear mode requires that the signal level be re-exponentiated. Thus, high gain is required at the top of the screen and low gain is required at the bottom of the screen to offset the characteristics of the Log Amplifier.

In addition to the signal path described in the Log Mode circuits, the output from preamplifier U4090A is also applied to linear mode amplifier U4090D, an operational amplifier with a successive resistor network in the feedback path. From this amplifier, the output signal is applied through FET Q5095 (if that transistor has been turned on by data bit 5 from the analyzer data bus being a 1) to the summing node at the input to output amplifier U4090C. After this point, the signal path is as described in the Log Mode circuits description.

Starting at the signal level that represents the top of the screen (0 volt) at the output of linear mode amplifier U4090D, the operation of the network is as follows.

With a 0 dBm input from the Log Amplifier to the Video Amplifier, the output of U4090D is 0 volt. At that level, the feedback path is through only resistor R6104. The other feedback path resistors (R7079, R7076, R7092, and R7093) are not in the path because the switch transistors are biased off by the bias network consisting of resistors R7082, R7081, R6085, R7086, and R7095, plus diode CR7095. (The diode is included for temperature compensation purposes.) As the display moves away from full screen, the output of U4090D rises positive and transistor Q6115 is biased on, thereby placing R7097 in parallel with R6104 and reducing the gain of U4090D. Further increases in the output of U4090D cause transistors Q6110, Q6090, and Q6095 to conduct in sequence and add resistors R7096, R7092, and R7095, respectively, in parallel to the feedback path. The sequential adding of resistors into the feedback path effectively reduces the gain of U4090D exponentially. Although it may appear that such a system would result in steps of gain resolution, the reaction characteristics of the transistors smooth the transitions and result in a smooth exponential gain curve.

Pulse Stretcher

The Pulse Stretch circuit, under control of the analyzer microcomputer widens narrow peak signals to allow the Digital Storage circuit time to acquire such signals. If this is not done, the 9-microsecond digitizing rate of the Digital Storage circuits is too short to acquire very narrow signals. The circuits accomplish this function by stretching the fall time of fast pulse signals. The circuit consists of FET switch Q7110 and the associated components in the feedback path of the output operational amplifier U4090C.

When pulse stretch mode is not selected (by data bit 8 from the analyzer data bus being a 0), FET switch Q7110 is off. With Q7110 off, capacitor C7104 is not in the circuit and the normal feedback path for U4090C and extra pulldown current is provided through resistor R5108. This allows the U4090C output to fall as fast as it rises.

When pulse stretch mode is selected (by data bit 8 being a 1), FET switch Q7110 is turned on and capacitor C7104 is inserted into the feedback circuit to slow the fall of the output. Also, the only pulldown current is through resistor R5086. Diode CR7101 serves only to isolate the pulse stretch circuit from the output circuit of the output amplifier. Diode CR5101 turns on at low levels to prevent the amplifier output from going too far negative and slowing the response when the input changes. When the output of Q4100 swings positive, the diode CR5101 disconnects. The primary advantage of this circuit is that the operational amplifier removes offsets by controlling very closely the voltage at the emitter of Q4100.

Digital Control

The Digital Control circuit provides the control signals for selection of the various Video Amplifier functions and consists of address decoding, data latching, and buffering circuits. From the analyzer data bus, address data and the DATA VALID signal are applied to the address decoder U6070 through edge connector pins 30, 26, 25, 27, 28, and 31. The decoder produces two enable signals that are applied through inverter U5070 to gain latch U6040 and mode latch U6050.

The Gain latch IC U6040, is an eight-bit latch that supplies command data to eight-bit digital-to-analog converter U5041 to offset the Log Amplifier output signal. Mode latch U6050 is an eight-bit latch that supplies command data through buffer U6060 to select the resistors in the dB per division switching circuit and to select pulse stretch, and log or linear mode.

VIDEO PROCESSOR 25

Refer to the block diagram adjacent to Diagram 25. The Video Processor circuits perform video filtering, blanking, and interfacing with a 1405 TV Sideband Adapter. The circuits that perform these functions are described in the following paragraphs.

496/1405 TV Sideband Adapter System

The TV Sideband Adapter is a specialized tracking generator that is used together with the 496/496P to analyze the response of a television transmission system. The spectrum analyzer is set to monitor the RF output of the transmitter while the sideband adapter drives the video input of the system. The video input may be at the transmitter site, the head end of the studio-transmitter link, or the video switcher in the studio. The sideband adapter must be connected to the 1st LO of the 496/496P by a short length of coaxial cable.

The system shown in Fig. 5-10 depicts a TV transmitter operating on Channel 10 with a video carrier at 193.25 MHz. The sideband adapter is tuned to Channel 10. The spectrum analyzer is tuned to 195.25 MHz with a span setting of 1 MHz/Div (for purposes of illustration, the sweep is assumed to be halted at the center frequency of the analyzer).

The sideband adapter applies a 2 MHz signal to the AM modulator of the video transmitter. The modulator produces a lower sideband at 191.25 MHz, a carrier at 193.25 MHz, and an upper sideband at 195.25 MHz. This signal is amplified, filtered, and combined with the FM aural signal. The composite signal is sensed by a RF pickup and applied to the RF Input of the 496/496P.

The 1st Converter of the spectrum analyzer applies the composite signal to the 1st mixer. The composite signal is mixed with a 2.26725 GHz signal from the 1st LO, forming three products. The subsequent stages of the analyzer accept only the 2.072 GHz product and reject the rest. For frequencies used in this example, the accepted product is the difference between the 1st LO and the upper sideband of the TV signal. The product is converted twice more, amplified, filtered, logged, and detected. This detected signal is applied either directly to the video amplifiers of the crt or to digital storage.

The 1st LO signal of the 496/496P Spectrum Analyzer is applied to the RF mixer of the TV Sideband Adapter. The 2.26525 GHz signal from the tunable LO is subtracted from the 2.26725 GHz signal from the 496/496P LO, yielding a 2 MHz product. This video frequency signal is conditioned with sync and blanking signals and applied to the video input of the TV transmitter.

When the 496/496P Spectrum Analyzer is sweeping, the video signal starts at 3 MHz, falls to 0 Hz, and rises up to 7 MHz. During this interval, the analyzer displays the lower sideband as it moves toward the carrier, displays the carrier, and then displays the upper sideband moving away from the carrier. Since the 496/TV Sideband Adapter system is similar to a tracking generator system, it rejects noise and uncorrelated signals. This allows normal in-service use of the transmitter by adding a low level (1 to 3 IRE units) cw signal to the video or by using full levels with a VIT inserter.

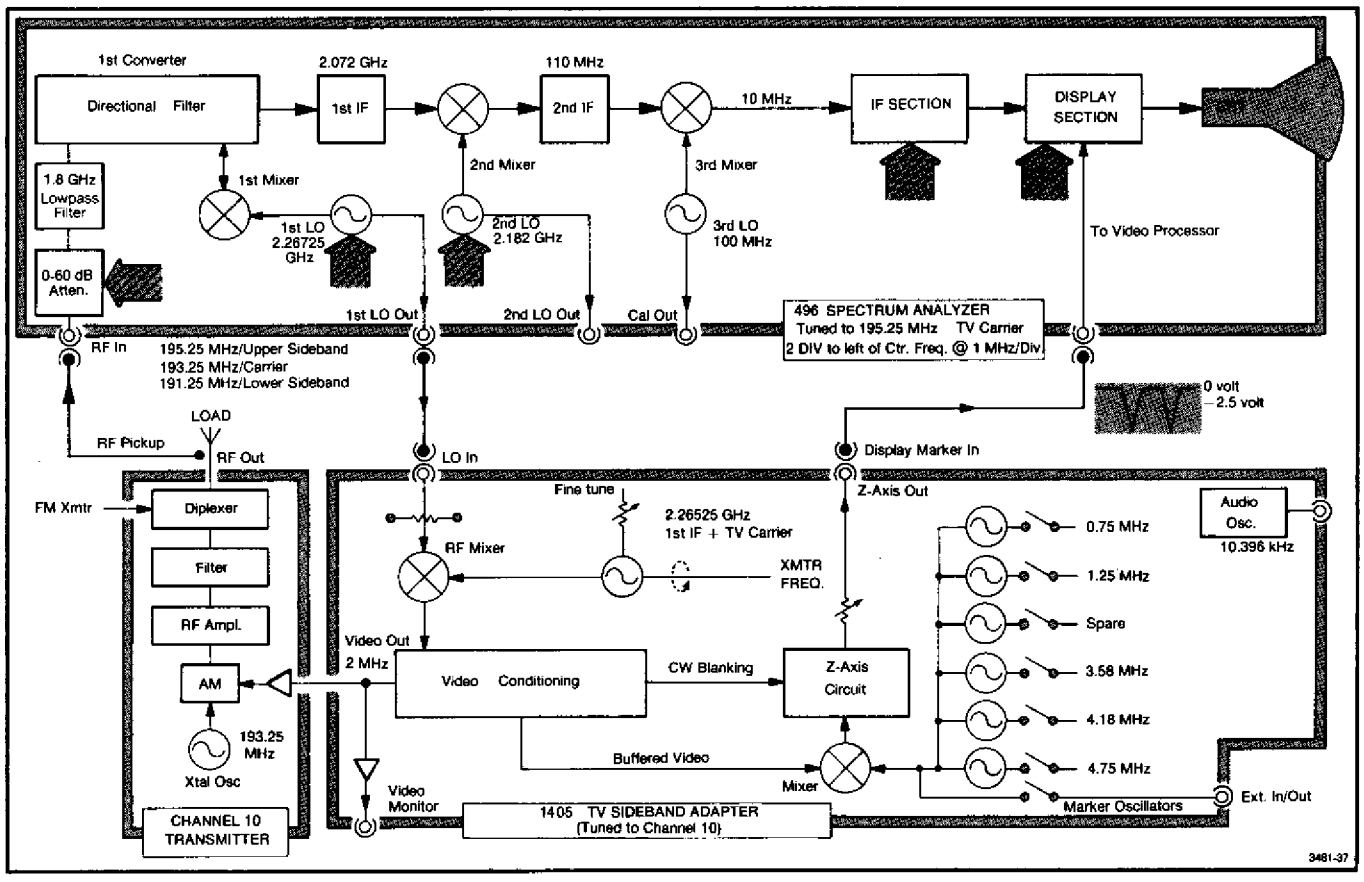


Fig. 5-10. 496/1405 TV Sideband Adapter System.

The sideband adapter can insert frequency markers at preselected deviations from the carrier frequency. Six selectable crystal oscillators have their outputs mixed with video signal and applied to a Z-Axis circuit. This circuit produces two negative pulses as the video signal sweeps through the crystal oscillator frequency. These pulses are applied to the spectrum analyzer, where they appear on the crt as two notches on either side of the marker frequency. (If a 7L12 or 7L13 is used, two dark spots will appear on the trace instead of two notches.) The sideband generator allows the width and depth of the notches to be adjusted with the Width and Intensity controls.

Video Marker

The Z axis signal from the TV Sideband Generator is applied to the DISPLAY MARKER INPUT connector on the rear of the 496/496P. This 0 to −2.5 volt signal is applied to pin 60 of the Video Processor board, which provides a 600 Ω termination via resistor network R4067, R4066, and R4064. Diode CR4065 produces negative clipping and R4066 and C4068 provide low-pass filtering.

Resistors R4063 and R3069 sum the Z axis signal from the sideband generator and the video signal of the spectrum analyzer. The feedback network of R3064 and R4062 set the gain of U3067 high enough to compensate for the losses of the summing network. The summing network causes the negative pulses from the sideband generator to produce notches in the video signal of the spectrum analyzer. Capacitors C3064, C3069, and C3068 assure a wide bandwidth for the video signal.

Video Leveling

A minor slope caused by the 1.8 GHz lowpass filter is corrected by inserting R4023 between OSCILLATOR DRIVE and the VIDEO 1 output signal. This resistor, which is selected at factory calibration, forms a voltage divider with R4046. The resistor is connected through switch U3025; pins 6 and 7 are always connected together, because control pin 8 is open-circuited. Substitution of R4023 allows fine correction of flatness at the high end of the analyzer's range.

Video Filter

Video filtering provides selection of one of six bandwidths, under the control of the analyzer microcomputer. As shown in the VIDEO FILTER table on Diagram 25, data bits 1 through 4 select any of six bandwidths: 30 kHz, 3 kHz, 300 Hz, 30 Hz, 3 Hz, and 0.3 Hz. Either wide or narrow-band filtering is selected at the front panel (30 kHz, 3 kHz, and 300 Hz are defined as wide-band; 30 Hz, 3 Hz, and 0.3 Hz are defined as narrow-band), and the microcomputer makes the selection, based on such factors as sweep rate and total dispersion. With no video filtering (all data bits equal 0), the video system bandwidth is 500 kHz, as determined by circuits that follow the Video Processor, which has an internal bandwidth of 3 MHz.

Two signal inputs can be applied to the Video Filter circuits: EXT VIDEO and INTL VIDEO. The EXT VIDEO signal, from the rear panel auxiliary connector, is applied to pin 15 of switch U3063 through edge connector pin 53. The INTL VIDEO signal from the Video Amplifier circuits (via the front panel LOG CAL control) is applied to pin 2 of switch U3063 through edge connector pin 51. Note that the two left sections of switch U3063 are normally held energized (pins 2 and 3 connected, pins 15 and 14 disconnected) by the +5 V supply through resistor R3064. If the EXT VIDEO SELECT line (also from the rear panel auxiliary connector through edge connector pin 55) is grounded, those switch sections are de-energized and the External Video signal is applied through, or around, the filter to become the VIDEO FILTER OUT signal at edge connector pin 57. This is shown in the simplified schematic diagram of Fig. 5-11.

As shown in the figure, when no filtering is selected (all data bits equal 0), either the internal or external signal is applied around the filter because the two right sections of switch U3063 are not energized by data bit 1. When data bit 1 is high (1), filtering of some value will be selected by bits 2, 3, and 4, which control three sections of switch U2015 to add or delete filter time constant.

The filter consists of resistors R2023, R2021, R2022, and capacitors C3026, C2016, connected between two comparators (U3062 and U2066). Table 5-6 lists the components that are in the circuit for each of the six bandwidths. Note that data bits 2, 3, and 4 are applied to switch U2015 pins 8, 16, and 9, respectively, to select components.

From buffer U2066, the signal is applied through contacts 7 and 6 of switch U3063 and edge connector pin 57 as the Video Filter Out signal.

Video Blanking

The Video Blanking circuits allow for selective blanking of the lower and upper ends of the local oscillator range. This is required because the local oscillator sweeps full span mode regardless of the prescribed band limits. Thus, the video system is designed to effectively open a display window only during the time for display. Data bits 5, 6, and 7, under control of the microcomputer, select the appropriate amount of display for each band.

Since the video filtering is on the Video Processor board, and the PRESELECTOR DRIVE signal (which provides frequency information, in voltage form) is also available, this board is a logical place for video blanking. Switch U3063 incorporates a disable function that, when provided a low input, opens all switch sections regardless of individual section input. Using this feature, the Video Filter Out signal may easily be blanked at will.

Control for this disable function is from a combination of outputs from two comparators, U3015A and U3015B. Inputs to these comparators are from the PRESELECTOR DRIVE signal and a combination of voltage dividers that are switch selected under control of data bits 5, 6, and 7. The PRESELECTOR DRIVE signal is applied from edge connector pin 54 to the minus input side of U3015A through divider resistors R4013 and R4012, and to the plus input side of U3015B through divider resistors R4014 and R4011. These dividers reduce the +10 V to −10 V excursion of the drive signal to +2.5 to −2.5 V, the maximum input level to the comparators.

Input to the plus side of U3015A is from a divider that consists of resistors R3011, R3012, R4024, and R4015. Note that the excursion of R4024 is controlled by data bit 5 through pins 15 and 14 of switch U3025, and that the inclusion of R4015 is controlled by data bit 7 through pins 2 and 3 of the same switch. Thus the junction of divider resistors R3011 and R3012 may be connected to −10 V through R4024 or to ground through R4015. Refer to the VIDEO BLANKING table on Diagram 25 for data bit states for different bands.

Input to the minus side of U3015B is from a divider that consists of resistors R4018, R4017, and R3028. Note the inclusion of R3028 is controlled by data bit 6 through pins 10 and 11 of switch U3025. Adding resistor R3028 connects the junction of R4018 and R4017 to +10 V through R3028. This arrangement of switching negative and positive levels for comparison with the reduced PRESELECTOR DRIVE signal, enables the top and bottom extremes of the frequency excursion to be blanked by activating the disable function of switch U3063. This blanking is under the control of the microcomputer.

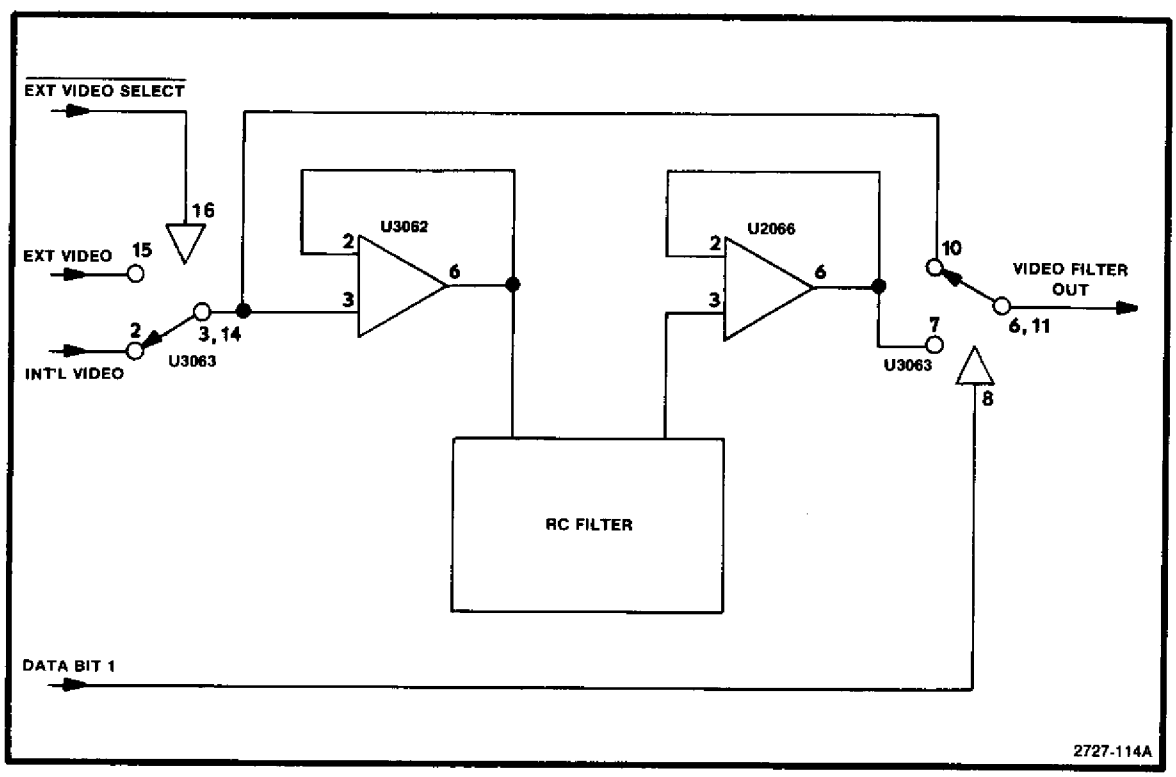


Fig. 5-11. Video filter simplified schematic.

DIGITAL STORAGE 26 27

Digital Storage provides the operator with the capability of selecting the method for displaying and processing information contained in the digital storage memories. This allows operations such as determining the highest amplitude that occurred during a selected period (MAX HOLD mode), storing a signal for later examination (SAVE A mode), subtracting one signal from another (B−SAVE A mode), averaging signals (AVERAGING mode), and comparing signals (VIEW A, VIEW B modes). Two memories are used independently in these operations to store two complete signals that are each digitized at 512 points across the sweep. Thus, two signals may be observed simultaneously or processed in various ways.

In MAX HOLD mode, the highest amplitude at each of the 1024 points in successive sweeps is stored and displayed. In SAVE A mode, a signal is stored in one memory for later examination, and is not updated. In the B−SAVE A mode, the A signal is stored and not updated, then arithmetically subtracted from the B signal, which is stored and continually updated. In the AVERAGING mode, the display area is divided by a horizontal cursor. Above the cursor, signals are peak detected and displayed; below the cursor signals are averaged. In the VIEW A and VIEW B modes, the contents of the selected memory or memories are displayed.

Graphical presentation of mathematic functions or experimental data is common today. One class of such graphs is those that have a single Y value for each X value. An alternate presentation of the data in this graph would be a table in which the X coordinate values were simply listed along with a corresponding Y value for each X value. In further simplification, if the first X value and the spacing between X values (assuming that all spacings are equal) were known, the two column table could be reduced to a single column with the X value implied by the position of the Y value in the column. This then is the essence of digital storage: to convert a vertical analog voltage (Y coordinate value) to a binary number and insert that number in a stored table. The location of the Y value in the table is determined by converting to binary the analog sweep voltage (X coordinate value). Once the table is created by storing a set of binary numbers representing values across a waveform, the waveform can be recreated at any time by converting the table values (Y) and positions (X) back to analog voltages representing amplitude and sweep position.

The digital storage system used in the 496/496P uses two tables: A and B. Table B is always updated on every sweep. Table A is changed unless SAVE A mode is selected. There are 512 A values and 512 B values. The spacing between values is the same throughout both tables, but the starting point for table B is shifted slightly so that when both tables are being read, the readout values are interlaced.

When the signals are recreated, the operator has the option of displaying either A or B, or both A and B. If both are to be displayed, and SAVE A mode is also selected, the contents of both table A and table B are drawn, each display in its own trace. If SAVE A mode is not selected, the contents of both table A and table B are displayed on one trace, with 1024 value positions across the screen. A third trace option is also available. In the B minus A mode, the displayed values are those resulting from an arithmetic operation and are the difference between the contents of table A and table B for each X value of analog sweep voltage.

Since a signal waveform is continuous and a table has discrete X values, an algorithm is used to determine the Y value to be stored for a particular X value. This allows the operator to select one of two methods for determining Y values: peak or average. The Y analog voltage is continuously sampled, with the sampling rate dependent upon sweep speed. For each X value, there are always at least two samples and there may be as many as 2^{17} samples. From this set of samples then, the user may select either the largest sample value (peak value) or the mean of all the samples (average value). Selection between peak and average is controlled by the front panel PEAK/AVERAGE control, which sets a dc level that is compared with the analog vertical input to produce the PEAK/AVERAGE logic signal. When the input signal is below the level selected by the front panel control, the signal is averaged; when the input is above that level, the peak signal is displayed. The dc level appears on the display as a positionable horizontal line. This marker line is created by switching the dc level to the analog output line during the marker cycle to produce the MARKER logic control signal.

Superimposed on the marker line is an intensified spot called the UPDATE MARKER, which indicates the X value at which new Y values are being computed for display update. The update marker is formed by comparing the analog sweep input to the display analog X output. When the two are the same value, the sweep is forced to pause, thus increasing the marker intensity at that point. Refer to the block diagrams, adjacent to Diagrams 26 and 27.

Table 5-6
FILTER COMPONENT COMBINATIONS

Bandwidth	DB=1	R2023	C3026	R2021	R2022	C2016
30 kHz	1	X	X	X	X	
3 kHz	1,4	X	X	X		
300 Hz	1,3,4	X	X			
30 Hz	1,2	X	X	X	X	X
3 Hz	1,2,4	X	X		X	X
0.3 Hz	1,2,3,4	X	X			X

Central to the 496/496P digital storage system are two specially designed and manufactured IC's; U1023 and U2032. Vertical section IC U1023 contains the vertical acquisition and display logic, and peak detection, signal averaging, Z-axis blanking, and special Y-value processing circuits. Horizontal section IC U2032 contains the horizontal acquisition address counter, horizontal display counter, 10-bit RAM address multiplexer, and a programmable logic array system control matrix. The remainder of the digital storage control circuits consists of two 8-bit digital-to-analog converters, two 10-bit digital-to-analog converters, one 10-bit latch, 8k bits of random access memory, and various ancillary circuits. Timing is controlled by clock pulses from the microcomputer board to pin 1 at approximately a 1 MHz rate. The two primary IC's, U1023 and U2032, are described as appropriate at the beginning of the vertical and horizontal section detailed descriptions that follow.

Vertical Section 

Vertical Control. (Refer to Fig. 5-12.) The vertical analog voltage is converted to a Y binary value using an 8-bit successive approximation register. Nine clock cycles are required for each Y conversion. After the conversion has taken place, the successive approximation register produces the negative-going $\overline{\text{SYNC}}$ signal. Most functions on both the vertical and horizontal control IC's are synchronized by this signal. On the negative-going transition of $\overline{\text{SYNC}}$, the successive approximation register is reset to 10 00 00 00 (binary) and the next conversion cycle begins. Incoming data bits are latched into the successive approximation register on the negative-going clock transition. From the register, the output data are applied to the peak and the averaging circuits.

The averaging circuit consists of three groups of circuits: those that accumulate the grand total of all of the Y values for a given X value (this total is called the numerator), those that count the number of samples that make up the numerator (this total is called the denominator), and those that subtract and shift to perform the division process.

As each new Y value is converted, it is added to the eight least significant bits of the numerator. Each carry from the most significant bit of this addition is counted by a 17-bit ripple counter. The contents of this counter and the 8-bit sum are cascaded to form a 25-bit grand total. Each time a new sample is added to the numerator, a second 17-bit ripple counter is incremented to produce the denominator.

A division cycle is initiated when the horizontal control IC U2032, located on Diagram 26, detects a change in the X value. At that time, U2032 produces the ST DIV (start divide) signal. Upon receipt of this signal, and in synchronization with the SYNC signal, vertical control IC U1023 performs several functions (refer to Fig. 5-12):

1) it latches the current numerator in a 25-bit latch (25 to 1 data concentrator in the block diagram), and latches the denominator in a 17-bit latch (17 to 1 data concentrator in the block diagram);

2) it clears the numerator adder circuits (25-bit summation register in the block diagram);

3) it performs a 17-bit priority encode on the denominator and loads a 1 in the appropriate cell of the 25-bit shift register;

4) it loads the latched numerator and denominator serially into the divide circuit (subtractor in the block diagram) using the contents of the 25-bit shift register as a mask;

5) it clears the denominator ripple counter (17-bit counter in the block diagram) to zero.

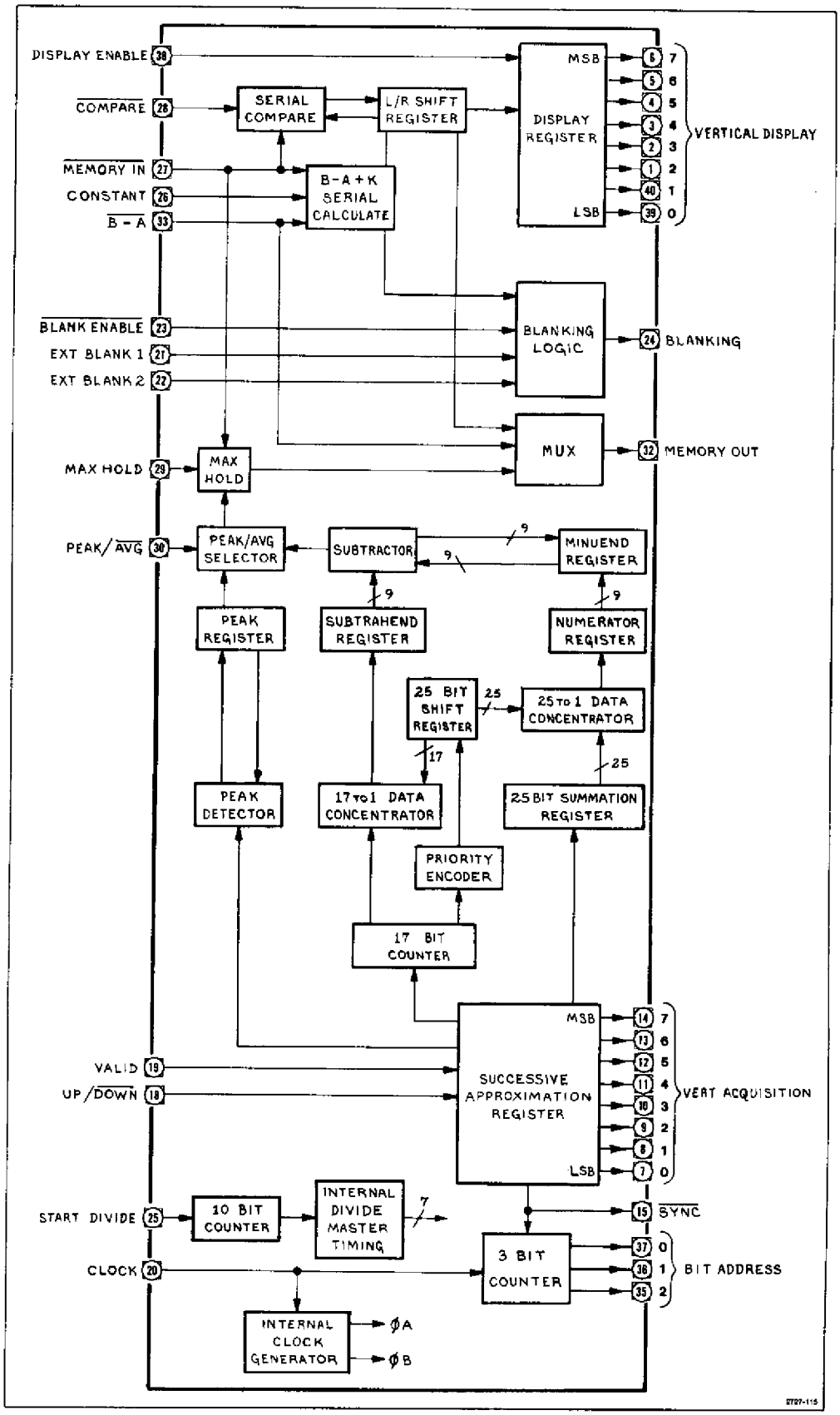


Fig. 5-12. Vertical control IC block diagram.

Ten clock periods are required to load the numerator and denominator into the divide circuit. The cycle starts on a SYNC pulse and the first bit of the quotient is available shortly after the first clock pulse following the next SYNC pulse. Division is performed by repeated subtract and shift operations. The quotient is arrived at serially with the most significant bit first. Only 8-bit accuracy is required, so, by using the priority encoder output as a mask, the divider circuit is loaded with the 8 most significant bits of the denominator and the 16 most significant bits of the numerator. (Ripple borrow for a 17 by 25-bit subtractor would be so long as to be impractical.)

The peak circuit consists of a peak detector and an 8-bit peak shift register. In operation, the previous peak Y value from the last set of samples is still stored in the peak shift register at the start of a conversion cycle. At that time, the peak detector, which is a serial compare circuit, is set to the state that will question whether the old or new number is larger. Each bit of the new value is then compared with the corresponding bit of the old value, most significant bit first. When one value is found to be larger, a flip-flop is set and the smaller number is gated out of the shift register. The start divide logic signal being true then forces the peak detector to select the new value and ignore the number in the shift register.

The peak/average selector, a multiplexer, selects either the peak or average value to be routed to the memories under control of the $\overline{\text{PEAK/AVG}}$ signal. The selector output is routed through the max hold circuit, which functions in the same manner as the peak detector. When the MAX HOLD signal is high, the value that is routed to the output multiplexer is the larger of two values: the current memory value at the subject X coordinate or the previously selected peak or average value.

Timing for setting up the divide operation and clearing the numerator, denominator, and peak circuit is controlled by a 10-stage Johnson counter. NOR-gate taps are taken from appropriate stages to develop the necessary clear and latch timing pulses. Because the denominator is loaded into the divide circuit using a priority encoder, the most significant bit is always a 1. Space and power were saved by modifying the subtractor and not storing this 1.

All data enter and leave the memory serially. Data read from memory enter an 8-bit shift register, and timed by SYNC, are transferred to the vertical display output latch (display register on the block diagram). The same shift register is used for other purposes, so the DISPLAY ENABLE signal prevents non-display information from being transferred to the output latches. An example of data moving through this shift register is that during the B minus A display mode. The A value is first read from memory and stored in the shift register. As the B value is read, the subtraction is done serially and the answer is applied to the shift register. Since the subtraction must be performed least significant bit first, a set of exclusive-OR gates change the order of extracting B from memory. The direction of shift for the shift register is reversed also to present the most significant bit to the proper display latch. The shift register output is also applied to the output multiplexer.

In the subtraction, the operation performed by the serial calculator is not merely B minus A. The actual expression implemented is $(B-A) + K$, where K is a serial input external constant specified by the user. This permits zero to be placed anywhere on the screen. To avoid confusion, when $(B-A) + K$ results in an off-screen position, the subtractor blanks the display. This is done by examining the carry bit and borrow bit when the most significant bit is calculated. If either bit is a 1, the screen is blanked.

When SAVE A mode is not selected and both A and B are being displayed, maximum resolution is obtained (1024 points across the display). If this display includes a very narrow pulse, it is possible that the top of the pulse is only as wide as a single X coordinate (2 to 2^{17} samples). If this maximum value were in the B table and SAVE A mode were selected and B turned off, there would be an apparent drop in amplitude. For this reason, when SAVE A mode is selected, a special set of circuits in U1023 compares all A and B values that have the same X value and stores the larger in table A. This is accomplished by first reading the B value and storing it in the display shift register. Then, as the A value is read, it is compared with the B value and the larger of the two is loaded into the display shift register. Finally, the number in the shift register is written into memory from the shift register. This operation is performed once each time that SAVE A mode is selected.

Vertical control IC U1023 also contains a 3-bit synchronous counter that identifies the specific bit of an 8-bit vertical value that is to be read from memory or written into memory. This is the only memory addressing that is performed by the vertical control IC. All other addressing is under control of the horizontal control IC (U2032).

Digitizing Circuits. The input vertical signal, VID FLTR OUT, coupled through edge connector pin 60 is applied through buffer U2033 to sample and hold switch U1033, which is controlled by flip-flop U1011B. Flip-flop U1011B generates the sample pulse and is enabled during the clock cycle after the last sample as indicated by the least significant bit from the successive approximation register in U1023. The switched sample is then applied through buffer U2032 to a summing junction, at which point the output current from the digital-to-analog converter (U2024) that is

supplied from the successive approximation register is subtracted from the sample current, and the difference current is applied through comparator U1031B to pin 18 of U1023 as the $\overline{\text{UP/DOWN}}$ signal. Thus, the combination of the successive approximation register, the digital-to-analog converter, and the sample and hold circuit effectively produces the binary equivalent of the input sample.

Address Decoding. The address decode logic accepts inputs from the address bus and produces the control signals for read and write operations: $\overline{\text{CONT W}}$ (control write), $\overline{\text{DATA W}}$ (data write), and $\overline{\text{DATA R}}$ (data read). The control write signal is used to gate the control word from the data bus into control register U1022 to generate mode control signals. This control word consists of five bits that represent front-panel functions. If output Q6 is low, a peak operation is forced; if output Q6 is high and Q7 is low, an average operation is forced. The data read and data write signals are applied to the interface logic to control memory read and write operations.

Interface Logic. The interface logic in general performs control and interface functions between the active data circuits in both the vertical and horizontal sections and the rest of the 496/496P. It allows the microcomputer to control the functions of the storage system and to access the digital storage memory, and it contains the circuitry for serial-to-parallel and parallel-to-serial conversion. (The microcomputer uses parallel transfer; the digital storage memory uses serial transfer.) Shift register U2021 is used to read data from memory to the data bus. Register U1021 is used to store information from the data bus for transfer to memory. Multiplexer U2016 performs the parallel-to-serial conversion and applies the data output to gate U2015B, which acts as a buffer to supply either the multiplexer output or the MEM OUT (memory output) signal from U1023 to the memory as the DSDI (digital storage data input) data train.

The interface circuit group at the lower right corner of the diagram is the handshaking logic that works with the horizontal control circuits for access to memory and for control of when to increment the memory address counter. In either a data read or data write operation (when the corresponding signal goes high), flip-flop U2014B is triggered, which in turn releases the BUS REQ (bus request) line, allowing that signal to go high. This signals the horizontal control circuit that access to memory is required. When the horizontal circuits recognize that request, those circuits pull the BUS REQ line low at the same time that SYNC is low. The interface logic detects the BUS REQ and SYNC low condition through U1013A, U1013B, U2011A, and U2012C, and produces the low $\overline{\text{BUS GRANT}}$ signal to indicate access to memory. The $\overline{\text{BUS GRANT}}$ signal then enables shift register U2021 to shift data from memory or enable register U1021 and multiplexer U2016 to shift data to memory as indicated by the $\overline{\text{DATA R}}$ and $\overline{\text{DATA W}}$ lines. At the end of a data read cycle, gates U1012B and U2023C produce the INCR ADRS (increment address) signal to increment the address register in the horizontal circuits.

Maximum Hold. As described previously, when MAX HOLD mode is selected, circuits in U1023 compare the binary equivalent of the input signal for a given X value with the information in memory for that same X value and cause the larger of the two to be stored in memory. The control signal that initiates this action is produced from Q5 of control register U1022. In combination with the VALID signal from the horizontal circuits, this signal produces the MAX HOLD command to U1023 through buffer U2023E and gate U1025A.

Constant Circuit. As described previously, in the B minus A operation, a constant is used. This constant is internally selectable with switch S1014. This switch, in combination with multiplexer U1015, supplies the constant to U1023. Multiplexer U1015 is in turn controlled by address bits 0, 1, and 2 to provide the proper switch signal to U1023.

Output Circuits. From the U1023 vertical display register, the parallel data output is applied to 8-bit digital-to-analog converter U1024. The converter output is then applied through a vector generator, consisting of an integrator (U1032 and C1031) with an associated feedback loop sample and hold circuit, to the output storage/cursor switch. Integrator U1032 has a time constant that provides a ramp lasting between the existing sample and the new sample (that is, between sync pulses). Circuits U1033A and U1034 and capacitor C1038 make up a sample and hold circuit with U1034 acting as an output buffer. From U1034, the output current through resistor R1032 subtracts from the digital-to-analog converter output current to modify the slope of the output ramp. The output of the vector generator is then applied to switch U1033B, which selects between the stored data and the marker under control of the buffered PK/AVG LVL (peak/average level) control signal from U2034B and supplies the output to the horizontal circuits.

Peak/Average Level Circuits. The buffered PK/AVG LVL signal is also supplied as a mode control signal to U1023 in combination with: the sample and hold up/down output from U2032, the VALID signal from the horizontal circuits, and Q7 of the control word from U1022 (always a 1), through buffer U1031A, gates U1025C, U1025D, U1025B, and inverter U2023D.

Horizontal Section (27)

A block diagram of the Horizontal control IC U2032 is illustrated in Fig. 5-13. The horizontal analog voltage is converted to a current table value through the use of a 10-bit tracking analog-to-digital converter, which consists of an up/down interlock and 10-bit up/down counter (U2032) and an external 10-bit digital-to-analog converter (U2036). As the sweep moves to the right, the counter increments; as the sweep retraces, the counter decrements. Each time the counter increments, a new X coordinate value is generated (the digital-to-analog converter output) and a ST DIV (start divide) signal is generated to start the storage cycle. The increment clock is the $\overline{\text{SYNC}}$ signal, the decrement clock is the basic 1 MHz clock divided by two. When SAVE A mode is selected, the counter skips every other binary number. Thus, only B coordinates appear as addresses.

Intelligence for the horizontal system is provided by a programmable logic array ROM state device (PLA). This PLA determines which trace is to be written on the screen, determines when to switch from read to write, generates the B–A coordination signals for vertical control IC U1023, controls the incrementing of the 9-bit display counter, and processes requests for the memory bus. Of these, the only function not obvious is the memory bus request. When an external device elects to read from or write to memory, it must request permission by allowing the BUS REQ (bus request) signal to go high. When that time becomes available, the PLA pulls the BUS REQ line low, signalling the start of a request cycle. For the next eight clock cycles, the multiplexer output lines are driven to the high impedance tristate mode.

The combination of the up/down interlock, 10-bit up/down register, 9-bit display counter, and horizontal display multiplexer constitute the primary circuits that:

1) convert the sweep voltage to binary form to generate X values to be written into memory, or

2) read the X values from memory by counting sync cycles and causing the external logic to read stored data from memory and produce a vertical signal (Y value) for each corresponding X value.

During acquisition cycles, the 10-bit up/down counter, controlled by the up/down interlock, operates in a loop with the external 10-bit digital-to-analog converter to derive the equivalent (X value) of a sample section of the sweep voltage. From the counter, the 10-bit output is applied to the 10-bit up/down register. During display cycles, the 9-bit display counter counts sync pulses to derive the X value. Either the 10-bit up/down register output or the display register output is applied to the horizontal multiplexer under control of the SELECT signal from the PLA. From the multiplexer, the output is applied to the memories.

Address Registers and Buffers. Address counting is accomplished by registers U2022, U2016, and U2012. These count INCR/ $\overline{\text{ADRS}}$ (increment address) pulses after having been reset to zero by the $\overline{\text{CONT W}}$ (control write) signal from the vertical section. From the address register, the outputs are applied to tristate buffers U1022 and U1016, which buffer the 10-bits of address from the counters and the DSR/$\overline{\text{W}}$ (digital storage read/write) signal line from the vertical section interface logic and multiplex those signals onto the HD (horizontal display) lines and R/$\overline{\text{W}}$ (read/write) line to the memories. These buffers are enabled only during the bus grant portion of the cycle for display of memory data. At all other times, horizontal control IC U2032 outputs control the HD lines to determine the memory address for update of memory data.

Tracking Analog-to-Digital Converter. As discussed previously, the 10-bit digital-to-analog converter operates as part of the loop that derives a binary equivalent of the SWP (sweep) input signal from the Sweep board. Converter U2036 accepts the output from the U2032 10-bit up/down counter and converts that output to an analog current that is subtracted from the sweep signal, which is applied at the edge connector pin 60 and through buffer U2044B. The result of this subtraction is then supplied to up comparator U2038A and down comparator U2038B, to produce the UP or DOWN signal, as appropriate to control the direction of the count of the 10-bit up/down counter in U2032. The counter then counts in the appropriate direction, thereby changing the digital-to-analog converter output to reflect the proper value. Overflow detector U1032 and underflow detector U1034 prevent the counter from counting too high or too low.

Update Marker Circuits. From U2032, the HD (horizontal display) signals are also applied to 10-bit latches U1024 and U1018. The outputs of these latches are applied to 10-bit digital-to-analog converter U2034. From the converter, the output current is applied through buffer U2044A, where it is converted to a voltage, to comparator U2042, which compares it with the sweep voltage and applies the output voltage to digital one-shot U1014A. The period of this one-shot is determined by counter U2024 under control of the low DISP ENBL (display enable) signal from the PLA in the horizontal control IC U2032. DISP ENBL, when high, indicates that valid data are to be transferred. Conversely, when DISP ENBL is low, the lack of valid data indicates retrace. One-shot U1014A produces the INTENSITY signal that is used to temporarily prevent counting by the 9-bit display counter in U2032, thereby effectively stopping the beam for a short time and causing a bright spot on the marker trace (cursor) to indicate the X point being updated. Also note that buffer U2044A also produces the HORIZ SIG (horizontal signal) that is sent to the Deflection Amplifiers.

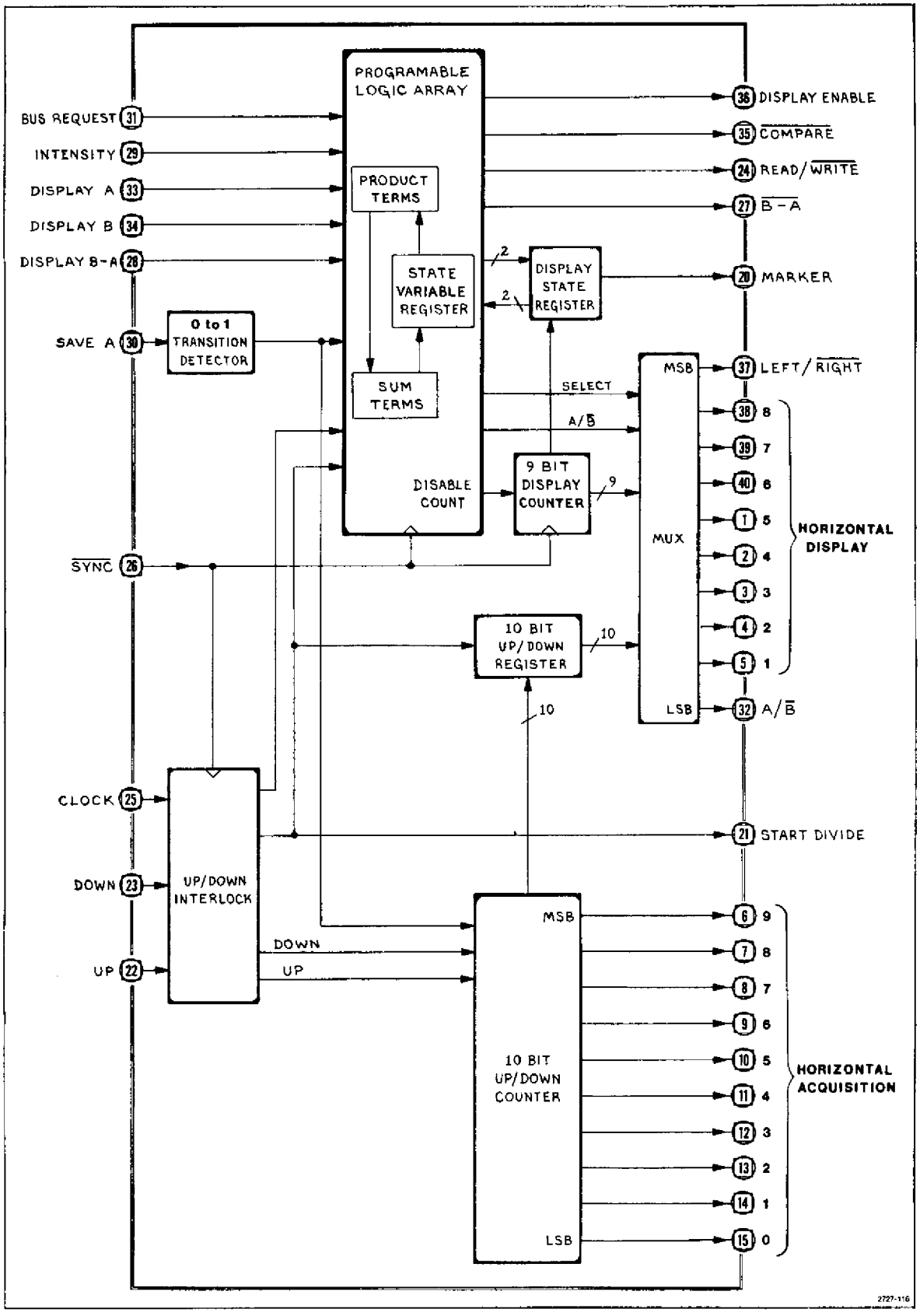


Fig. 5-13. Horizontal control IC block diagram.

Fast Retrace Blanking. Between the display of the B memory contents and display of the A memory contents, a fast retrace occurs. This retrace, unlike that following the A memory display (cursor), is not required to be seen and is thus blanked. This is accomplished by blanking control flip-flop U1014B, which is controlled by the most significant bit of the memory address and the display enable signal during a marker cycle.

Memories. Integrated circuits U1026 and U2026 provide 8k bits of random access memory for storage of the 1024 data points used in the digital storage system. Addressing is controlled by address tristate buffers U1022 and U1016 during display of memory data and by horizontal control IC U2032 during memory update.

DEFLECTION AMPLIFIERS 

Refer to the block diagram adjacent to Diagram 28. The Deflection Amplifier selects from among several inputs to generate the drive signals for the crt plates, and generate a signal to drive the auto-focus portion of the Z-Axis circuit. Input signals are from the Horizontal Sweep, Readout, Video Filter, and Digital Storage circuits.

Horizontal Section

Signal lines HORIZ SIG (from the Digital Storage circuits) and SWEEP (from the Sweep circuit), through edge connector pins 49 and 51, are applied to switch IC U7055. One half of U7055, under control of the STORAGE OFF signal from the Digital Storage circuits, selects either HORIZ SIG or SWEEP inputs. When the STORAGE OFF line is floating or pulled high, the SWEEP signal is selected; when the line is pulled low, the HORIZ SIG signal is selected. The selected signal is then divided down from 1 V/div to 0.5 V/div by resistive divider R7051 and R7081 and buffered by U7073. From buffer U7073, a sample of the signal is applied to a rear panel connector via edge connector pin 48. The signal is also applied to the other section of switch U7055 along with the HORIZ R/O signal from the Readout circuits. Selection between these two signals is controlled by the R/O OFF signal, also from the Readout circuits, through edge connector pin 3. When R/O OFF is floating or pulled high, the signal from buffer U7073 is transmitted through the switch; when the line is pulled low, the HORIZ R/O signal is selected.

From U7055, the signal is applied to a shaper network to compensate for non-linearity in the crt deflection characteristics. This network consists of resistors R3051, R3052, R4059, R4058, R4057, R4062, R4061, and R3059, plus diodes CR4052, CR4051, CR4058, and CR3058. Note that HORIZ POS voltage from the front panel via edge connector pin 47 through resistor R2053 is applied to the shaper circuit so the shape correction factor relates to the crt deflection.

The shaped signal is then applied through preamplifier U2060 to the Deflection Amplifier circuits. The feedback path around U2060 includes Horiz Gain adjustment R1055 to calibrate the amount of compensation required for deflection sensitivity.

The horizontal deflection amplifier consists of two similar circuits, one for each horizontal deflection plate. One circuit is an inverting amplifier, the other operates in-phase. Inputs to the inverting side are through the parallel combination of resistors R3049, R3048, and capacitor C4057 to Q4038A. High-frequency response compensation is provided by the series connection of resistor R3048 and variable capacitor C4057. High-frequency feedback is controlled by capacitor C3043.

Input to the non-inverting side is through resistors R5020 and R5029 to the base of Q4025A. Resistors R3019 and R5035 set the dc level for the feedback loop to the base of Q4025B. Variable capacitor C5021 provides adjustment to set transient gain. Again, high frequency feedback is controlled by capacitor C2021.

Gain of each amplifier section is approximately 20. (Horizontal deflection sensitivity of the crt is approximately 21.3 V/div per side.) Each section is single-ended and incorporates at the input side, a gain-degenerated dual (for temperature compensation) PNP transistor connected as a differential amplifier. For example, Q4038B of the right deflection amplifier drives emitter follower Q4047.

Signals with a low rate of change drive the output transistor through R5037, P3033. As the rate of rise increases, the drop across R5037 increases and when it reaches 0.6 V, either Q4035 or Q4042 are biased on. These transistors provide the high current drive for the output transistors. When the signal rate of change is low, Q1043 drives the crt deflection plate and Q1049 provides bias current for the amplifier. As the rate of rise increases, C3039 couples signal to the base of Q1049; Q1049 provides the positive drive to the deflection plate, Q1043 the negative drive. Each output transistor can provide a 200 V excursion in about 1 μs.

The horizontal amplifiers operate with approximately 1 mA of bias current in the output stage, as set by the current through resistor R3031 and the resistors connected at the base and emitter of output transistor Q1049. The current through resistor R3031 also provides the operating current for the dual input stage (Q4038A and B). Emitter follower Q4047 operates at approximately 2.5 mA. The output stage is degenerated for fast steps by emitter resistors R1045 and R1034. For a 0 V input, the output operating level is set by current from the −15 V source through resistor R4033. Dc feedback resistor R3045 sets this output level at approximately 142 V.

The preceding description of the right-hand (inverting) section is applicable to the left-hand (non-inverting) section except for the circuit element designations.

Output signals from the second half of switch U7055 are also supplied to the auto focus amplifier (IC's U6093, U6102, and transistors Q7097, Q7103). Amplifiers U6093 and U6102 produce a negative absolute value signal that is three times higher in amplitude than the signal from switch U7055. This amplified signal is then used to produce a shaped current by transistors Q7097, Q7103, and resistors R7102, R7101, R7107, R7108, to apply to the Z-Axis Interface circuit through edge connector pin 48. This signal will sink from 0 to approximately 0.8 mA of current from an external node at a voltage of approximately 0 V.

Vertical Section

Signal lines VIDEO FILTERS OUT (from the Video Processor circuits) and VERT SIG (from the Digital Storage circuits), through edge connector pins 53 and 52 respectively, are routed through switch IC U6055. One side of U6055, under control of the STORAGE OFF signal from the Digital Storage circuits, selects either VIDEO FILTERS OUT or VERT SIG. Note that the VIDEO FILTERS OUT signal is buffered by IC U7065 to prevent changing load transients from affecting the signal level. When the STORAGE OFF line is floating or pulled high, the buffered VIDEO FILTERS signal is selected; when the line is low, the VERT SIG signal is selected. The selected signal is inverted and clamped to ground by U6065. (Both the VIDEO FILTERS OUT and VERT SIG signals are specified at 0.5 V/div with 0 V for the baseline and positive voltages above the baseline. The signal is re-inverted and offset by buffer U6073 so center screen represents 0 V. From buffer U6073, a sample of this centered signal is applied to a rear panel connector via edge connector pin 46. The signal is also applied to the other side of switch U6055 along with the VERT R/O signal from the Readout circuits. Selection between these two signals is controlled by the R/O OFF signals; also from the Readout circuits. When R/O OFF is floating or pulled high the signal from buffer U6073 is transmitted through the switch. When the line is pulled low, the VERT R/O signal is selected.

The vertical section shaper (resistors R3061, R4065, R4067, R3071, R3064, and diodes CR4063, CR4064) and preamplifier (U2062) operate the same as the horizontal section. Transistor Q4078 limits positive excursions to approximately one division below the top of the screen to protect the output stages from being overdriven.

The vertical output stages are similar to the horizontal stages with the exception of higher bias current. Current flow of approximately 1 mA through resistors R3095 and R3098 result in approximately 5 mA in the output stages. Resistors R5081 and R5099 are of less resistance than R5041 and R5027 in the horizontal section to correct for the increased current in dual input stage transistors Q4083 and Q4101.

Comparator U6024 compares the level of the signal from baseline clamp U6065 with a reference level set by divider R7032 and R7034 to produce the CLIP signal for the Z-Axis Interface circuits. The CLIP line is pulled low when the Video signal is more negative than the reference level (approximately 1 division above baseline), and pulled high by R7021 if the signal is more positive than the reference level.

CRT READOUT 

The Crt Readout assembly stores readout characters and generates deflection and Z-Axis signals to display the characters. It also handles the frequency dot marker display. Both characters and frequency dot displays are time-shared with the spectrum trace.

Generating Readout

Crt readout is handled by sequential logic, clocked at 3.41 MHz, supplied by the Processor board. The readout circuitry (Fig. 5-14) comprises:

1) readout on timing, RAM for character storage;

2) character counter to access the RAM and control the scan;

3) character generator to unblank the crt beam;

4) D/A converters to deflect the crt beam;

5) instrument bus interface to store characters and control display. A more detailed block drawing is provided with the schematic, Diagram 29.

Up to 32 characters can be displayed in a line across the top of the crt and another line across the bottom; either of two sets of characters (page 1 or page 2) can be selected for display. Page 1 is used for normal front-panel readout; page 2 can be used for message input over the GPIB.

Readout-On Timing. Characters are drawn one at a time, allowing a portion of the spectrum to be drawn between each character. The character duty cycle is in the range of 10% to 25% because it varies with the character drawn. The time-sharing is pseudo-random, reducing the effect of gaps in the spectrum display by moving them on the trace.

The readout-off time is set to 175 μs by one-shot U2044 (Fig. 5-15). Flip-flop U2036B asserts GEN ON after U2044 times out, allowing a character to be drawn. When the character is finished, $\overline{\text{ROW 0, COL 0}}$ resets the flip-flop, which retriggers the off-timer. The ON control bit must have been set by the microcomputer to get readout (as discussed below under Instrument Bus Interface).

If BLANK (MSB of the character data) is not set, the GEN ON flip-flop unasserts R/O OFF through AND-gate U1038B; this switches the readout deflection signals onto the deflection amplifier inputs on Diagram 28. BLANK can be set by the microcomputer as it loads a space into the character RAM so the readout does not use time for the spectrum trace to scan a blank character.

Character Scan. Although the 8678 character generator IC is often used in raster scans, in this application it is used to write complete characters, as shown in Fig. 5-16. A character is drawn as a pattern of dots in an 8 x 8 matrix where the top row and first three columns are blank. These blank dots allow for beam retrace and spacing. The idle position between characters is indicated on the figure.

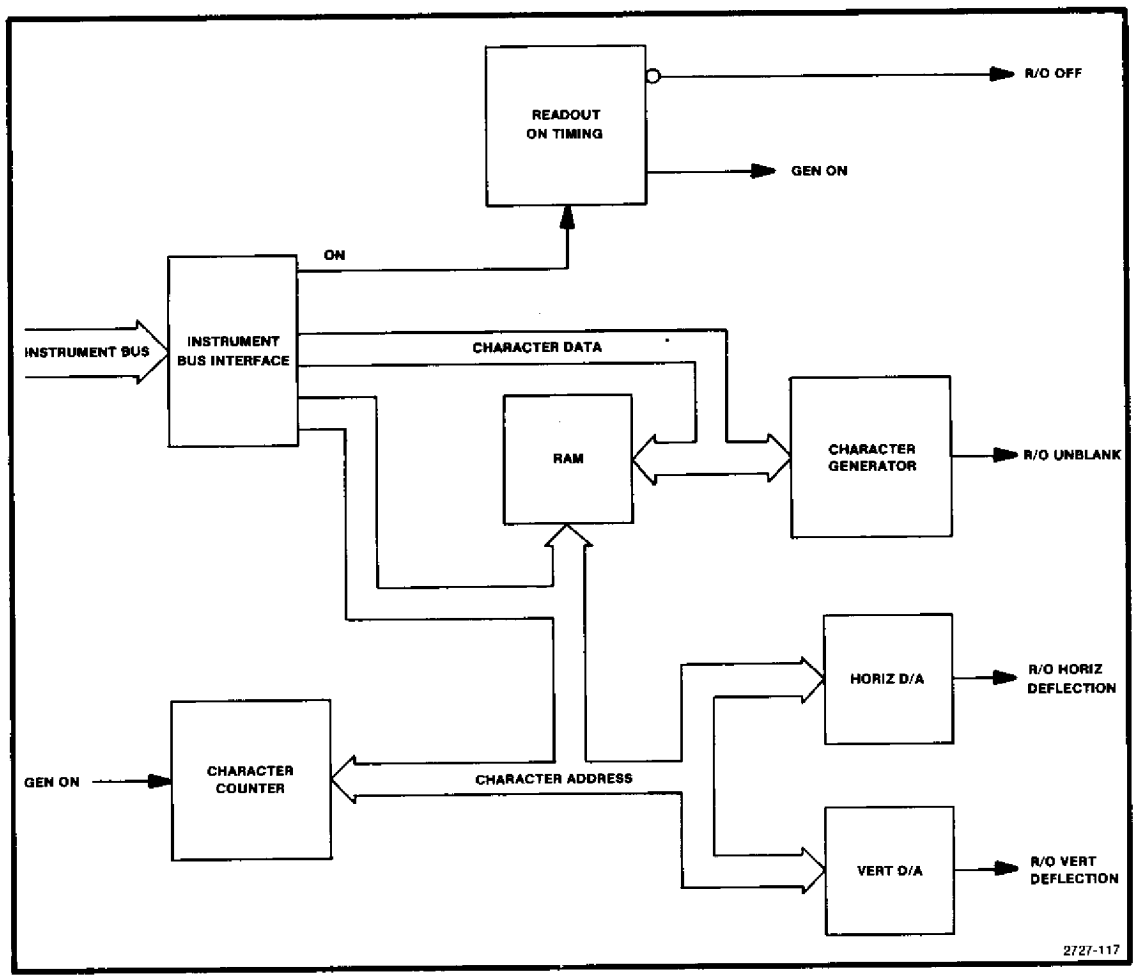


Fig. 5-14. Simplified crt readout block diagram.

Character counters synchronize the horizontal and vertical scan with the Z-axis signal from the character generator IC to draw the character. These counters, U2016, U2012, and U2018, are wired as a module 4096 counter to count the column (bits 0—2), the row (bits 3—5), and position of the character (bits 6—11). Bits 6 through 10 represent the horizontal position and bit 11 the vertical position (top or bottom). The position bits also address the character in RAM (assuming the readout is turned on by the microcomputer). The counters are enabled only when the generator has control of the crt beam (GEN ON) and INC is high; INC low stops the beam to write a dot on the crt.

The counters are wired to force the D/A converters to step through the character horizontally a row at a time. At the same time, the pattern of dots is accessed under the control of the timing decoder logic, U1022A and U1014. The AND-gate and decoder combine to control the character generator (U1028), which generates the correct pattern of blanking to draw the pattern of dots for the character.

The 8678 (U1028) character generator IC (Fig. 5-17) contains a ROM with the correct pattern of 64 bits for each of the 64 characters in its repetoire. The bit patterns are accessed by a decoder that operates on the ASCII code on the character generator inputs. The pattern of bits is multiplexed one 8-bit line at a time into a shift register that is clocked out one bit at a time to control the crt Z-axis.

Character Generator Timing. The character generator timing lines are called DOT, LINE, $\overline{LE}$, and $\overline{CLR}$. Each cycle of DOT clocks one dot (bit) out of the shift register. A positive transition on LINE switches the next line (row) of dots onto the shift register inputs; the dots are latched by a negative transition on $\overline{LE}$ (load enable), setting up the shift register to display another row of dots. $\overline{CLR}$ resets the line counter to begin drawing another character.

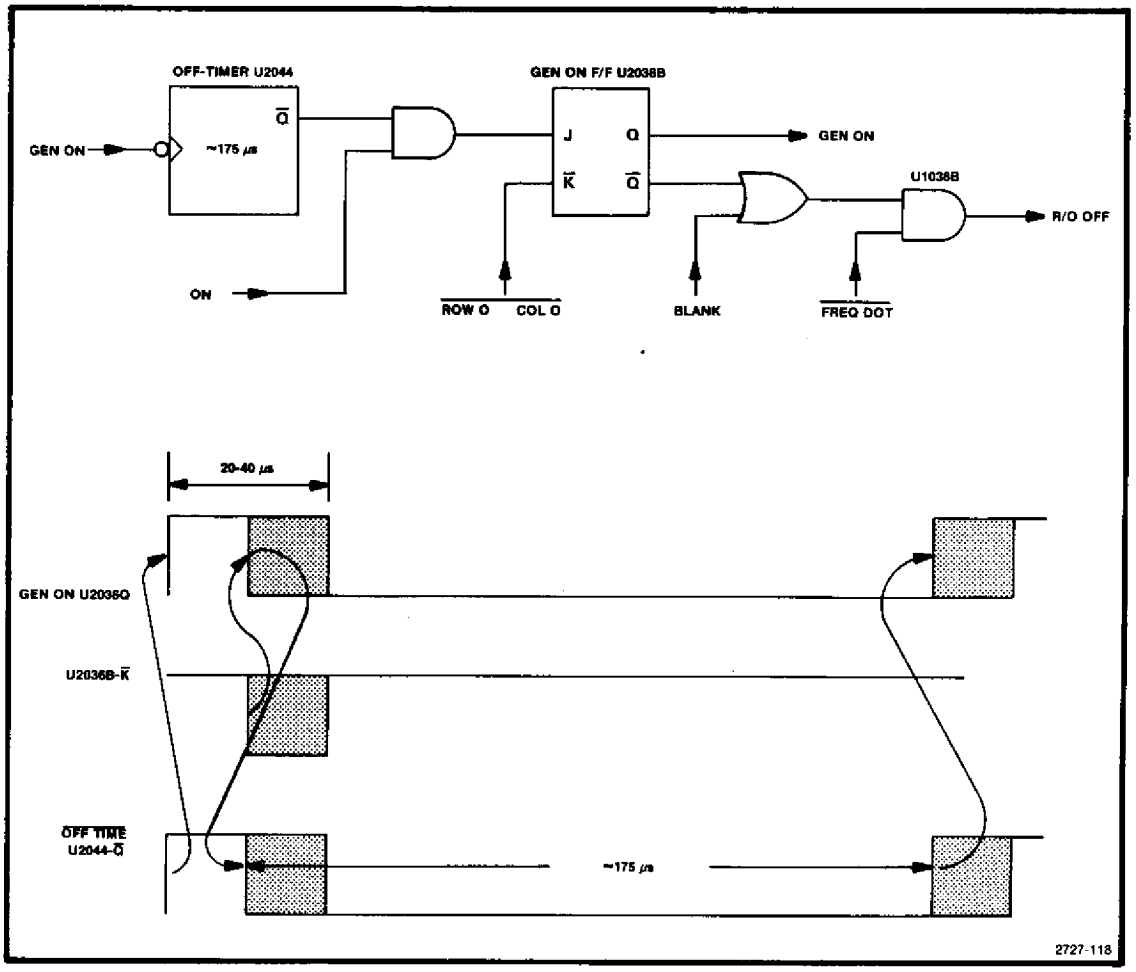


Fig. 5-15. Character on/off timing.

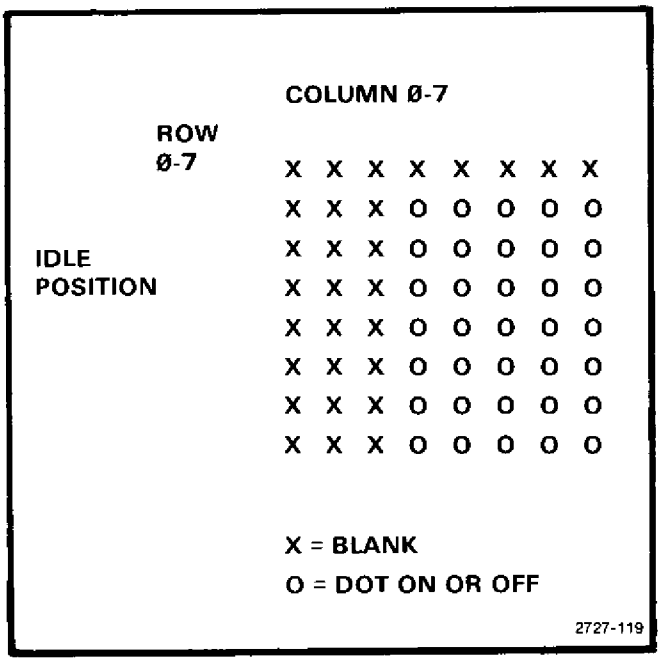


Fig. 5-16. Character scan.

DOT is ANDed from GEN ON, INC, and CRT CLK by U1022B. Inversion by the gate restores the phase relationship of the DOT input and the inverted clock used by the rest of the character generator. $\overline{LE}$ is gated by U1022A when the character counter reaches column 2. This loads the shift register with the next row of dots, which is displayed starting at column 3. LINE advances the line (row) counter after the scan of the current row begins to set up the next row of dots on the shift register inputs; this occurs at column count 4. $\overline{CLR}$ is asserted only once during the scan of each character. It is decoded by U1014 when the character counter reaches row 1, column 0, the first non-blank row of dots scanned in each character.

See the character timing figure (Fig. 5-18) for the sequence of events to scan a character. At 1 on the figure, the character generator finishes a character. When the counter advances, decoder U1014 asserts $\overline{ROW\ 0\ COL\ 0}$, resetting the GEN ON flip-flop on the next clock. This stops the counter at row 0, column 1 (2 on the figure). When U2044 completes the time-out period and again sets the GEN ON flip-flop, the character counter resumes the scan, first causing $\overline{LE}$ (at 3) and LINE (at 4). Just before the scan enters the actual character area (at 6), CLR resets the character generator line counter (at 5). The break (7 on the figure) indicates that the scan continues. After the character is scanned, the scan returns to the idle state; 8 and 9 correspond to 1 and 2 on the timing figure.

Dot Delay. Each bit shifted out of the character generator is the value of a dot in the 8 x 8 matrix: 0 for a blank and 1 for a dot that is to be written. As the scan progresses at better than 3 MHz, a rather faint character display might be expected. To brighten the dots that are written, a shift register inserts some dot delay by stopping the counters while holding the crt beam unblanked. The dot delay timing is shown in Fig. 5-19.

A high on the character generator output (U1028-11) sets the dot delay shift register (U1036A,B,D) input high (assume Q of U1036C is high). It also sets the unblanking flip-flop (U2036A) J input high; once set, the flip-flop unblanks the beam during the rest of the dot delay cycle. Because the shift register must have completed any previous dot delay before entering a new cycle, the character generator high output also gates INC (increment) low at U1022C (assuming the microcomputer has turned on the readout). On the next clock, the highs on the two register inputs are latched.

Meanwhile, INC low puts the character counters on hold and disables the gate (U1022B) that clocks the character generator U1036C, the INC flip-flop, stores the low on INC at the next clock, putting a low on the dot delay shift register input.

Successive clocks propagate the dot through the shift register; when it emerges after three clocks, it is inverted by U1018C to reset the unblanking flip-flop and gate INC high. This sets U1036C again on the next clock. INC remains high if the value of the next dot is 0 or is gated low to repeat the dot delay cycle if the next dot is 1.

Instrument Bus Interface

The microcomputer controls the crt readout and frequency marker dot over the instrument bus through the following ports:

Port	Hex Address
Control	5F
Address/data	2F

Decoder U2038 asserts CONTROL when it sees a value of 5 on the upper four bits of the instrument bus address lines and $\overline{DATA}$ when it sees a value of 2. The decoder must be enabled by GEN ON low and DATA VALID high on the instrument bus. The false transition of DATA VALID causes the addressed port to latch the data on the instrument bus.

Control Port. The control port (U2034) turns the readout on or off, steers data sent to the address/data port, and controls the mode of the frequency marker dot. The lower four bits are defined (see Table 5-7). Bits are numbered in this discussion as on the instrument bus—starting at zero. However, the D and Q pins of U2034 (and some other ICs) are numbered as on their data sheets, starting at one.

Bit 0 turns the crt readout display on (1) or off (0). When set, this bit gates the off-timer to the GEN ON flip-flop J input through U1038D, enables the INC gate (U1022C), and steers the position counter onto the character RAM address inputs through multiplexer U1024. When cleared, this bit places an address, latched in U2024, on the character RAM address inputs.

Bit 1 interprets data sent to the address/data port as an address (1) or data (0) for the character RAM. Setting this bit disables the character RAM for input and sets up the clock signal to latch the address.

When this bit is set, $\overline{Q2}$ of U2034 gates a high on the output of U2032A. This high prevents input to the character RAM (U1026) by setting its R/W input high. This high also disconnects the instrument bus from the character RAM data inputs by disabling U2028. Meanwhile, $\overline{Q2}$ of U2034 is low, enabling U2032D to gate the clock signal that latches the address. The positive clock transition is applied to U2024 when DATA VALID goes false at the end of a write cycle to the address/data port, releasing $\overline{DATA}$.

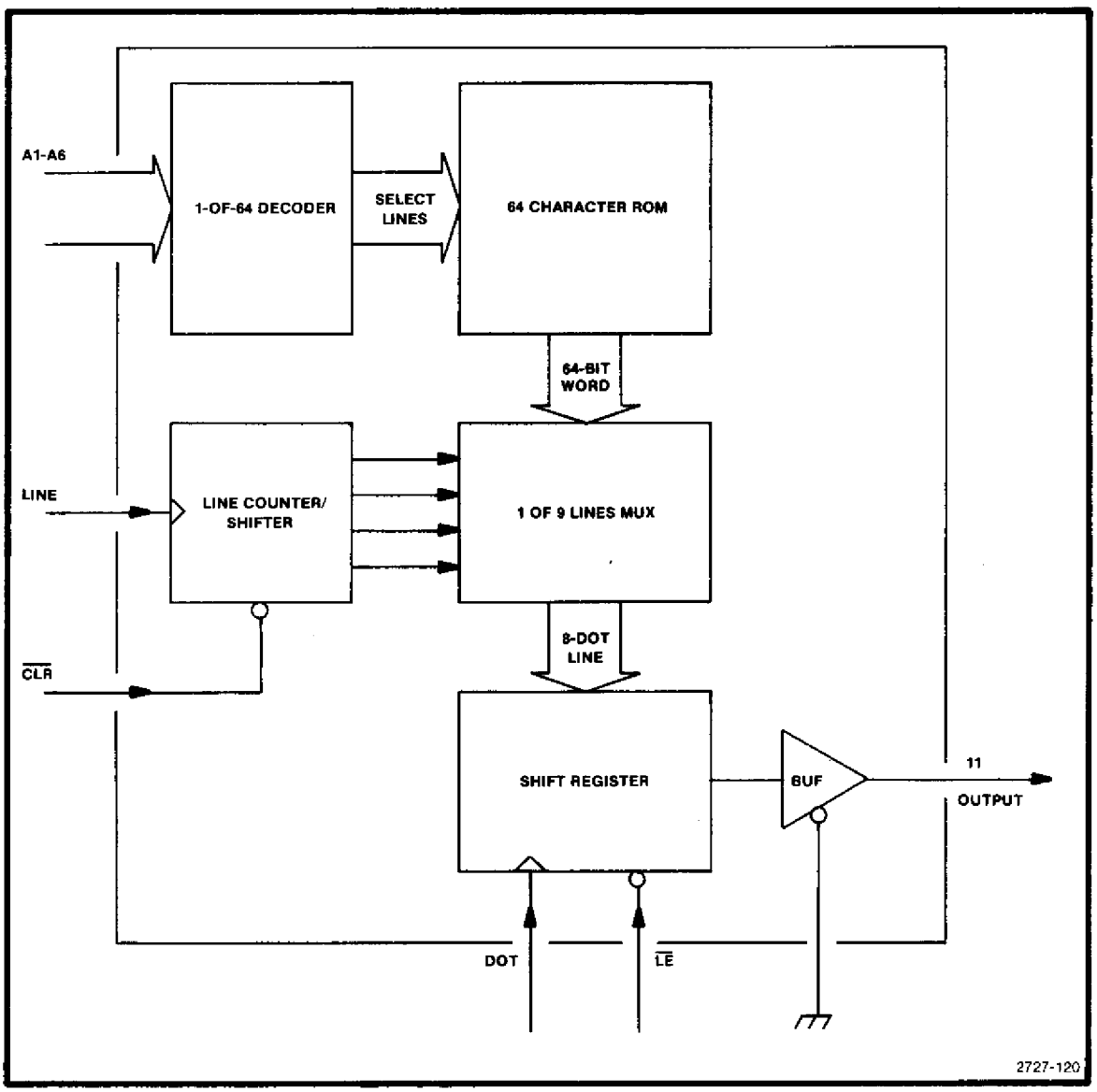


Fig. 5-17. Character generator (U1028) block diagram.

When this bit is cleared and DATA is asserted, U2032A enables the character RAM for input and passes the data through U2028.

Bit 2 selects information from the two halves of character RAM space. When set, this bit selects page 1, the normal front-panel readout. When cleared, this bit selects page 2, a 64-character space that may be loaded with messages via the GPIB.

Table 5-7
CONTROL PORT

Bit	Function
0	Readout on/off
1	Address/data
2	Page 1/page 2
3	Max Span dot

Bit 3 controls the frequency dot marker. This bit is set in MAX SPAN mode to position the frequency dot with BFRD TUNE VOLTS from the first local oscillator. When cleared, this bit centers the frequency dot on the spectrum display.

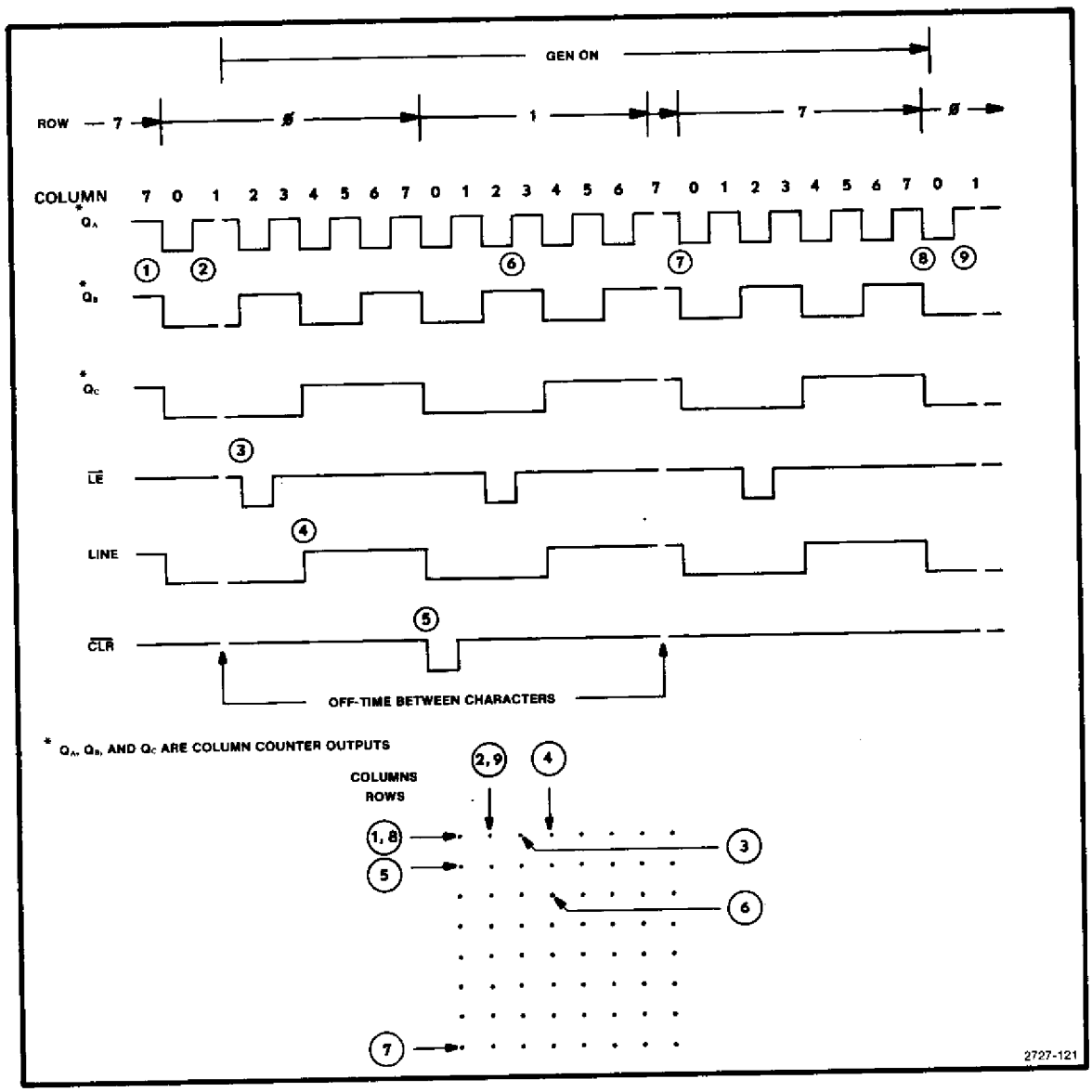


Fig. 5-18. Character scan timing.

Address/Data Port. The microcomputer loads characters for crt display through the address/data port. Each character requires four write cycles:

1) bit 2 in the control port is set for an address transfer;

2) the address in character RAM is sent to the address/data port;

3) bit 2 in the control port is cleared; and

4) the data is sent to the address/data port. The bits are defined in Table 5-8. Bits 0—5 are the lower six bits of the character RAM address or are the ASCII code for the character.

Table 5-8
ADDRESS/DATA PORT

Bit	Function
0—5	Address of ASCII code
6	Vertical shift
7	Blank

Bit 6, when set, shifts upper readout characters to the center of the crt (and lower readout characters off the bottom of the screen). This may be used with page 2 characters to give prominence to a message sent to the operator.

Bit 7 is used to reduce readout display overhead. It is set when a space is transferred to the character RAM so the readout does not steal time from the spectrum trace to scan a blank. When set, this bit prevents the GEN ON flip-flop from gating R/O OFF low through U2032C.

Frequency Dot Marker

The frequency dot marker is refreshed immediately after the last character position in the lower readout is scanned. Normally, the marker is centered on the screen just below the upper readout as a pointer for the center frequency readout. When MAX SPAN is selected, however, the dot marker moves to a point on the display that corresponds to the center frequency value.

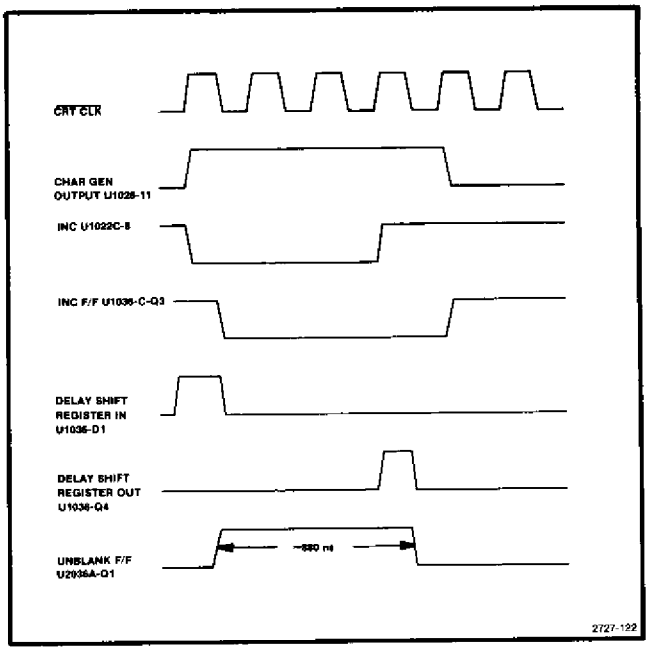


Fig. 5-19. Dot delay circuit timing.

The negative transition of $\overline{TOP}$ triggers the marker generator. A simplified diagram of the circuit and its timing is shown in Fig. 5-20.

U2042A delays the marker dot to allow retrace while gating $\overline{FREQ\ DOT}$ low to set up the display. $\overline{FREQ\ DOT}$ affects the readout deflection outputs in the following ways.

The horizontal output is connected either to ground for a center-screen dot or BFRD TUNE VOLTS for a max span pointer. TUNE VOLTS is proportional to the center-frequency readout offset from the center of the frequency range.

Bits 4 and 5 at the vertical D/A input are asserted to shift the crt beam below the upper readout (the row counter inputs are zeros).

R/O OFF is gated low to switch the deflection amplifier inputs for a display using the marker dot horizontal and vertical signals.

When the retrace one-shot times out (about 5.9 μs), it triggers the unblanking one-shot, U2042B, which sets R/O UNBLANK high for about 5 μs. This refreshes the dot. The corresponding low on the one-shot's inverted output holds $\overline{FREQ\ DOT}$ low until the dot marker is drawn. CR1041, R1041, and C1041 slow the rise on the other input of U1038A to prevent a spurious signal on FREQ DOT.

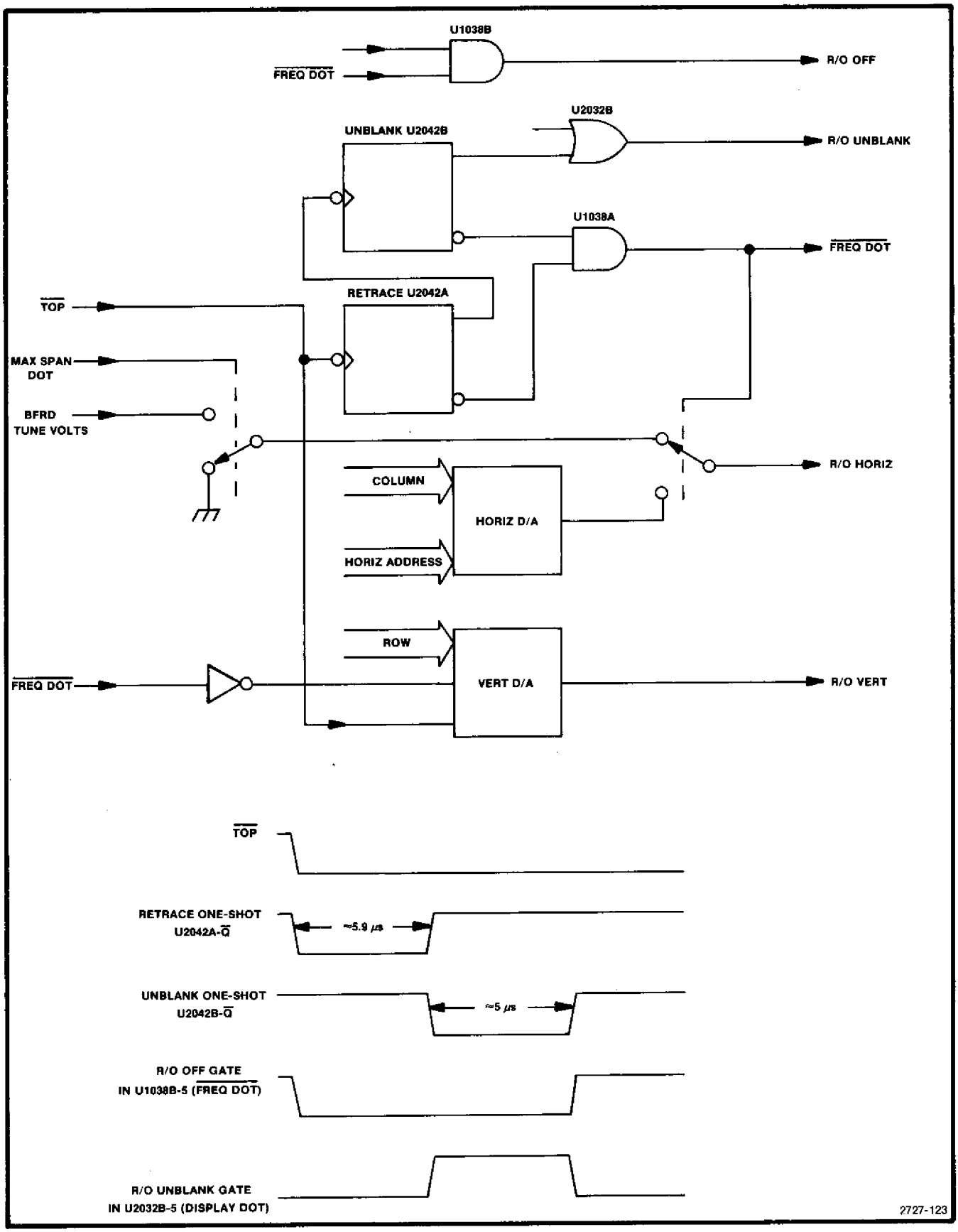


Fig. 5-20. Frequency dot marker circuit and timing.

Z AXIS CIRCUITS 30

Refer to the block diagram adjacent to Diagram 30. The Z-Axis circuits take the various beam control inputs such as SWP GATE, INTEN, etc., combine them, and furnish the drive currents and bias voltages required to operate the crt electrodes. The Z-Axis circuit consists of the Intensity Control Logic circuits, which control the crt beam current for normal signal display operations. It also includes the unblanking gates which furnish current to the Z-Axis Drive Amplifier to drive the crt control grid. The Z-Axis circuits also include voltage-setting circuits for astigmatism, crt trace rotation coil, geometry, and other crt electrode voltages.

Z-Axis Driver Amplifier

The Z-Axis Drive Amplifier Q3047, Q4058, and Q4059, is driven by two sources, exclusive to each other: U2038B/Q2042 drives the amplifier during readout display periods, and U2038A/Q2044 drives the amplifier during sweep display periods. IC U2039 is an AND-NOR gate that is connected to provide the logic to one input of NAND gate U2038A which turns Q2044 on or off. The R/O OFF line and the output of U2039 must both be high for U2038A to furnish current to Q2044. Table 5-9 lists the conditions under which U2039 will output a high to U2038A.

Table 5-9
J2039 TRUTH TABLE

U3046 output (line 28)	0	0	0	1	1	1	0	0	0	
CLIP	0	0	0	0	0	0	1	1	1	
Z Axis Blank	1	1	1	1	1	1	1	1	1	
Storage Off	0	0	1	0	0	1	0	0	1	
SWP GATE	1	0	1	1	0	1	1	0	1	
U2034, pin 13	0	0	0	0	0	0	0	0	0	

Only the combinations shown in the truth table plus a high on R/O line will gate a low out of U2038A. When U2038A output is low, emitter current is furnished to Q2044, which in turn will furnish current through R2051 (the input resistance of the Z-Axis Driver Amplifier) to Q3047. IC U2034 is a single-shot that produces a 3 μs pulse to blank the crt beam during trace return between readout and signal display.

The other source of input current to the Z-Axis Drive Amplifier is Q2042. This transistor is turned on by U2038B when R/O UNBLANK is high and the R/O OFF is low.

Q1028 serves as a current source for the divider (R1030-R1025) that sets the operating point for Q2042 and Q2044 which sets the intensity level. Diodes CR1045 and CR1043, connected from base to base of Q2042 and Q2044, limit the display intensity by preventing the bases from going more positive than about 0.6 V above the emitter voltage of Q2022. This circuit, which includes the adjustment (R1027), sets the maximum current for both Q2042 and Q2044.

The Z-Axis Drive Amplifier is an operational amplifier consisting of transistors Q3047, Q4058, Q4059, and related components. The input resistance for the amplifier is R2051, and the feedback resistor is R3052. The output is clamped by diodes CR3059 and CR3066, to protect the amplifier from transient surges in case of crt arcing.

Transistors Q1017 and Q1015 provide current for the trace rotation coil. The adjustment (R1021) sets the current so the displayed trace is aligned with the graticule.

Transistors Q3045, Q4063, Q4065, and related circuitry are for use in future applications.

HIGH VOLTAGE SUPPLY 31

Refer to the block diagram adjacent to Diagram 31. The High-Voltage Supply furnishes the −3860 V to the crt cathode, the filament voltage for the crt, and provides dc restoration for the Z-AXIS DRIVE signal. The circuit consists of the following:

1) the high-voltage oscillator, which produces the crt filament voltage and the 200 Vac that is stepped up and applied to the voltage doubler circuit;

2) the voltage doubler, which rectifies and filters the high voltage for application to the crt cathode;

3) the high-voltage regulator, which samples the high voltage and regulates the operation of the high-voltage oscillator;

4) the Z-Axis clipper and rectifier circuits, which couple the Z-AXIS DRIVE signal to the crt control grid.

High Voltage Oscillator. This circuit consists of transistor Q1073, transformer T2065, and associated components. The output of the oscillator, approximately 200 Vac, is coupled across T2065, where it is stepped up for application to the Voltage Doubler, and stepped down for application to the crt filament.

Voltage Doubler. The voltage doubler consists of CR4041, CR4035, C4027, C5021, C4024, R3038, and R1039. The output of the doubler is taken off the anode of CR4035 and applied to the crt cathode. Reference voltage for the regulator is taken off the end of R1039.

High-Voltage Regulator. This circuit consists of amplifier U4083 and surrounding components. The high voltage is applied through a voltage divider consisting of R1017B and R1017C, which is connected through R1042 to +15 V. The sample of the high voltage at pin "U" is applied through R4075 to the input of comparator U4083. The correction signal, in the form of dc drive, is applied to the base circuit of Q1073 to set the oscillator current.

Diodes CR4078 and CR4077 at the input to U4083, protect the input against excessive voltage excursions. The circuit consisting of CR4071, R3079, and R4074 protect the oscillator if the +100 V supply should fail. Normally, CR4071 is back-biased. If the +100 V is not present, CR4071 conducts and clamps the input negative; the output of U4083 swings negative and Q1073 remains cut off. This circuit ensures that Q1073 will begin oscillating only after U4083 switches. Diode CR3077 (in the output circuit of the regulator) prevents the base circuit of Q1073 from going negative.

Z-Axis Clipper. This circuit consists of diodes CR1056 and CR1046, plus associated components. The 225 Vac from pin 8 of T2065 is coupled through C1058 and R1048 to the junction of CR1046 and CR1056. The regulator circuit consisting of VR1041 and R1051, hold the cathode of CR1046 at +110 Vdc. Thus, if the Z-AXIS DRIVE signal is +110 Vdc, the two diodes clip the incoming 225 Vac to a total excursion of 1.2 V. If the Z-Axis peak-to-peak voltage is at ground potential, the ac voltage at the junction of the two diodes swings from ground to +110 V. The voltage that passes the clipper circuit is coupled through C1031 to the Z Axis rectifier. The Z-AXIS DRIVE signal is also coupled directly to this circuit, where it is coupled through C1041 to the crt grid circuit.

The clipped Z-Axis drive signal is rectified by CR2044 and CR2046, which are the principle components of the second section of the Z-Axis circuit. The rectified voltage is then fed to the grid of the crt. C1041 couples the fast changes of drive voltage to the crt grid to speed up the response of the grid circuit. Neons DS2052, DS2057, and DS2058 protect the crt from high-voltage arcs from external sources. Resistors R1044 and R1053 protect CR2046 and CR2044 respectively, from external high voltage surges.

FREQUENCY CONTROL SECTION

The Frequency Control section performs the tuning and sweeping (scan) function for the 1st LO (Local Oscillator), and 2nd LO. It contains the following major circuits.

Sweep. The Sweep circuit accepts trigger inputs from line, internal, and extenal sources in addition to the normal free-run mode of operation. It also receives external horizontal and manual sweep inputs. The circuit produces a PEN LIFT signal for chart recorder applications, a SWEEP GATE signal for crt display blanking, a SWEEP signal to drive the crt horizontal axis and digital storage circuit, plus a ramp for the Span Attenuator circuits and eventually the 1st LO and 2nd LO.

Span Attenuator. This circuit inverts and attenuates the incoming ramp signal, as required to sweep the 1st and 2nd Local Oscillators.

Center Frequency Control. The Center Frequency Control circuit provides a tuning voltage for the 1st and 2nd Local Oscillator circuits that results in a linear center frequency change as the front panel FREQUENCY control is changed. The circuit is directly controlled by the microcomputer, so remote control of the frequency is possible, by way of the GPIB rear-panel connector. The COARSE TUNE VOLTS signal from this circuit is applied to the 1st LO Driver circuits for summing with the SPAN signal to drive the 1st LO. The FINE TUNE VOLTS signal is applied to the phaselocked 2nd LO.

1st LO Driver. The 1st LO Driver performs the following:

1) combines the COARSE TUNE VOLTS signal with the SPAN signal and produces current to drive the 1st LO;

2) produces the mixer bias voltages;

3) produces the BUFFERED TUNE VOLTS signal that is applied to the Display section;

4) produces a reference voltage that is used in the 1st LO Driver circuit;

5) produces a supply voltage for the 1st LO.

SWEEP 32

An overall block diagram of these circuits appears adjacent to Diagram 32. The Sweep circuit provides the ramp signal to drive the Horizontal Deflection Amplifier and the 1st Local Oscillator Driver. The sweep generator also provides signals for an external plotter pen, the Z-axis, and digital storage circuits.

The Sweep circuit consists of four major circuits:

1) the digital control circuits, which receive and decode the address and instructions from the microcomputer, select the sweep rate, holdoff time, trigger source, sweep mode, and control interrupts to the microcomputer;

2) the trigger circuits, which process and multiplex the three trigger signals;

3) the sweep generator, which generates the voltage ramp that drives the Deflection Amplifiers, Digital Storage, and the swept oscillators;

4) the sweep control circuit, which generates the SWEEP GATE and PEN LIFT signals, and determines the holdoff time for the sweep generator.

Trigger Circuits

The sweep generator can be triggered from three sources: internal, external, and line signals. All three signals are converted to TTL levels by input buffer stages. Each output signal is coupled to U3034, the trigger multiplexer.

The external trigger signal (EXT TRIG/HORIZ IN) is capacitively coupled from the external trigger input connector through a compensating network to the input of the external trigger buffer and level shift circuit, which consists of differential amplifier Q2084 and buffer U1052E which converts the signal to TTL level. Diodes CR2075/CR2086 protect the input stage from excessive voltage.

The signal for the internal trigger circuit (VIDEO FILTER OUT) from the video filter is applied through Q2074 coupled to differential amplifier Q1078, then converted to TTL levels by U1052F. Diodes CR1088 and CR1089 protect the input of Q1078 from excessive voltage.

The input line trigger signal amplitude is large enough to overdrive Q1047 producing a line trigger output 0 to +5 V peak. Diode CR1035 protects the emitter-base junction from reverse bias.

Upon instructions from U2043, the "2" side of dual trigger multiplexer U3034 selects the trigger signal for the clock input of trigger flip-flop U2034B. The flip-flop clocks on the rising edge of the applied signal, so the complement of the signal at the D input appears at the output at the first trigger after the multiplexer enable goes to a low state.

Upon instructions from U2043, the "1" side of U3034 selects either the output of U2034B or the high state at pin 6. When the multiplexer is disabled, which occurs during sweep holdoff time, the multiplexer output is low. If free run is selected, the output goes high as soon as the multiplexer is enabled. However, if the sweep is in a triggered mode, the output will not go high until the next trigger occurs. This transition restarts the sweep. When the sweep starts again, U2034B is set by sweep state flip-flop U5026A in preparation for the next sweep end-holdoff-trigger cycle.

Sweep Generator

The sweep generator consists of the timing current generator (timing resistor selector U6102, voltage regulator U4095, U6092B, and surrounding circuitry), the integrator (U4101, U5085C, Q3100, U5085A, Q3090, U5085D, Q3095, and associated components), and the reset clamp (U5085B, Q2107, and surrounding circuitry).

The timing reference voltage for the sweep circuits is set by U4095 to −10 V. Divider R5092—R5094 sets the voltage at the non-inverting input of U4101 to −8 V; feedback sets the inverting input at the same potential. This input is driven by the output of multiplexer U6102. Operation of the circuit is as follows: The 1 to 10 V reference, from U4095, is applied to U6092B, which changes this level to −12 V, which connects to one side of the timing resistors connected to U6102. A 4 V difference then appears across the timing resistor. Multiplexer U6102 decodes instructions from U3042 (the 0F port latch), and connects only one resistor or resistor pair to its output pin, which then becomes the current source for integrator U4101. The multiplexer input codes for each of the sweep rates are listed with the description of the Digital Control circuits. Sweep accuracy adjustment R5105 is set to compensate for errors in this voltage or in the timing capacitor values. The timing capacitors are matched, so one adjustment can be used for the entire set.

The timing current furnished by the multiplexed resistors varies such that 1/I is proportional to a 2-5-10 sequence. Decade switching of sweep rates is provided by timing capacitor selection (C3079, C2094, and C2098). Capacitor C2098 is used in all sweep rates, and for the 20 μs to 1 ms range. When a sweep rate of 2 ms to 100 ms is selected, the output of open collector comparator U5085D goes high, causing FET Q3095 to conduct and place timing capacitor C2094 in parallel with C2098. Likewise, when a sweep rate of 200 ms to 10 s is selected, U5085A causes Q3090 to switch C3079 in shunt with the other two capacitors. (The 10 s/div sweep rate is only used in the auto-sweep routine, or in the 496P.) VR2093, R2099, CR2101, CR2102, and CR2103 clamp the output to prevent the negative sweep retrace from causing the FETs to conduct.

A voltage divider consisting of R2012, R2013, and R2017 set a switching threshold of about +7.4 V at the input of the right-of-screen comparator U2015B. At the beginning of the sweep, the output of integrator U4101 is −8 V. The output voltge rises linearly to +7.4 V, then U2015B switches, placing a low at the input to U5016B. This causes the output PEN LIFT signal to move high. This signal was low up to this point, because of the high SWP GATE signal at the beginning of the sweep cycle and the high level at the output of U2015B. The PEN LIFT signal switches before retrace occurs to give the pen time to lift. The sweep rises in amplitude until it reaches +8 V, causing U2015A (the end-of-sweep comparator) to switch. (The same divider that was mentioned earlier sets a switching threshold of about +8 V at the non-inverting input of U2015A.) The low state from U2015A is inverted by U1052A and the high output applied to U4016A sets U5026A. The high state at the Q output of U5026A is inverted by U4016B, causing the SWP GATE signal to move low, blanking the crt display. The low out of U4016B also gates PEN LIFT high through U5016B.

The low state now at the $\overline{Q}$ output of U5026A is coupled to the holdoff circuits and the inverting input of U5085B, an open collector comparator. IC U5085B switches, its output rises, and Q2107 conducts. This clamps the output of the integrator to its input, and discharges the timing capacitors. Transistor Q2107 continues to conduct until a trigger is furnished to U4016C, which resets U5026A to begin the next sweep cycle.

When manual scan or external sweep is selected, both inputs to U5016D are high, which causes its output to be low. This causes the output of comparator driver U5085C to switch high and turn FET Q3100 on. As a result, feedback resistor R3105 is placed across U4101, converting it into an amplifier. Timing capacitor C2098 is still in the circuit, but its small capacitance has negligible effect at the low frequency of operation in this mode. The output of U5016C also resets U5026A and the SWP GATE remains high. These levels will remain until the output of U4101 overcomes the switching point of U2015A.

The input signals from manual scan and external horizontal are multiplexed by U6102 and applied to U4101. Since the summing node of the amplifier is not at ground, R7091 and R4093 shift the dc levels of the manual and external drive signals, respectively. IC U6092A is an inverting buffer for the external voltage; VR6086 is for overvoltage protection.

The sweep ramp from U4101 is applied through voltage divider R6058—R6052, which reduces the ramp voltage to U6061 to 11 V, centered around 0 V. The output of U6061 is applied to the Digital Storage and Deflection Amplifier circuits. The extra volt of sweep amplitude is used to deflect the beam 0.5 division off screen on each side.

The sweep signal from U4101 is also applied to U6071, which amplifies the ramp to 22 V, centered around 0 V. This signal drives the Span Attenuator and ultimately the 1st Local Oscillator.

Sweep Control

This description is based on the assumption that the sweep is in neither the manual nor the external mode. At the end of the sweep, U5026A is in set state. Its $\overline{Q}$ output is low, which causes the output of U4026C (the holdoff generator) to switch high. This starts the holdoff cycle. The holdoff time between sweeps must be sufficiently long for the timing capacitors to discharge and for any transient responses in the swept circuits to die. As the sweep time increases, the holdoff time is increased.

When the output of U4026C rises, the holdoff capacitors charge to +5 V through R3027. Capacitor C1013 is always in the holdoff circuit. When U2043 latches Q4 or Q5 high, this produces a low out of U4026F or U4026E which increases holdoff time by adding C3028 or C3027 into the holdoff circuit. Diodes CR3034 and CR3035 protect the two inverters from reverse voltage transients that might pass through the capacitors.

When the voltage on the capacitors reaches +5 V, the output of U2015D switches high. If single sweep has not been selected, both inputs to U3061C will now be high and its output will enable trigger multiplexer U3034. When the next sweep is ready to run (depending on the trigger selection conditions), pin 7 output of U3034 switches high. This change in state gated through U4016C resets U5026A and begins the next sweep cycle.

When the single sweep mode has been selected, pin 2 of U5016A is high. IC U2034A, the single-sweep flip-flop, must furnish a low to U5016A to enable U3034 to trigger a single sweep. This enabling occurs when the microcomputer clocks U2034A. When the sweep starts, U5026A resets and sets U2034A. This ensures that only one sweep occurs for each microcomputer command.

Single-sweep mode is usually selected by front-panel commands; however, in some modes, the microcomputer will command single sweep. The microcomputer can also abort a sweep and start another with the next trigger; a pulse from U5052C, through U3061B, to pin 3 of U4016A sets U5026A and causes the sweep circuit to reset.

Digital Control Circuits

As mentioned throughout this description, the sweep is controlled by latched codes and pulses. The board has two ports for receiving information from the microcomputer, addresses F and 1F. IC U5033 buffers the data inputs, decreasing the loading instrument bus. Address decoder, U5043, decodes the address bus and strobes the data onto the board. Each output of U5043 goes to low when the corresponding port is addressed. Data is latched on the rising edge of this strobe, which is the trailing edge of Data Valid. The output of U5043 is inverted (U1052B inverts 1F; U1052C inverts 0F), then combines with the proper data bus line to form each bit of pulsed data. The pulse is at the low state for the duration of the Data Valid pulse (approximately 1 μs).

IC U3042 latches the data from port 0F. The combinations of D3 to D7 select the sweep rate; D3 and D4 control timing capacitor selection, and D5 to D7 control timing resistor selection. Table 5-10 lists the sweep rate selection codes. D2 is high during single sweep operations; otherwise, it is low. D0 commands a single sweep cycle.

Table 5-10
SWEEP RATE SELECTION CODES

Sweep Rate	D7	D6	D5	D4	D3
20 μs/div	1	1	0	1	1
50	1	0	1	1	1
100	1	0	0	1	1
200	0	1	0	1	1
500	0	0	1	1	1
1 ms/div	0	0	0	1	1
2	1	1	0	0	1
5	1	0	1	0	1
10	1	0	0	0	1
20	0	1	0	0	1
50	0	0	1	0	1
100	0	0	0	0	1
200	1	1	0	0	0
500	1	0	1	0	0
1 s/div	1	0	0	0	0
2	0	1	0	0	0
5	0	0	1	0	0
10	0	0	0	0	0
Manual	1	1	1	1	1
External	0	1	1	1	1

IC U2043 latches the data from port 1F. Line Q6, when high, enables an interrupt to the microcomputer at the end of a sweep. This is done as follows: At rest, U2024A is reset and the low at its Q output holds U2024B in the set state. When the sweep ends (which constitutes an interrupt event), the positive edge out of inverter U1052A clocks U2024A to the set condition and the $\overline{Q}$ output of U2024A, through inverter U3061A causes Q4052 to conduct, forcing $\overline{\text{SER REQ}}$ low. The microcomputer responds by setting the interrupt read line low; that is, it polls all addresses serially, which eventually places a high at AB7 and POLL simultaneously (Fig. 5-21). This causes a high at the output of U4016D (the Q of U2024A is low, since the flip-flop is now set), and saturates Q4051, pulling the D4 line low (this identifies the sweep board as the service request originator). Now, the microcomputer clocks an interrupt clear pulse to reset U2024B. This in turn, resets U2024B which sets U2024A. The circuit has returned to its reset stage.

IC U5052A and U5052B produce the interrupt read and clear signals. When the microcomputer wants to read or clear, it sets the POLL line high. Address bus line AB7 is high to read, resulting in a low at the output of U5052A. AB7 is low to clear, which results in a high at the output of U5052B.

SPAN ATTENUATOR 33

The Span Attenuator, under control of the microcomputer, selects the appropriate attenuation factor for the incoming sweep signal, to establish the frequency span. Refer to the block diagram adjacent to Diagram 33. The Span Attenuator consists of digital control circuits, which receive and decode the address and instructions from the microcomputer; the input amplifiers, which perform noise reduction and signal inversion on the incoming sweep signal; the digital-to-analog converter, which attenuates the sweep signal to the desired amplitude for driving the 1st LO Driver; and the decade attenuator, which provides three decades of attenuation for the output signals.

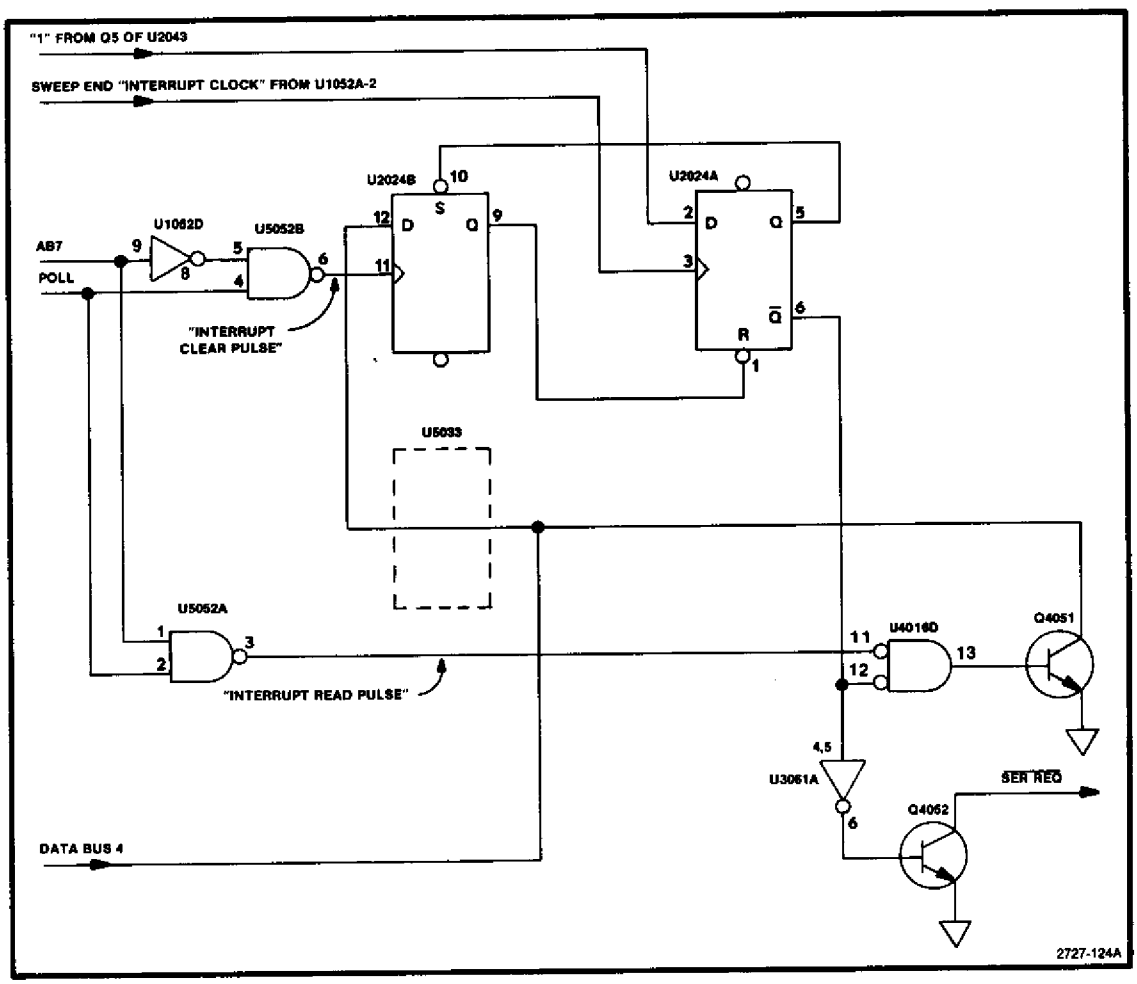


Fig. 5-21. Sweep "interrupt" circuits.

Digital Control

Decoder U5025 decodes the address information from the address bus and sends a low signal to either of the two latches, U1025 (address 75) or U2015 (address 76), when a latch is addressed and the DATA VALID line moves high. (The data is stored in the latches on the trailing edge of the DATA VALID signal.) Logic buffer U4015 reduces loading of the data bus. Latch U1025 stores data that controls the eight least significant digits of the span attenuation factor. Latch U2015 stores data that controls the two most significant digits of the span attenuation factor, and other functions on the board. When a span attenuation factor is selected, the microcomputer selects an address and places the first byte of the data on the bus. The DATA VALID signal causes the data to be stored in one of the two latches. Then the second address is called and the next byte is stored in the other latch. The block diagram illustrates the significance of each bit in tables near the affected circuit. A logic 1 represents the more positive of two levels or high state, and a logic 0 represents the more negative of two levels or low state.

Input Section

The sweep signal and its ground reference are applied to differential input buffer U3036. Any signals or noise induced in the two signal transmission paths are cancelled by this stage.

The following stage consists of amplifier U3032, plus switching transistors Q2025, Q2028, and Q2023. Different mixing modes require the 2nd LO frequency to either increase or decrease to increase the signal frequency. Thus, this circuit is a unity gain amplifier that can be changed from inverting to non-inverting under bus control. When line Q8 of latch U2015 is low, Q2023 conducts more and its collector moves positive to about +5 V. This in turn causes both Q2025 and Q2028 to conduct. Pin 3 of U3032 is effectively grounded, the sweep signal is applied through R3032 to the summing node of the amplifier, and the gain of the stage is −1. If line Q8 is high, Q2023 does not conduct and the voltage at its collector falls to nearly −15 V. Neither Q2025 nor Q2028 are now in conduction, so the sweep signal is applied to pin 3 of U3032, and pin 2 is disconnected. Now, the gain of the stage is +1.

Digital-To-Analog Converter

The magnitude of the sweep signal is determined by the desired frequency span, band, and option installed in the instrument. The microcomputer calculates the proper magnitude for each combination, and sends the appropriate codes to the data latches, which in turn control the attenuation factor of the digital-to-analog converter. This stage consists of converter U1042, amplifier U2042, and a complementary pair, Q2062 and Q3056, that form the output current buffer.

Figure 5-22 illustrates a simplified two-bit digital-to-analog converter. The circuit works by current division. Since the summing node of the amplifier is at ground potential, the magnitude of the current through a resistor is not affected by the position of the switch that selects that resistor. For example, when switch S1 is at position B, the current is shunted to ground. When S1 is at position A, the current through R1 becomes part of the total output current. Thus, the output current can be 0, 1/4, 1/2, or 3/4 of the total current available. Because of the resistance ratios, the ratio of the output voltage to the input voltage equals the ratio of the output to the total current ($V_{out}/V_{in} = I_{out}/I_{total}$). In this 2-bit converter, there are 2_2 or 4 output values possible. In the actual 10-bit converter, there are 2_{10} or 1024 output values ranging from 0 to 1023/1024 of the input.

In converter U1042, each internal resistance is switched in or out by a CMOS FET (internal to the device). The CMOS inputs are each protected by a series input resistor. Since the sweep signal is applied to the V_{ref} input, U1042 serves as a digitally controlled attenuator for the sweep signal.

The attenuated sweep signal from U1042 is applied to U2042, an operational amplifier. It in turn drives an output current buffer, consisting of complementary pair Q2062/Q3056. The pair is biased to produce an output current of about 10 mA in the absence of an applied signal. This eliminates crossover distortion of the output signal. Diodes CR2051, CR2053, CR1051, and CR1049 provide temperature stabilization for the bias current in the stage. When high current is passing through the pair, diodes CR1056 and CR1061 clamp the voltage across the emitter resistors to reduce voltage drop.

Feedback for the output stage is provided by R1056, plus an internal resistor in U1042. The internal feedback resistor ensures better temperature tracking. The internal resistor provides a gain slightly less than unity; R1056 increases the stage gain and permits gain calibration, as described below.

One-of-four decoder, U4025, using the data from the Q4 and Q5 lines from U2015, controls three sections of a quad FET switch, U3025. (RC circuit inputs of each FET control line filter out noise from the digital circuits.) The code is exclusive; i.e., only one FET is switched on at a time. See Table 5-11 for a listing of the codes. When a FET is switched on, it connects a calibration adjustment potentiometer to the summing node of the operational amplifier. Adjustment R1065 sets the 1st LO tune coil sweep, R1071 sets the 1st LO FM coil sweep, and R1067 sets the 2nd LO span.

Table 5-11
CALIBRATION CONTROL SELECTION CODES

U4025		
Pin 3	Pin 2	Selected Adjustment
low	low	R1065 (main coil)
low	high	R1071 (FM coil)
high	low	R1067 (2nd LO)

Decade Attenuator

Since accuracy of the digital-to-analog converter is specified as a percentage of full scale, the accuracy decreases as the attenuation is increased. To maintain accuracy at 1%, it is never used at an attenuation factor of more than ten. If more attenuation is required, the decade attenuator, consisting of K4072, K3075, K3065 and the connected divider network, provides further sweep attenuation of X0.01, X0.1, and X1. See Fig. 5-23 for a simplified circuit diagram.

The "2" side of U4025 is controlled by data on the Q6 and Q7 lines from U2015. The "2Y" outputs of U4025 are applied through buffer amplifiers in U4042 to select the appropriate attenuation factor for the output sweep. Table 5-12 lists the states required to energize the attenuation relays. A diode across each relay coil protects the driving circuit from inductive feedback transits.

Table 5-12
ATTENUATION SELECTION CODES

U2015		
Pin 15 (Q67)	Pin 16 (Q7)	Attenuation Factor
low	low	X1 (K3065)
high	low	X 0.1 (K3075)
low	high	X 0.01 (K4072)

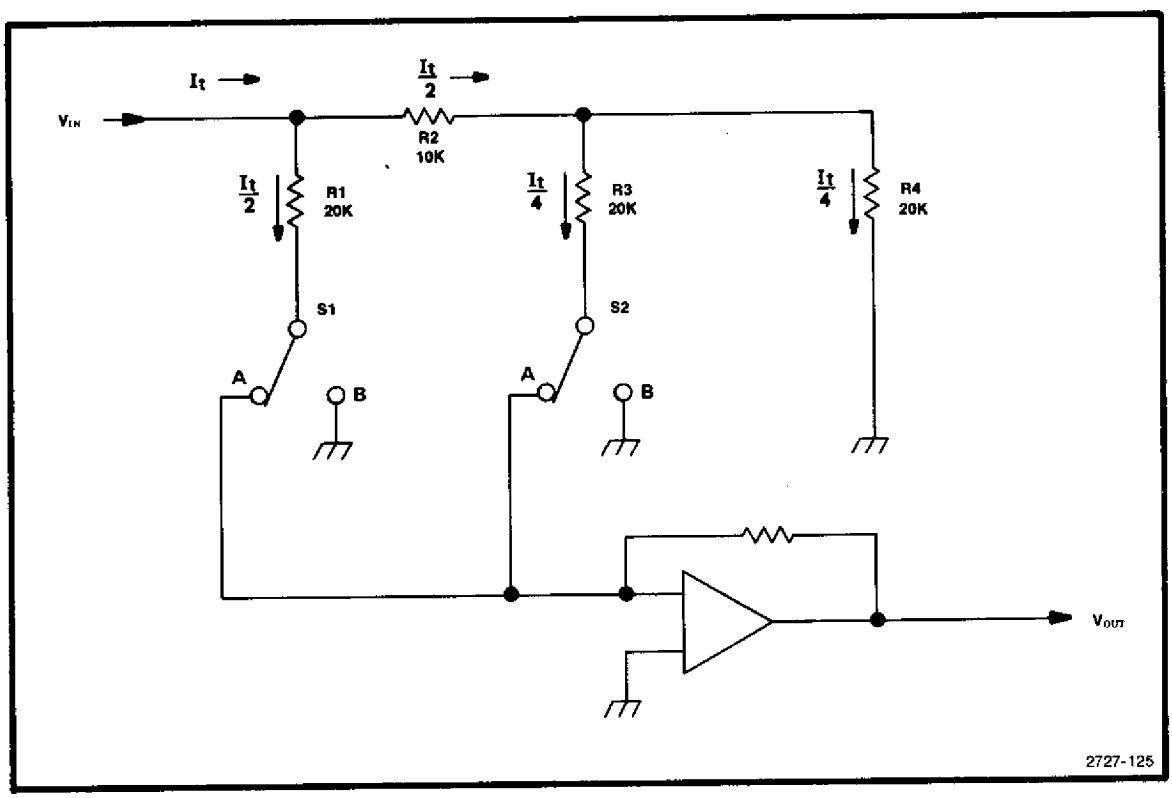


Fig. 5-22. Simplified digital-to-analog converter.

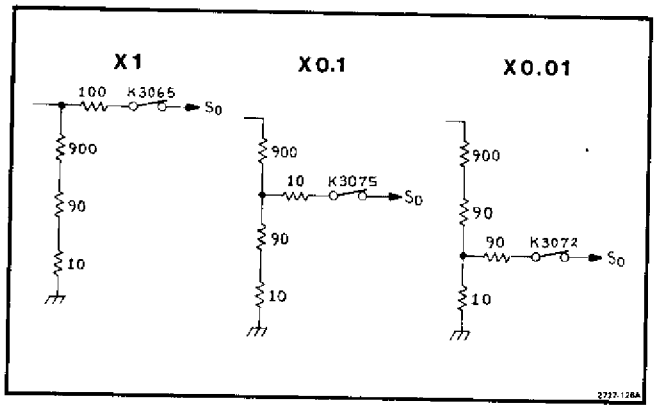


Fig. 5-23. Simplified span decade attenuator.

CENTER FREQUENCY CONTROL 34

Refer to the block diagram adjacent to Diagram 34. The Center Frequency Control circuits form the electrical interface between the front-panel controls and the converter stages in the 496/496P. The circuit receives digital information and instructions from the microcomputer, and converts it to a coarse and fine tuning voltage that is applied to the other elements of the Frequency Control system.

The Center Frequency Control circuits consist of the following major blocks:

1) the Digital Control circuit, which buffers and decodes the addresses and other data to control the other circuits;

2) the coarse and fine storage registers (latches), which store the numerical bytes that control the DAC (digital-to-analog converter) stages;

3) the coarse and fine DAC stages, which convert the digital inputs from the storage registers into analog current and voltage equivalent values;

4) the coarse and fine track/hold amplifiers, which store the analog output values during the approximation routine, and compare the stored value and the approximated value for the microcomputer;

5) the write-back circuits, which inform the microcomputer when the stored value and the approximated values are equal.

Operating Modes

Some explanation of the design principles of the circuit is required before the operation of the circuit can be discussed. DAC devices are now available that can furnish the resolution required to tune the analyzer in small enough steps. To achieve the necessary amount of resolution, two DAC devices are used in tandem. However, this method can cause some errors and non-monotonic behavior in the overall converter circuit.

To circumvent this problem, the outputs of the tandem DAC units are summed together so that the two units are overlapped by three bits (that is, the MSB of the low-order DAC is weighted equally with the third least significant bit, or 2E-10 bit). The overlap means that the lower DAC will have sufficient range to monotonically tune the output of the converter over the entire range of the analyzer, but only if the proper codes of the lower DAC device can be found. Now, suppose that the tandem DAC is loaded as follows:

Upper order:
1 0 0 0 0 0 0 0 0 0 0 0 0
Lower order: 1 1 1 1 1 1 1 1 1 1 1 1 1

The contents of the devices are shown overlapped to illustrate the bit weighting. Now assume that the low-order device is to be incremented one bit. The MSB of the low-order device must be moved into the high-order device before the low-order device can be incremented. Thus, the two must appear as shown below:

High-order:
1 0 0 0 0 0 0 0 0 1 0 0
Low-order: 0 1 1 1 1 1 1 1 1 1 1 1

If the high-order device operated with no overall linearity inaccuracy, the operation would now be complete, and the low-order incrementation could occur. However, the DAC device can vary by one LSB of the correct value; Fig. 5-24 illustrates a graph of the best and worst case output instances. Note that even in the worst case, the output may move only once every two or three state changes, but the output is always monotonic and within one LSB of the correct value.

If, in the example shown earlier, the high-order device is at point A in Fig. 5-24, incrementing the device to point B has no effect on the output. If the MSB of the low-order device is set to zero, as shown in the first example, the combined output will actually decrease. Ordinarily, the Center Frequency Control circuit can increment and decrement whenever the microcomputer commands without going through a special routine. However, as just described, some microcomputer adjustment is necessary to compensate for the disparity that usually occurs between the low-order and high-order DAC units.

The first operating mode is the tracking mode, where the preamplifier and integrator are connected together by the disconnect stage, and the entire unit acts as an operational amplifier. Figure 5-25 illustrates the basic circuit. While the circuit operates in this mode, the amplifier tracks the DAC stage, and sends the voltage out to the tuning circuits.

When the transfer of bits from the lower to the upper DAC is required, the microcomputer commands the circuit to shift to the hold mode. The command comes through the decoder to shut off the disconnect stage, and the preamplifier output is disconnected from the integrator. The integrator holds the voltage that was previously at the output for comparison, and the approximation cycle begins.

The microcomputer resets the low-order DAC to zero. Then, the highest order bit in the low-order DAC is set to one, and the circuit is queried to find if the DAC output and integrator output is greater or less than required. If less, the microcomputer loads the next lower bit in addition and queries the circuit once more. This process goes on until the two values are the same. Had the microcomputer found that the DAC output was greater than the integrator output at the first inquiry, it would have set the highest order bit to zero and loaded the second-order bit into the low-order DAC, then continued to load successively lower order bits, one at a time, until the circuit signalled that the comparison had reversed. By this process, which is known as the successive approximation method, the circuit finally reaches the point where the outputs are equal, and the microcomputer commands the circuit to shift back to the track mode.

Digital Control

The digital control circuits consist of buffer U2016, address decoder U2014, steering register U2022, and the steering gates (U2024A, U2024B, U2024D, U2026A, U2026B, and U2026C). Because of the quantity of data that must pass through these circuits, a steering register is used that has a separate address. The first byte of data, which is the steering byte, is clocked into U2022 by the ADDRESS 70 signal. The output levels are applied to the steering gates, and the circuit waits for the next byte. The microcomputer then furnishes the first byte of data to be sent to low-order fine-tune digital-to-analog converter DAC, for example, by way of storage register U3022. The byte is clocked into the register by the coincidence of low states at the inputs of U2026C; one from the steering byte, and the other from the ADDRESS 71 signal, which is used to clock the steered data bytes into the correct register. This continues until seven bytes of data have been clocked into the circuits, including the steering byte. The third output from U2014, ADDRESS 80, controls transistors Q2043 and Q1039, which enable the write-back function.

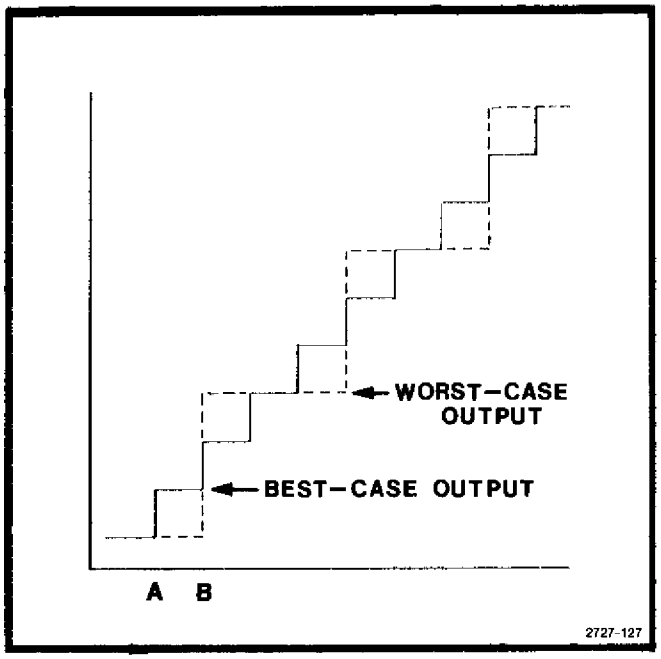


Fig. 5-24. DAC variance graph.

In addition to the six steering lines that drive the steering gates, U2022 also controls, by means of the Q1 and Q8 lines, the hold/track selector transistor for each converter side. Table 5-13 illustrates the format for ADDRESS 70. Addresses are expressed as hexadecimal numbers. Table 5-14 lists some of the significant states that are used to tune the DAC.

Table 5-13
ADDRESS 70 FORMATS

DB0	Fine Tune hold
DB1	Fine Tune low byte enable
DB2	Fine Tune mid byte enable
DB3	Fine Tune high byte enable
DB4	Coarse Tune high byte enable
DB5	Coarse Tune mid byte enable
DB6	Coarse Tune low byte enable
DB7	Coarse Tune hold

Storage Registers. Six storage registers are used in the circuit, (U1014, U1016, U1022, U3014, U3016, and U3022 respectively). Since both sets are identical, only the first three are described.

Data from U2016, the data buffer, is clocked into the registers each time a different tune voltage is required. U1022 feeds the lowest eight bits to the low-order DAC, U1026; U1014 feeds the highest eight bits of the high-order DAC, U1032; and U1016 feeds the remaining bits of both units.

Digital-To-Analog Converters. Each side of the converter has two DAC stages contained on sub-assemblies A46A1 and A46A3, (DAC 1200 Interface). These sub-assemblies plug into the Center Frequency Control board A46 through IC sockets J1024 and J1030 for the Coarse Tune circuit, and J3024 and J3030 for the Fine Tune circuit. Since both sets operate the same, only Coarse Tune units are described. Each DAC furnishes current or voltage outputs that are commensurate with the data applied. Figure 5-25 is a functional block diagram of each DAC, illustrating its operation in the circuit. U1020 is the low-order DAC, U1026 is the high-order DAC. U1012 and Q1018 are configured as an operational amplifier to provide the drive for U1024.

The DAC unit is basically a programmable current generator that drives an internal high quality operational amplifier. In this configuration, only the low-order DAC uses the internal operational amplifier. Thus, the low-order unit operates in the voltage output mode, and the high-order unit operates in the current output mode. The two devices feed the two inputs of preamplifier U1044, which sums the two inputs, amplifies the sum, and sends it through the switching circuit to the integrator.

Since the DAC units generate the dc voltage that tunes the entire instrument, noise and extraneous signals must be kept at a minimum. Thus, each tune voltage is provided with an isolated ground system, U1042A/U1042B for the Coarse Tune voltage converter, and U1041A/U1041B for the Fine Tune voltage converter.

Track/Hold Amplifiers

Since the coarse and fine amplifiers are identical in operation, only the coarse amplifier is described here. The amplifier consists of preamplifier U1044, control transistor Q2044, storage gate FET Q2046, and integrator amplifier U2046.

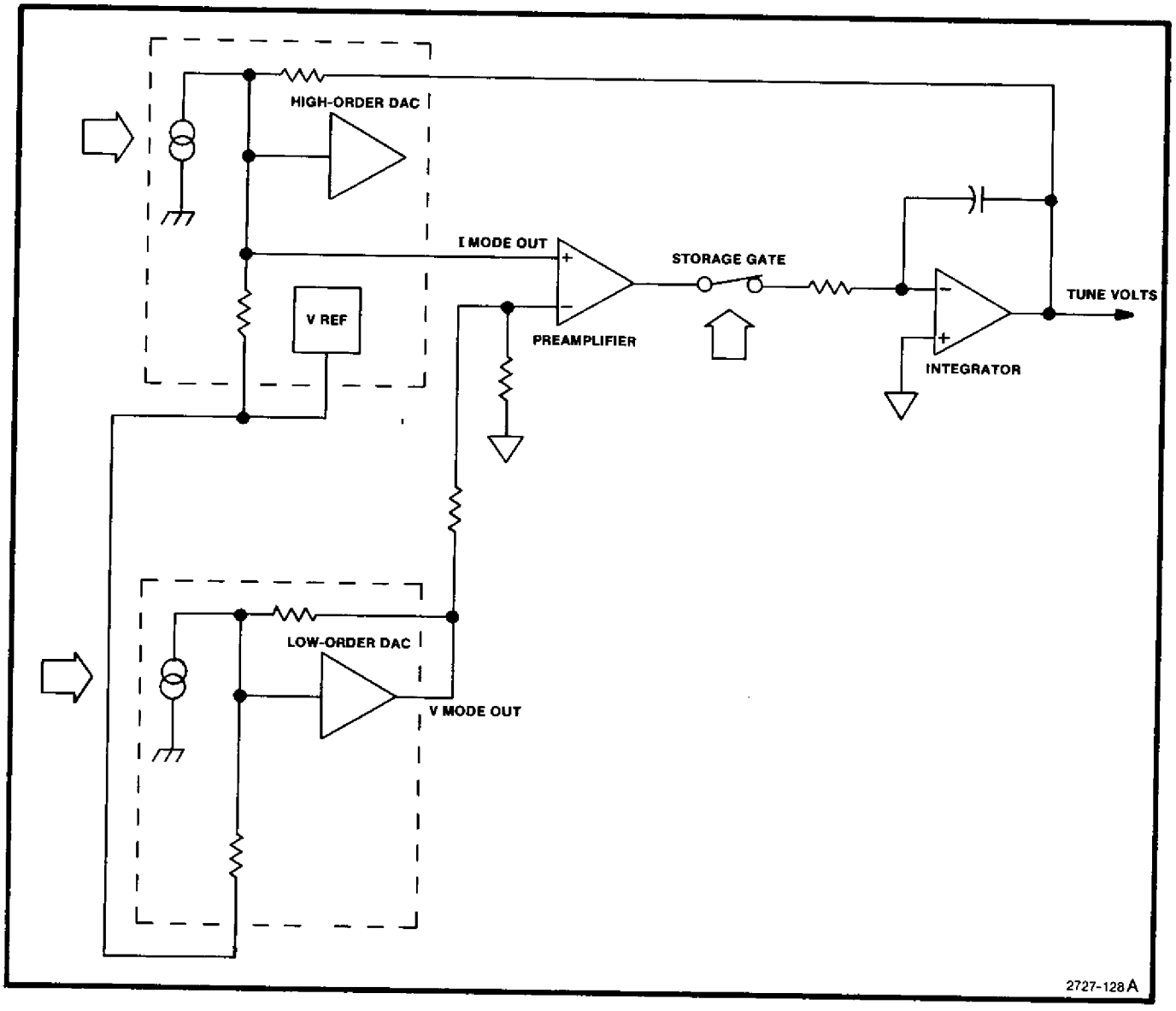


Fig. 5-25. Basic tune voltage converter.

Table 5-14
DAC TUNING CODES

Tuning Point	Data	Address	Results
Positive full-range	00	70	Enables all latches, track mode
	00	71	Loads zeros into all positions of both DAC's
Mid-range	00	70	Enables all latches, track mode
	00	71	Loads zeros into all positions of both DAC's
	33	70	Enables high byte latch, track mode
	80	71	Loads 80 into DAC's. Midrange value
Negative-full-range	00	70	Enables all latches, track mode
	FF	71	Loads FF into all positions of both DAC's

The output of the low-order DAC (U1024) is fed through input resistor R1048 to the inverting input of preamplifier U1044. The current output of the high-order DAC U1030, is fed directly into the non-inverting input of the preamplifier. Feedback resistor R1044 establishes the gain of the stage at about 10,000 (ratio of R1044 to R1046). The combination of CR1046, CR1045, and R1047 in the feedback circuit, prevents the output from swinging to extreme voltages with large input signals. Thus, whenever the output exceeds about one volt in either direction, one of the diodes conducts and connects R1047 and R1045 across the feedback path to reduce the gain of the stage to about unity. The output signal from the preamplifier is connected to the source of storage gate FET Q2046. The gate of this device is controlled by transistor Q2044. Normally the circuit is tracking, so line Q8 (B7) from U2022 is low and Q2044 is conducting. Diode CR2035 is cut off since the voltage drop across R2043 holds the gate of Q2046 at about −0.4 V. (The 0.4 V back bias on the source-gate junction reduces memory slewing while switching modes.) Transistor Q2044 holds the diode back-biased as long as the transistor continues to conduct. This permits Q2046 to pass the signal from the preamplifier output to the integrator input.

Integrator U2046 tracks the preamplifier output during track mode and serves as the inverting amplifier for the feedback system shown in Fig. 5-25. Under normal circumstances the incoming signal is routed through R2046. To improve the amplifier's slewing rate, CR2044 and CR2045 conduct to connect R2047 in parallel with R2046 when signals in excess of one volt are applied. This speeds up the response of the circuit when large scale tuning changes are required.

When the hold mode is selected, line Q8 (B7) of U2022 moves high, Q2044 cuts off and CR2044 pulls the gate of Q2046 low enough to cut off the FET. This disconnects the preamplifier from the integrator which then maintains the charge on C2046 during the approximation routine. COARSE TUNE RANGE adjustment R1032 is connected across pins 16 and 18 of U1030. It compensates for the different resistance values inside the DAC. This variation is more serious in the higher-order DAC owing to its greater effect on the output.

Write-Back Circuits

These circuits consist of amplifier U2044 and U3045, plus enabling transistors Q1039 and Q2043. Since both are identical, only the coarse circuit is described.

Following the command to shift to the hold mode, the microcomputer will interrogate the circuit to see if the DAC output and the stored voltage match. It does this by pulling ADDRESS 80 high. This causes Q1039 to conduct, which in turn furnishes U2044 with operating current. The output of U1044 is at zero volts when the two input voltages match. If the loop error voltage is high, U2044 will pull down on DATA BUS line 7. This informs the microcomputer whether the bit just set is too large or too small. The output of U2044 is open-collector, so it has no effect on the data line when it is not pulling the line low.

1st LO DRIVER

Refer to the block diagram adjacent to Diagram 35.

The 1st LO Driver performs the following functions: Buffers the TUNE VOLTS signal and applies it to the dot marker circuit; combines the SPAN VOLTS and TUNE VOLTS signals, and applies the combination to the Oscillator Driver circuits, which drive the 1st Local Oscillator coils; selects and applies the appropriate tune bias voltage to the 1st Mixer; controls the oscillator filter switch in the 1st LO Driver; produces a stable and precise −10 V reference for the 1st LO.

The major circuits and their function are as follows:

1) the digital control section buffers the incoming data from the data bus, decodes the address data, selects the required mixer bias, connects or disconnects the TUNE VOLTS and SPAN VOLTS signals for the summing amplifier, energizes the filter switch for the 1st LO, and controls the drive and filtering of the oscillator driver stage;

2) the tune volts buffer buffers the COARSE TUNE VOLTS signal from the Center Frequency Control circuits, and reduces the signal amplitude to drive the dot marker circuits;

3) the oscillator filter driver furnishes drive current to the capacitor switching relay in the 1st LO;

4) the input switching circuits combine the SPAN VOLTS and COARSE TUNE VOLTS signals, and applies these signals to the summing amplifier;

5) the summing amplifier furnishes the drive signal to the oscillator driver. The summing amplifier sums the SPAN VOLTS ramp signal from the span attenuator with the coarse tune voltage from the Center Frequency Control circuit. In less than maximum span, a sweep voltage of ±10 V sweeps the oscillator at a rate of 333 MHz/division. As the TUNE VOLTS signal varies from −10 to +10 V, the oscillator's center frequency is moved over its full range of 2016 to 3943 MHz, plus about 50 MHz overtune at each end;

6) the oscillator driver furnishes swept current drive to the 1st LO coil;

7) the reference supply, which produces a precise −10 V reference for the 1st LO Driver;

8) the mixer bias driver produces the required bias voltages for the 1st Mixer in the IF stages.

Digital Control

The digital control circuit sets the oscillator span volts, the 1st Mixer bias and programmable bias for the 496P. Decoder U4034 output Y1 (pin 14) goes low when input address is 72 and output Y7 goes low for address 7E. When either of these outputs go high, data is clocked or latched into U4017, U4024, and U4022. Data for U4017 consists of control codes for the oscillator drive circuits and switch U1016 which selects 1st Mixer bias for the 3.0 to 21 GHz bands, and the bias set by the front panel PEAKING control. The codes are described where each applies to the description and in Table 5-15. Data for DAC U3022 is converted to an analog signal which provides the Programmable Bias for the 496P. The resistance between output terminals 16, 2, and 15 of resistor U3022 is the input resistance for operational amplifier U2018. Resistor R2022 is the feedback resistance.

Tune Volts Buffer. The tune volts buffer consists of amplifier U1025B and surrounding components. The COARSE TUNE VOLTS signal from the Center Frequency Control circuits is reduced to approximately 25% of its amplitude by divider R1028/R1027. The reduced voltage is applied to U1025B, which is configured as a voltage follower with a gain of +1. The output is then fed to the Dot marker stage in the Crt Readout circuits.

Input Switching. This stage consists of FET Q2033, comparators U3014A and U3014C, and FET Q2026. When MAX SPAN is selected, line Q8 of U4017 goes low, causing U3014C to switch. This in turn causes Q2026 to conduct and place R2030 in parallel with R2031, increasing the stage gain of U2032. Also, the same low state is applied to the input of U3014A, which switches and cuts off Q2033. This action disconnects the TUNE VOLTS signal from the amplifier; the TUNE VOLTS is then used only to position a marker on the display. With only the span voltage connected, however, the oscillator is still able to sweep over its full frequency range. The center frequency is equal to the center of the range, which is 2979.5 MHz.

If the main coil is not to be swept, line Q7 of U4017 goes low, which cuts off Q3028 and de-energizes K2028. This removes the SPAN VOLTS signal from the amplifier. Diode CR3031 protects Q3028 from the inductive feedback surges that occur at turn-off.

Oscillator Filter Driver. This circuit consists of Q2029 and related components. When relay K2028 is de-energized, as just described, Q2029 conducts. This stage drives a capacitor-switching relay on the 1st LO Interface board. The capacitors are switched across the main coil whenever it is not being swept, to filter noise from the tuning current. Capacitor C2025 maintains current through the relay after power is turned off, until the coil current has decayed.

Table 5-15
U4017 (U3027) OUTPUT LINES

	Low	High
Q1	Not Used	Normal mode
Q2	Not Used	Normal mode
Q3	Not Used	Normal mode
Q4	Not Used	Normal mode
Q5	Output Filter disconnected	Output filter connected
Q6	Driver Input connected	Driver Input disconnected
Q7	SPAN VOLTS disconnected	SPAN VOLTS connected
Q8	Maximum span; TUNE VOLTS disconnected	Normal span; TUNE VOLTS connected

Summing Amplifier. This operational amplifier circuit consists of amplifier U2032, complementary pair Q2035/Q2039, and related components. The feedback resistance for this circuit is R1038. The input resistance is R2027 for the COARSE TUNE VOLTS input and R2031 for the SPAN VOLTS input. (Resistor R2030 is switched across R2031, as mentioned earlier, to increase stage gain for maximum span operation.) The output of the summing amplifier, which swings from −10 V to +10 V, is applied to the Video Processor. It is also fed through R1031, the 1st LO SENSE adjustment, summed with the offset voltage from R1032 (1st LO OFFSET), then applied to the source of Q2040. Adjustments R1031 and R1032 match the oscillator driver stage to the oscillator characteristics. Resistor R1032 adds offset to the output of U2032 to place the oscillator at center operating frequency when the output of U2032 is at zero volts. Resistor R1031 matches the sensitivity of the oscillator to the output amplitude from Q2039/Q2035.

FET Q2040 is used to disconnect the signal from the driver stage. In order to degauss the oscillator coil, (thus establishing a known magnetic history), the microcomputer causes line Q6 of U4017 to go high for about 200 ms. The output of comparator U3014D goes low, cutting off Q2040. This removes all drive from the oscillator coil until the Q6 line returns low.

Oscillator Driver. The oscillator driver stage consists of operational amplifier U2043/Q3047 and surrounding components. It converts its voltage input into the current drive required by the oscillator main tuning coil.

Preamplifier stage Q2045, which receives the signal from the operational amplifier U2032, Q2039/Q2035 through Q2040, is a low-noise matched dual transistor. Transistor Q2045 is part of the input circuit of a feedback amplifier containing U2043, Q3047, and driver transistor Q352. The feedback path through R3040 and R2042 sets the voltage across a four-terminal resistor R1040. This voltage in turn sets the current of the resistor which is also emitter current for driver transistor Q352. The oscillator coil current 1st LO Sense adjustment R1031 sets the voltage gain of the amplifier which changes the current drive to the oscillator coil.

Capacitor C3038 filters noise on the tune volts and voltage reference inputs. Because of its effect on tuning speed, the capacitor is in the circuit only in the phaselocked mode with phaselock switched off, or when the phaselock option is not included in the instrument. Normally Q5 of U4017 is low, which through U3014B, causes Q3042 to cut off.

Reference Supply. Operational amplifier U2052 and surrounding circuitry form the −10 V reference supply. One side of preamplifier Q2052, biased by R1055 and VR1051, sets a reference voltage at the inverting input of U2052. The output voltage is set by R1034, the −10 V adjustment. IC U2052 senses changes in load that are amplified by Q2052, and changes the current through regulator transistor Q2051. The diode network across the base-emitter junction, limits the collector current to about 23 mA, protecting the transistor from damage.

Mixer Bias Driver. The mixer bias driver circuit, which consists of quad FET switch U1016, amplifier U1025A, and buffer Q2025/Q1028, plus associated circuitry, furnishes the required bias current (up to 20 mA) to the 1st Mixer circuit. The bias voltage varies from +1 V to −1 V for the internal mixer, and from +1 V to −2.25 V for an external mixer.

Regulator U1013/U1018, provides regulated +12 V and −12 V across the three bias adjustment potentiometers, R1013, R1026, and R1022. The voltage at the center arm of one of thse potentiometers, or the output of U2018, (which represents the front panel PEAKING control setting or programmable bias) is selected by quad FET switch U1016 and applied to the input of U1025A. Quad FET U1016 is controlled by Q1 through Q4 lines from data latch Q4017. A low at any one of these outputs causes the associated FET to conduct and connect that line to the input of U1025A. IC U1025A drives a pair of transistors, Q1028/Q2025, connected as a complementary pair to provide the 1st Mixer bias voltage.

Programmable Bias. When the microcomputer sends address 7E to decoder U4034, pin 7 (output Y7) goes low. At the end of data output cycle, data is clocked into either U4024 or U4022, depending on which latch is enabled by DB6 or DB7. This data is then converted to an analog current by U3022, which is the current source for operational amplifier U2018. The output of U2018 is a bias voltage that is fed to the RF circuitry to the 1st Mixer.

Oscillator Collector Supply. This circuit comprises amplifier U4055, buffer Q3049, and surrounding circuitry. IC U4055 holds Q3049 in saturation, so the collector of the transistor remains at a fraction of a volt below +15 V. This voltage is applied to the 1st LO circuits.

DIGITAL CONTROL 8

The Digital Control section of the 496/496P provides the operator/496 and digital controller/496 interfaces. It translates changes in front-panel controls and instructions received via the accessories interface or GPIB interface (496P only) into codes that control the instrument via the instrument bus.

The Digital Control section simplifies operating and programming the 496 and 496P. Unless overridden by the operator, the microcomputer automatically selects secondary parameters. Some examples are: when the operator selects span, the microcomputer chooses an appropriate bandwidth; when the operator changes the reference level, the microcomputer trades off input attenuation and IF gain.

In the 496P, the microcomputer can handle some operations automatically. For example: the microcomputer can search digital storage for signals and change FREQUENCY and REFERENCE LEVEL to zoom in on signals it finds.

The digital control operating program is defined by the meaning of the controls and commands given in the operating and programming manuals and is not further defined here. The following description focuses on the hardware.

The following circuits make up the digital control section:

1) microcomputer, including processor and memory boards;

2) addressable registers on the instrument bus;

3) front panel Accessories interface;

4) GPIB interface (496P only).

The microcomputer is based on a 6800 microprocessor; its operating program is stored in ROM. The microprocessor accesses the ROM-RAM, and I/O interface via the microcomputer bus. The bus operates with 16-bit addresses, 8-bit bytes, and several control lines for data transfers.

The front panel and the addressable registers that control some other 496/496P assemblies reside on the instrument bus. This bus requires only 8-bit addresses and transfers 8-bit bytes. The bytes may be codes to set or indicate the status of an assembly or, in the case of digital storage and crt readout, data values that correspond to the display. When one of the assemblies requires the attention of the microcomputer, it asserts a service request line. The microcomputer responds by finding the source of the service request and executing the appropriate service routine.

Processor communication over the instrument bus can be stopped by an external controller on the accessories bus; the external controller can then override normal operation.

The GPIB interface (496P only) resides on the microcomputer bus. It contains added ROM for the operating program used for GPIB I/O and added RAM. The interface is based on a general-purpose interface adapter (GPIA) IC that reduces processor overhead required for GPIB operation.

PROCESSOR 36

The Processor board contains the processor clock, microprocessor, address decoders, microcomputer bus buffers, and instrument bus interface. These blocks are shown on the Processor board block diagram adjacent to Diagram 36.

Processor Clock

The two-phase processor clock is derived by U4035 from its internal oscillator. A simple logic diagram of this IC is shown in Fig. 5-26.

The two clock signals, $\phi 1$ and $\phi 2$, are complementary and non-overlapping. They are divided by 4 from the oscillator frequency for a processor clock frequency of about 850 kHz. The $\phi 2$ CLK is buffered for use by the rest of the microcomputer system and is in phase with the $\phi 2$ clock signal used by the 6800. The undivided oscillator frequency signal is distributed as CRT CLK for crt readout timing.

$\overline{RST}$ stays low while C3042 charges following power-up and holds the microcomputer in a reset state until the power supply is fully on. This signal does not disable the clock, so the 6800 can initialize itself during this time.

6800 Microprocessor

The 6800 microprocessor (U3027) is an 8-bit processor with an 8-bit bidirectional data bus and 16-bit address bus. The 6800 block diagram in Fig. 5-27 shows the internal organization of the IC. The function of each block is as follows.

Accumulators. Eight-bit accumulators A and B hold operands for and results of ALU operations.

Condition Code Register. Bits in the condition code register indicate results of ALU operations and whether interrupts are masked; see Table 5-16.

Program Counter. This 16-bit register holds the address of the instruction being executed.

Table 5-16
CONDITION CODES

Bit	Function
0	Carry from accumulator bit 7
1	Overflow
2	Zero result
3	Negative result
4	Interrupt mask
5	Carry from accumulator bit 3 (half-carry)
6	Unused (always 1)
7	Unused (always 1)

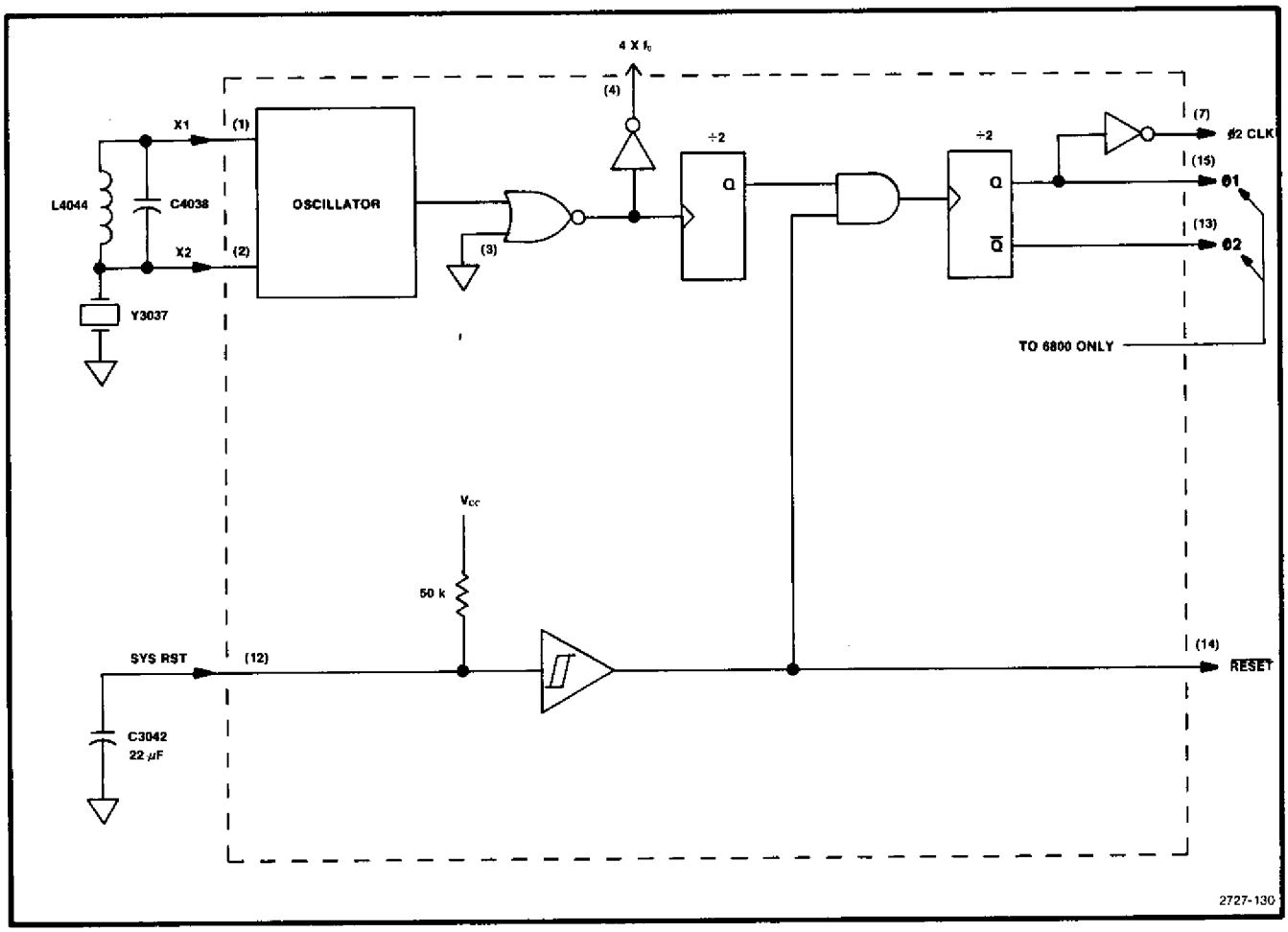


Fig. 5-26. Simple logic diagram of processor clock.

Stack Pointer. This 16-bit register acts as the pointer for a previously defined stack in memory. The pointer is the address of the next available location on a LIFO (last-in, first-out) basis. The stack is used to store the contents of MPU registers when an interrupt occurs or the 6800 executes a subroutine. The stack pointer is decremented when data is pushed onto the stack and incremented when data is popped off the stack.

Index Register. This 16-bit register facilitates indexed-mode addressing. Instructions can load, increment, decrement, compare, etc., so it can also be used as a general purpose register.

Instruction Register and Decoder/Timing Control. During the instruction fetch (the first one or more machine cycles), successive bytes of an instruction are loaded from the program memory into the instruction register. The contents of this register are then passed to the decoder and timing logic. This block decodes the byte(s) and generates the machine states and control signals that affect execution of the instruction. The number of machine cycles this takes depends on the instruction and addressing mode.

Data and Address Buffers. These tri-state buffers isolate the 6800 internal buses from the external microcomputer bus.

Clocks. The two-phase TTL-level clock signals synchronize 6800 operation. A machine cycle is defined as the interval between two successive positive-going transitions of the $\phi 1$ clock signal.

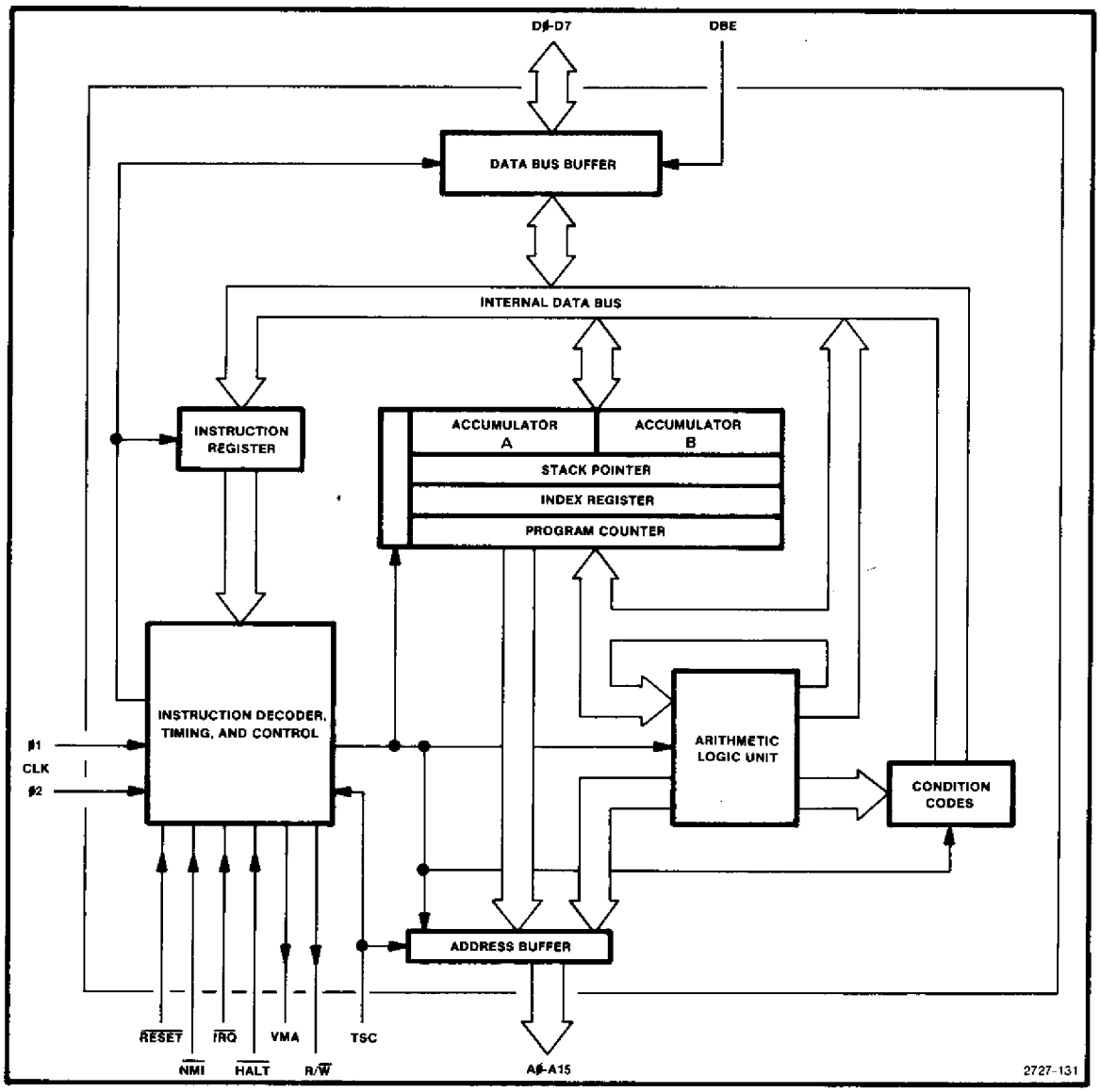


Fig. 5-27. Block diagram of 6800 microprocessor.

HALT. This input is unused (tied high through a pull-up).

Three-State Control (TSC). This input is tied low so the address buffer and read/write line are always enabled.

Read/Write (R/$\overline{W}$). This output sets the direcion of data flow—high when the 6800 is reading data and low when the 6800 is writing data. It is also high between read and write operations.

Valid Memory Address (VMA). This output is asserted high when the 6800 places a valid address on the microcomputer bus. It enables the memory address decoders.

Data Bus Enable (DBE). This input is paired with the $\phi 2$ clock input so the data buffer is enabled during $\phi 2$ of the machine cycle.

Figure 5-28 shows a read and a write cycle on the microcomputer bus. This illustrates how the control signals are used to control data transfers on the bus.

Interrupt Request ($\overline{IRQ}$). This input is buffered from SER REQ on the instrument bus. When one of the assemblies asserts this line, it is seeking the microcomputer's attention. The 6800 completes its current instruction before reacting. It then checks the interrupt mask bit in the condition code register. This bit is set when the microcomputer is executing most service routines in response to front-panel changes or GPIB messages. If the bit is set, the request is ignored until the microcomputer completes the routine and resets the bit. If the bit is clear, the microcomputer sets the bit and then starts an interrupt sequence.

1. Push the contents of the program counter, index register, accumulators, and condition code register onto the stack, decrementing the stack pointer each time a byte is stored.

2. Set the interrupt mask bit and load the address stored at FFF8, the interrupt vector.

NOTE

6800 addresses are given as hexadecimal numbers.

3. Execute the interrupt service routine that begins at the address read in step 2. This routine begins by interrogating the assemblies to find one that pulled down on the interrupt request line. It then proceeds to service that assembly.

4. At the end of the interrupt routine, return to the idle routine that occupies the microcomputer between tasks by retrieving the previous register contents from the stack.

Non-Maskable Interrupt ($\overline{NMI}$). Tied high through a pull-up, this interrupt is not used by the digital control system.

RESET. This input initializes the 6800 following power-up. The clock generator (U4035) holds this line low for about one second for 6800 start-up. After the input goes high, the 6800 begins its initialization routine at the address stored at FFFE and FFFF. This routine masks interrupts until it is ready to handle them. It then continues executing the operating program according to the flow chart in Fig. 5-29.

6800 Address and Data Bus

The 6800 address outputs are buffered by U2035 and U3036; they are always enabled. The data I/O buffer, U1013, is normally enabled. If disabled by P1020, it isolates the 6800 from the microcomputer bus data lines for diagnostics. See further information about diagnostics under Address Decoders. The direction of data flow is set by the R/$\overline{W}$ line. Address Decoders U2044 and U1037B drive address select lines and status lights for the microcomputer system. The address select lines are shown in Table 5-17.

Table 5-17
ADDRESS SELECT LINES

Line	Selects	Address
SYS RAM	RAM on Memory board	0000—07FF
GPIB RAM	RAM on GPIB board	0800—OFFF
U1037B-12	Instrument bus	1000—11FF
GPIB	GPIA on GPIB board	1200—13FF
OPSW	Switch register on Memory board	1400—15FF

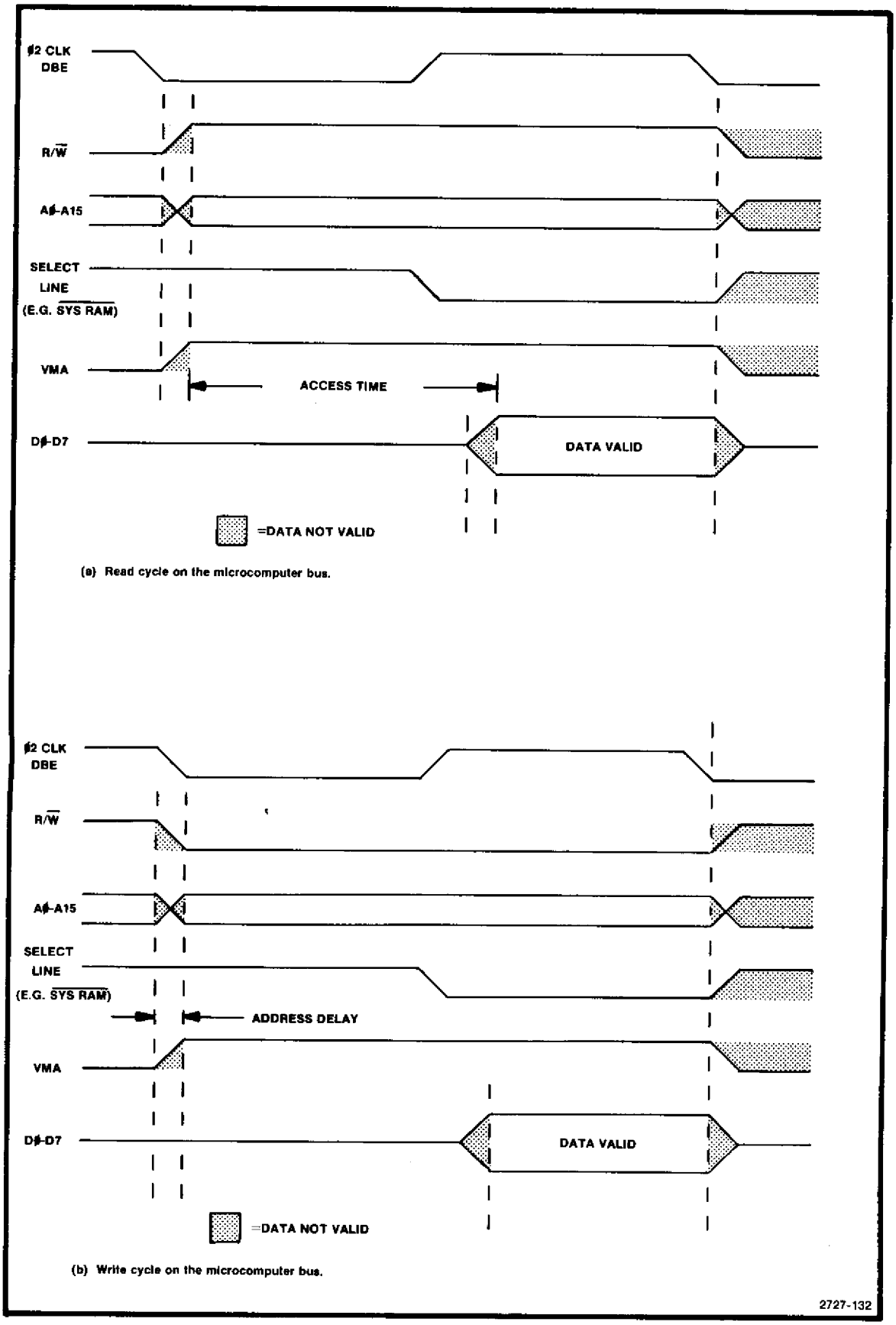


Fig. 5-28. Read and write cycle timing on the microcomputer bus.

Other addresses are decoded on the Processor board for diagnostics, turning on LEDs on some outputs of U2044. Diagnostic routines can cause the 6800 to access an address that turns on an LED as a test indicator. For further information, see the self-test instructions in the Maintenance section.

ROM addresses on the Memory board and the GPIB board are decoded there and do not rely on address select lines from the Processor board.

U2044 is enabled by VMA and zeros on A15 and A14 (3FFF and below). It decodes the 3-bit binary input of A11, A12, and A13 to assert one of eight outputs (Y6 and Y7 are unused).

U1037B is enabled when U2044 decodes an address in the range 1000—17FF and decodes A9 and A10 to assert one of four outputs.

Address Map

Microcomputer memory is mapped in Table 5-18 (addresses in hexadecimal).

Instrument Bus Interface

The microcomputer communicates with the rest of the instrument over the instrument bus (with the notable exception of the GPIB interface). Peripheral interface adapter (PIA) U3022 is programmed to send addresses and send or receive data on the instrument bus. It also handles control lines for writing to and reading from registers on the instrument bus. It does not, however, handle service requests; the SER REQ line goes directly to the 6800.

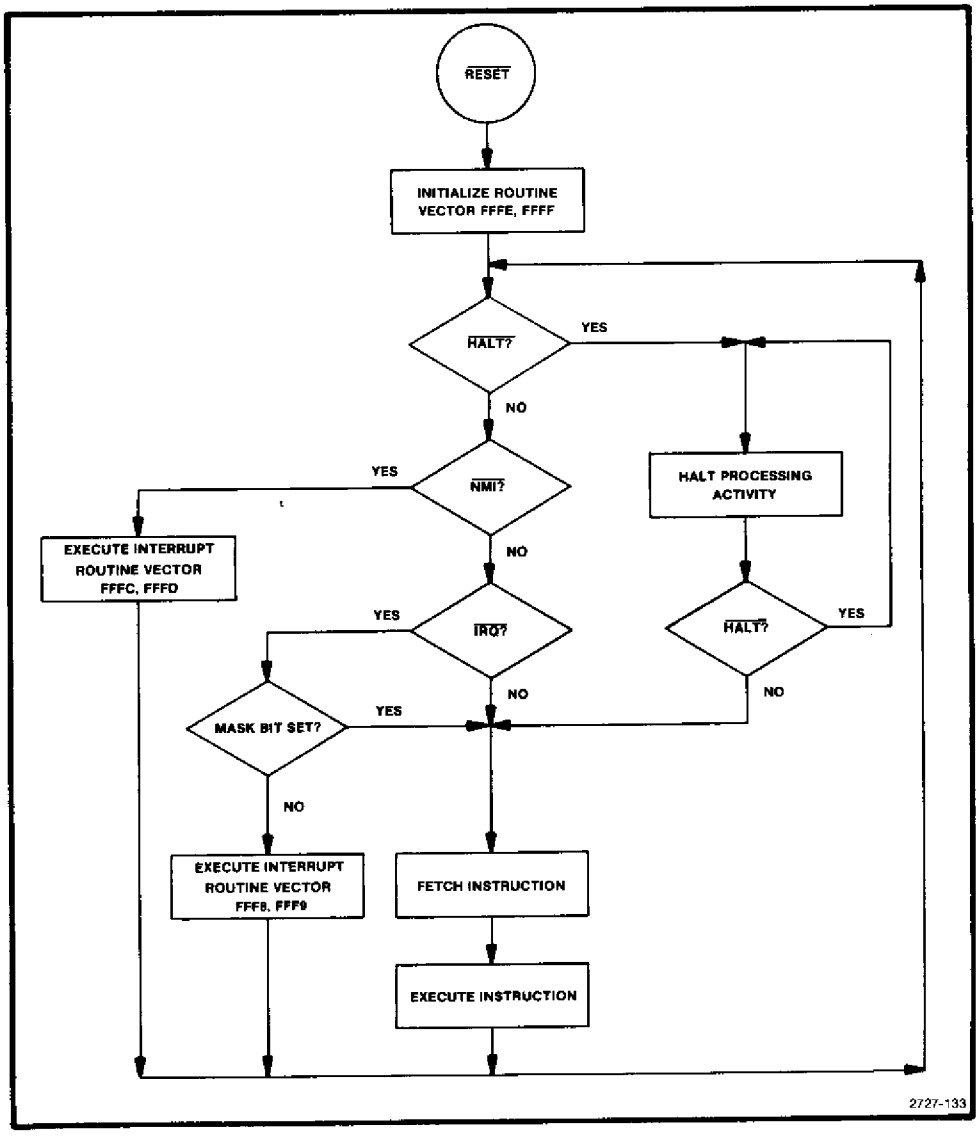


Fig. 5-29. Flow chart of the 6800 main decision paths.

The PIA is reset at power-up and the 6800 then programs it for each of its tasks. How the 6821 PIA is configured in the 496/496P microcomputer system is shown in Fig. 5-30.

Table 5-18
496/496P MICROCOMPUTER ADDRESS SPACE

0000	System RAM
0800	GPIB RAM
1000	Instrument Bus Interface
1200	GPIA on GPIB board
I/O 1400	Options switch on Memory board
1600	Unused
1800	ROM on Memory board (Four 2K EPROM's)
3800	Unused
4000	ROM on GPIB board (B 2K EPROM's or 2 8K ROM's)
8000	ROM on Memory board (Four 8K sockets with 2K EPROM's or 8K ROM's)
FFFF	

Chip Select. Chip select lines CS0 and CS1 are always enabled; the 6800 selects the PIA by addressing 1000, which asserts CS2. Data transfers are then performed under control of the read/write, register select, and enable signals.

Register Select. Four registers and two peripheral interfaces are addressable. The 6800 selects one by a code on RS0 and RS1 (the two LSBs of the PIA address) and by setting or clearing bit 2 in the appropriate control register as shown in Table 5-19.

Read/Write. The 6800 sets the direction of data through the data buffer with R/$\overline{W}$. When the 6800 sets this line low, it enables the input register. A high enables input to the 6800 from the PIA internal output bus.

Enable. The $\phi 2$ clock high pulse transfers data to the input register and enables one of the peripheral interfaces (if addressed) on a write cycle.

Data Direction Registers. These registers allow the MPU to control the direction of data on each line connected to the peripheral interfaces. A zero (0) configures the corresponding data line as an input; a one (1) configures it as an output.

Control Registers. The 6800 uses bit 2 of these registers for addressing as explained above. Bits 3, 4, and 5 form a code to control CA2 and CB2 as outputs on the instrument bus. CA2 is configured as POLL to enable a parallel poll on the instrument bus. CB2 is configured as DATA VALID to strobe data into an addressed register during a 6800 write to the instrument bus. It is also asserted on 6800 reads to enable the data buffer. The RC delay following inverter U1013B provides data settling time on the bus before DATA VALID goes high. U1013B's open-collector output pulls down faster than R1024 pulls up, so DATA VALID's low-high transition is delayed compared to its high-low transition.

Table 5-19
PIA REGISTER AND INTERFACE SELECT CODES

		Control Register Bit		
RS1	RS0	CRA-2	CRB-2	Register or Interface
0	0	1	X	Peripheral Interface A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Interface B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

Peripheral Interface A. PA0—PA7 are configured as outputs to drive the instrument bus address lines. The 6800 writes to this interface to address a register on the instrument bus.

Both the A and B interface buffers are disabled if an external controller pulls the INTL CONT line low. They are also disabled if P1020 is disconnected for diagnostic purposes. Either releases the low on the output of U1037A. The interrupt line buffer, U3043A, is also disabled. These buffers for the address, data, and interrupt lines then decouple the 6800 from the instrument bus.

Peripheral Interface B. PB0—PB7 are configured either as inputs or outputs to transfer data from or to the instrument bus. The 6800 writes data to this interface to send it to a register on the instrument bus and reads data from this interface when it interrogates a register on the instrument bus.

Pull-ups on the data lines result in all ones if a read cycle inputs a byte when no instrument bus register is enabled.

The MSB of the address determines the direction of data through U3016, the data lines buffer. Instrument bus addresses 80 and above set U3016 to buffer data from the instrument bus to the PIA (6800 read); address 7F and below set U3016 to buffer data in the opposite direction (6800 write).

The RC delay in the enable signal for buffer U3016 slows the low-high transition at the input of the Schmitt trigger, but has little effect on the high-low transition. This holds the instrument bus data lines stable while DATA VALID is going false, but has little effect when the data lines are to be driven at the beginning of a write cycle.

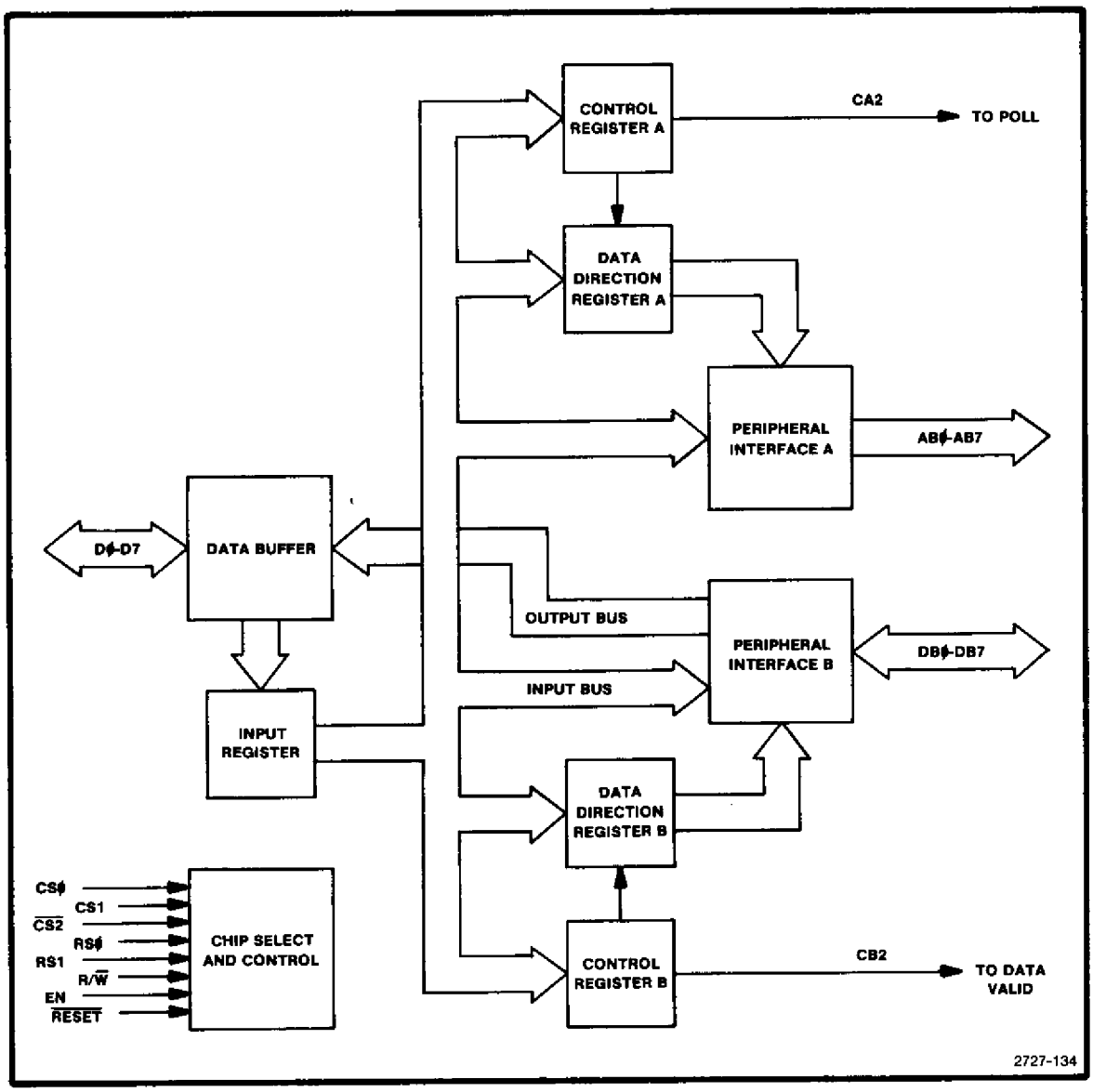


Fig. 5-30. 6821 PIA registers and control lines.

Instrument Bus Registers

Instrument bus address lines are split into a right bus and a left bus for economy in address decoding. On the right bus, a board with an addressable register need only decode AB0 through AB3 and AB7; on the left bus, a board need only decode AB4 through AB7. In both cases, AB7 indicates read (high) or write (low), as it does for the instrument bus interface data buffer noted above. The microcomputer communicates with the following registers to control assemblies as shown in Table 5-20.

Instrument Bus Data Transfers

Data transfers on the instrument bus require two steps: the 6800 writes the address to peripheral interface A and then reads or writes the data through peripheral interface B.

When the 6800 writes to the instrument bus, it configures the PIA to pulse DATA VALID (the CB2 output). The PIA does this automatically after data is written to peripheral interface B as shown in Fig. 5-31.

Table 5-20
INSTRUMENT BUS REGISTER ADDRESSES

Register	Circuit Board	Write	Read
---------- Right Bus ----------			
Tune control data	Center Frequency Control	70	F0
Data steering	Center Frequency Control	71	
1st LO driver control	1st LO Driver	72	
1st LO phaselock control	1st LO Phaselock Control	73	F3
Front panel LEDs	Front Panel	74	
Front panel encoders	Front Panel		F4
Span magnitude data	Span Attenuator	75	
Span magnitude and decade attenuator data	Span Attenuator	76	
Post VR gain	Log & Video Amplifier	78	
Video display mode/gain	Log & Video Amplifier	79	
Digital storage data	Vertical Digital Storage	7A	FA
Digital storage control	Vertical Digital Storage	7B	
Video level/filter/blank	Video Processor	7C	
---------- Left Bus ----------			
Sweep rate and mode	Sweep	0F	
Holdoff, interrupt, trigger	Sweep	1F	
Crt readout data	Crt Readout	2F	
10 MHz IF gain and bw	VR Motherboard #2	3F	
Z-axis & RF deck control	Z-Axis/RF Interface	4F	
Crt readout control	Crt Readout	5F	

When the 6800 reads from the instrument bus, it does not configure the PIA to pulse DATA VALID as it does for a write cycle. Rather the 6800 writes to control register B to set CB2 low. CB2 low asserts DATA VALID, after the RC delay allowing for the data to be accessed, and the 6800 then reads the data through peripheral interface B. After reading the data, the 6800 writes again to control register B to unassert DATA VALID.

Instrument Bus Poll

When the 6800 recognizes an interrupt request ($\overline{SER\ REQ}$ asserted), it enters a service routine. As part of this routine, it performs a parallel poll to find who is requesting service. A parallel poll sequence is shown in Fig. 5-32.

The 6800 begins by writing an invalid address on the instrument bus, FF; all address decoders on the bus ignore this address. Next, the 6800 writes to control register A to set CA2 high, asserting POLL. All boards that respond to a poll recognize this line and contain logic that either responds or prepares to respond when the 6800 causes DATA VALID to be asserted. Each interrupt is assigned a data line as shown in Table 5-21. The board originating that interrupt pulls low on the corrsponding line.

After the 6800 reads the status byte, it clears POLL and writes address 7F on the instrument bus. The transition on POLL disables the poll response circuitry of boards on the instrument bus. Since 7F is also an invalid address, it also unaddresses all instrument bus registers. The following positive transition on POLL prepares all parallel poll boards, so when the 6800 writes back the parallel poll byte, it clears all interrupts that were read.

Table 5-21
PARALLEL POLL BYTE

7	6	5	4	3	2	1	0
X	X	X	End-of sweep	Center frequency knob	Phase lock	X	Front panel encoder

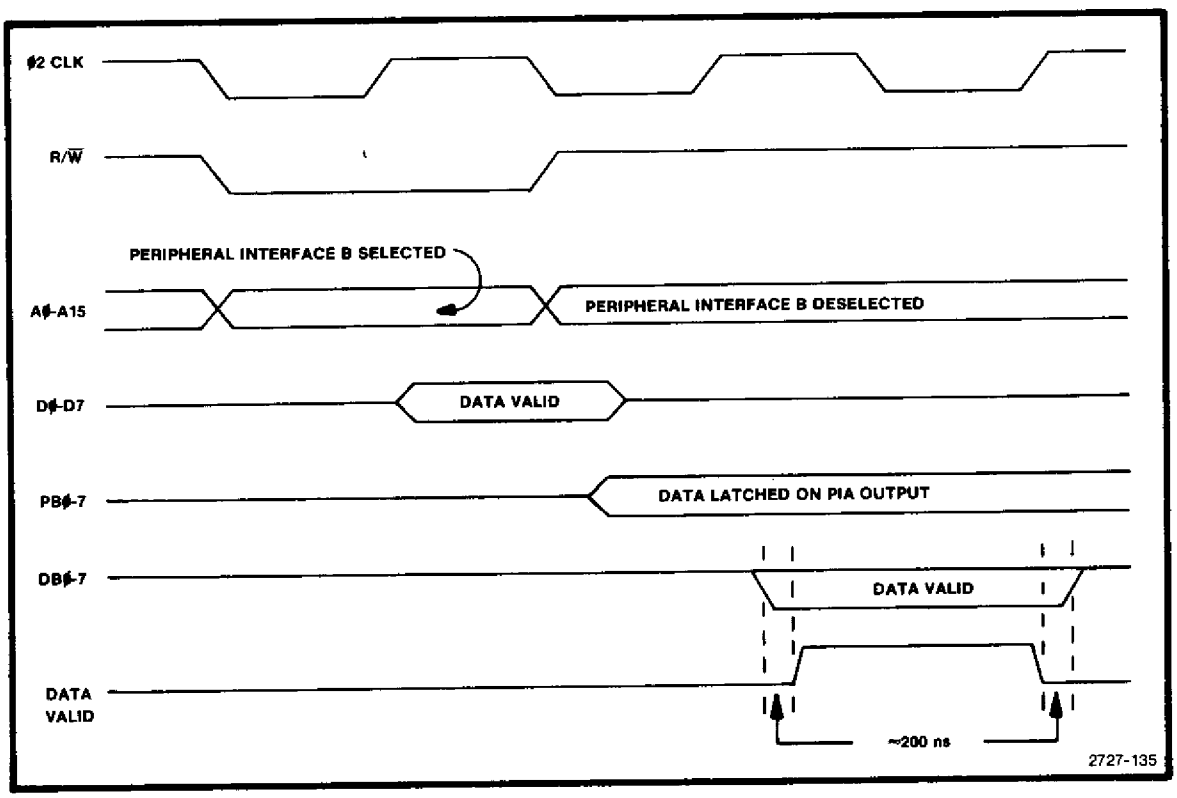


Fig. 5-31. A 6800 write to the instrument bus.

The 6800 reads the interrupt status of the GPIA on the GPIB board separately and combines it with the instrument bus status before servicing the interrupt(s). Interrupts are serviced according to their priority.

MEMORY BOARD 37

The Memory board holds the ROM operating program for the microcomputer and the RAM used by the program. It also holds a bank of switches that the microcomputer can read to configure itself for options and diagnostics.

ROM Address Decoding

The full microcomputer address bus extends to this board for ROM address decoding. U1036 and U1038 decode banks of addresses and assert one-of-eight ROM chip-enable lines when a bank that corresponds to one of the ROMs is addressed. The decoders are enabled by VMA and R/$\overline{W}$ high (a valid address during a read cycle). U1036 also requires A15 to be low to be enabled; if enabled, it decodes addresses in the range 1800 to 3800 from the binary code formed by A11 through A13.

Since U1038 alone responds to the upper-half of address space, it need not decode addresses further than A13 through A15. The four ROMs in this address space, however, are strapped to treat the enable and the upper address bits differently if 8k rather than 2k chips are installed. For 8k, the decoded enable lines drive the chip-enable inputs and the upper address bits (A12 and A11) are decoded by the chip. For 2k, the decoded enable line, rather than A11, drives pin 18, and a logic one, rather than A12, is applied to pin 21; pin 20 is grounded. The decoder responds to $\phi 2$ CLK so the enable lines are clocked for the benefit of 8k ROMs, which recognize a new address only on the negative transition of $\overline{CE}$.

RAM

Data words in RAM are divided between the two 1k X 4 ICs; U2032 holds the upper four bits and U2035 holds the lower four bits. Both are selected by SYS $\overline{RAM}$ and the $\phi 2$ clock, while R/$\overline{W}$ sets the data direction.

Option Switch Register

The microcomputer accesses U1033, a buffer enabled by $\overline{OPSW}$, to read S1033 at power-up. Switch 1 is normally open. Switches 2 through 6 indicate internal hardware configuration. Switches 7 and 8 call self-test routines. For the correct use of switches 2 through 8, refer to the Maintenance section of this Service manual.

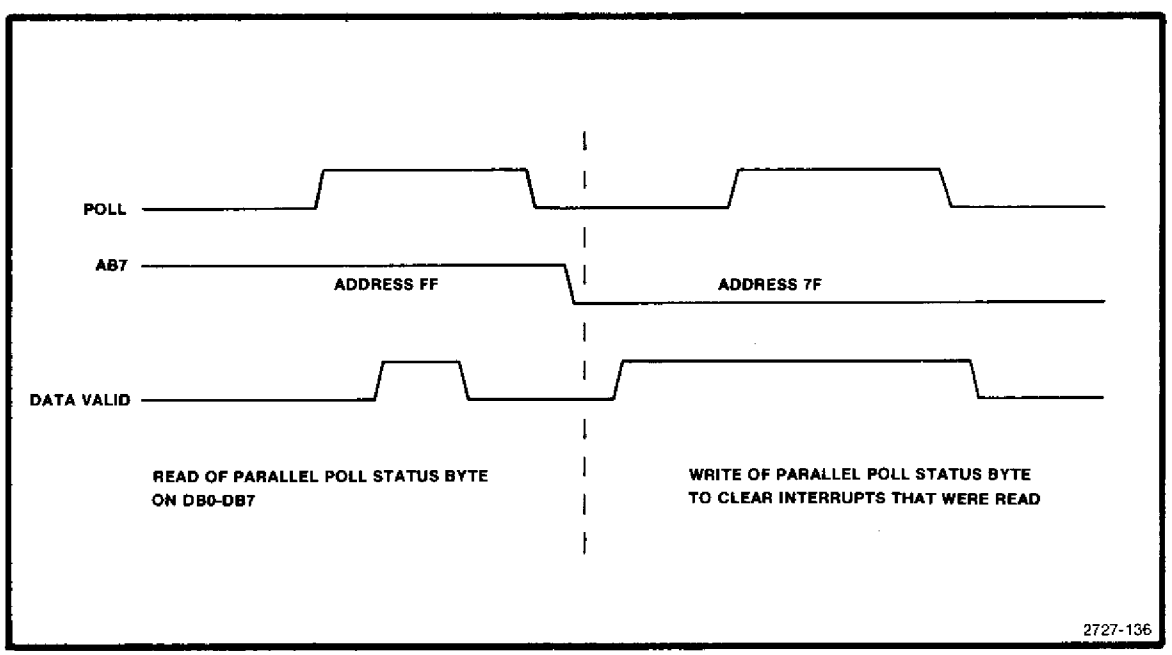


Fig. 5-32. Instrument bus poll sequence.

FRONT PANEL (38)

The Front Panel board translates an operator action of a front-panel control into data for the microcomputer to read and implement. The board, in turn, accepts data from the microcomputer to display via LEDs the current operating modes of the instrument. Some analog control signals are also derived from potentiometers on this board.

Push button switches and some rotary switches are wired in a matrix that is read by a keyboard encoder; this is the main switch encoding block. A power-up circuit prompts the encoder to output the initial value of the rotary switches. The FREQUENCY control drives a separate up/down encoder. Each encoder interrupts the microcomputer when it senses a change and transmits its data through the instrument bus port.

The LED display inputs data through the instrument bus port and strobes it into shift registers that drive the LEDs.

Instrument Bus Port

The instrument bus port comprises an address decoder, an output path for the encoders, and an input path to the bank of LED driver shift registers. The output and input paths appear as registers on the instrument bus.

Address Decoding. The data and enable inputs to U4031 select output Y2 when the microcomputer places address 74 on the instrument bus and output Y6 for address F4. These addresses correspond to the input and output paths through the port:

Hex address	Data path
74	Input to LED display shift registers and power-up circuit.
F4	Output from keyboard and frequency encoders.

Input. DB 0, DB 1, DB 2, and DB 4 provide the inputs to shift registers U2045, U3030, U5045, and U6075. The microcomputer writes to this input port eight times to fill the shift registers, which drive the front-panel LEDs. The MSB of U6075 drives the graticule light circuit.

DB 3 drives the power-up circuit.

Output. DB 0 through DB 6 represent the 7-bit code from the keyboard encoder. The code corresponds to one of the positions shown in Fig. 5-33 under Switch Matrix Codes. The X-Y positions of the switch can be decoded from the 7-bit code as a decimal number in which the first digit is X and the rest of the number is Y. To obtain the number:

1) convert the binary code to decimal number;

2) add 1 to the first digit and 1 to the second digit;

For example:

1) binary 0011101 is converted to decimal 29;

2) 1 is added to the first digit (2), and 1 is added to the second digit (9), for X=3 and Y=10—the FINE button.

DB 7 represents the direction of change in the FREQUENCY control (see FREQUENCY Encoder that follows).

Buffer U1047 is enabled only when the output path is addressed.

Switch Encoding

A keyboard encoder, U3039, scans the switch matrix continuously and compares any switch closures it senses with those sensed during the last scan. Any new closure causes the encoder to request service so the microcomputer can read the code for the switch.

How the encoder scans the matrix is illustrated in Fig. 5-34. By asserting X1 through X8 in turn, the encoder accesses a column of switches. It senses the state of each switch in that column on Y1 through Y10.

Encoder Logic. The logic inside the keyboard encoder that scans the matrix, senses switch closures, handles the bookkeeping for which switches changed, and outputs the code for new closures, as shown in Fig. 5-35.

The keyboard encoder is clocked by a 555 timer, U1011. The clock drives the Y counter, which causes the key sense logic to present the status of each of its inputs, Y1 through Y10, sequentially to the control logic. These inputs represent the state of a column of switches in the switch matrix. The control logic continuously shifts through the shift register to compare the input from the key sense logic to the value last stored for the switch represented by that input. When a scan of the column is finished, the X counter advances so the next column is scanned.

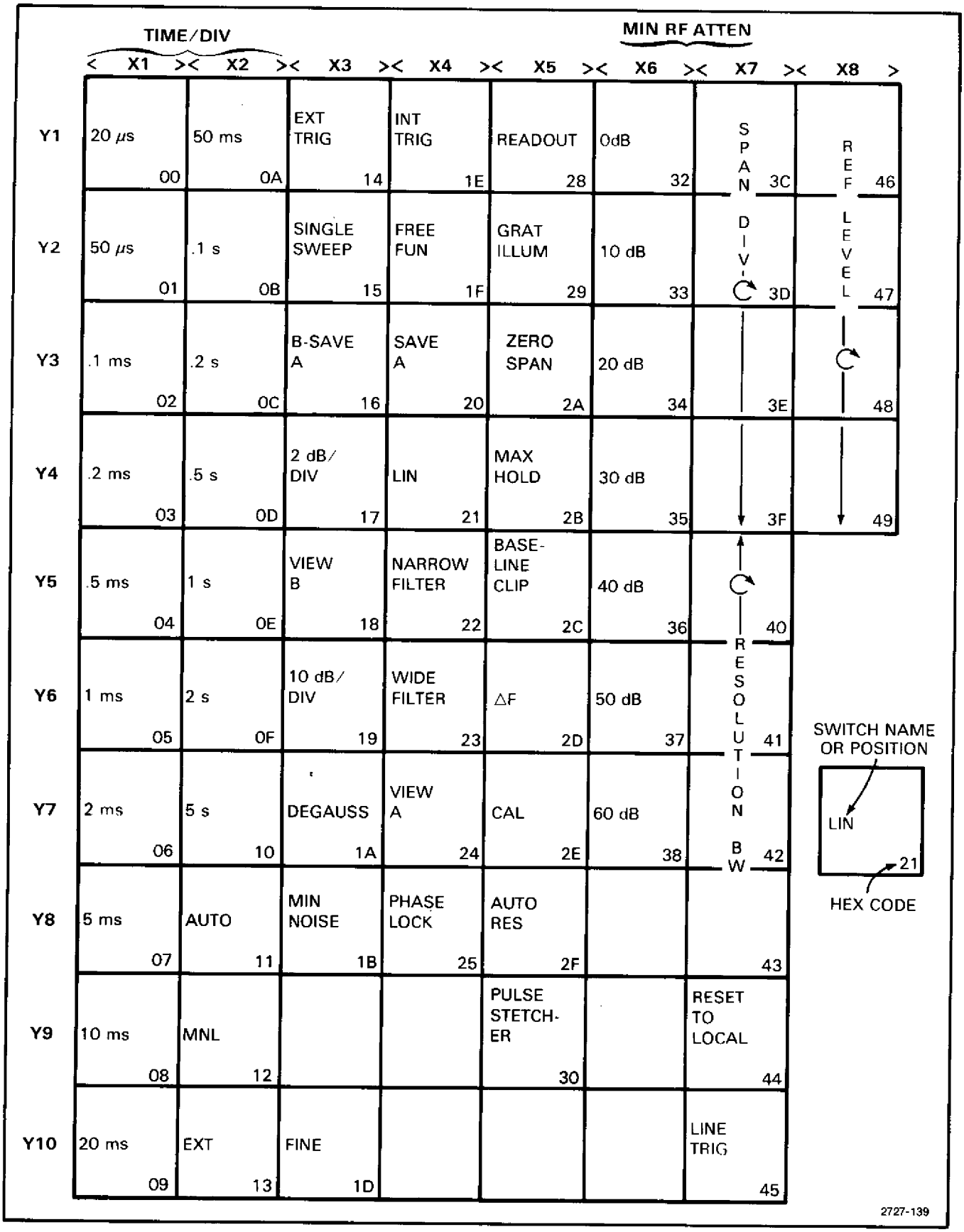


Fig. 5-33. Switch matrix codes.

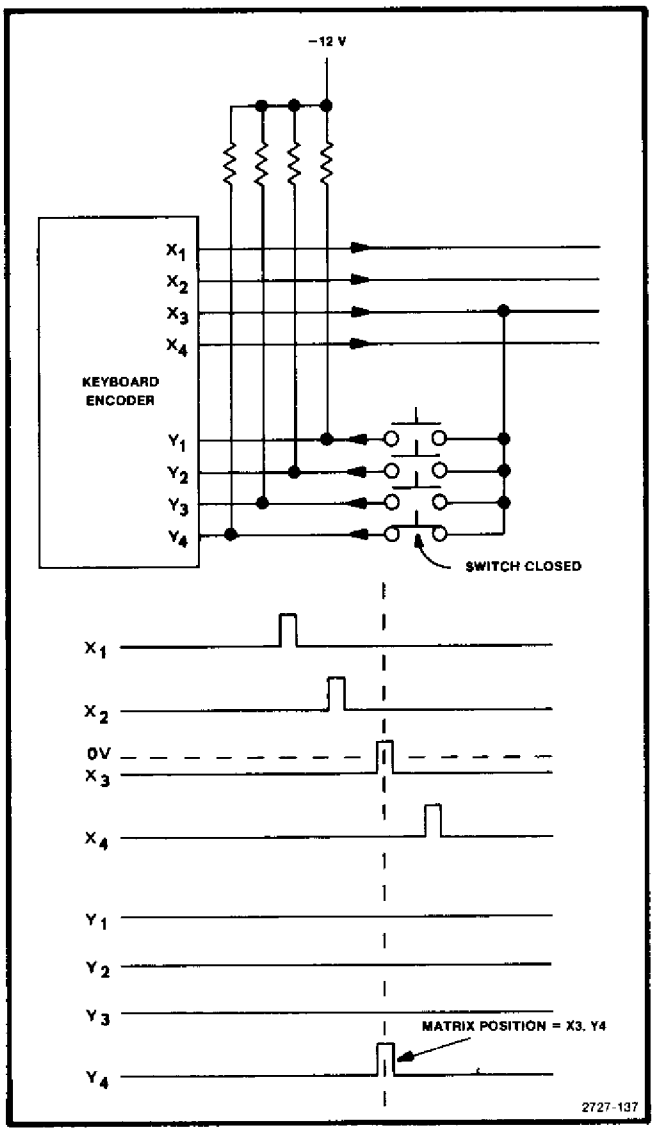


Fig. 5-34. Scan by simplified keyboard encoder.

When the control logic detects a difference between the input and a bit in the shift register, it activates the debounce mask, its latch output, and the encoder strobe output. The mask signal holds off action by the control logic so the encoder doesn't see multiple switch closures caused by switch bounce. The mask time is controlled by C4026. The latch output causes the character code, in read-only memory, addressed by the X and Y counters, to be entered in the character store. The encoder strobe output activates the encoder interrupt interface to request the microcomputer's attention.

Switch Interrupt Interface

The encoder strobe output is level controlled by the switch interrupt interface. When the encoder asserts its strobe output (high), it causes U3014C to pull down on $\overline{\text{SER REQ}}$. The strobe high also releases the preset input to U2018B, which was holding the keyboard encoder strobe control input low. Since the encoder is waiting for a low-to-high transition on this input, to stop asserting its strobe output, $\overline{\text{SER REQ}}$ remains asserted.

When the microcomputer responds to the interrupt, it learns that the keyboard encoder requested service from DB 0, the encoder's parallel poll bit. DB 0 is set low by U3014E at the same time $\overline{\text{SER REQ}}$ is asserted. The microcomputer ends its poll sequence by clearing all interrupts it has read. It does this by first setting AB7 low, disabling U3014E so it cannot continue to assert DB 0. The microcomputer then writes the parallel poll byte back on the instrument bus. If the encoder was requesting service, the low on DB 0, when written back, is clocked into U2018B when POLL is removed by the microcomputer. The output of U2018B then cancels the encoder strobe with its low-to-high transition.

Switch Matrix. The switch matrix includes both momentary contact and rotary switches. One side of each switch is connected to −12 V through a resistor in parallel with a Y input. The other side of the switch is connected in parallel with the other switches in the column to an X output.

When an X output is asserted, the Y inputs remain at a negative voltage unless a contact is closed. If the contact is closed, the X output raises the Y input for that switch to a positive voltage. Rotary switches occupy as many positions in the matrix as they have contacts. The switches are wired to yield the codes shown in Fig. 5-33.

Rotary switches for RESOLUTION BANDWIDTH and SPAN/DIV are a special case. Although each occupies four positions in the matrix, the two are used only as up/down prompts to the microcomputer to change the corresponding parameter. The microcomputer notes the initial setting and changes the parameter accordingly when the switch is moved, keeping track of the direction the switch was changed by comparing its new position to its old.

Power-up Circuit. When the microcomputer performs its power-up routine, it writes a 1 in bit 3 address 74. Because this bit is not latched, the microcomputer continues to write this 1 in the bit while the keyboard encoder is initialized.

The keyboard encoder is initialized by setting to zero the bits in the shift register that represent the rotary switches.

This happens because:

1) writing a 1 to bit 3 sets both inputs of U3012A high, turning off Q6028;

2) Q6028 off allows −12 V to be applied through R6028 to the rotary switch X inputs. This overrides the keyboard encoder X scan signals, so the Y inputs remain low without regard to the position of the switch;

3) because the microcomputer continues to write a 1 in bit 3, the keyboard encoder is given enough time to update its shift register with all zeros representing the rotary switch contacts.

After the keyboard encoder is initialized, the microcomputer resets bit 3. This restores the switch matrix to normal operation, and the keyboard encoder reads the position of the rotary switches as changes in the switch matrix. It outputs these apparent changes to the microcomputer, which interprets them as the power-up values for TIME/DIV and MINIMUM RF ATTENUATION and the initial switch position for REFERENCE LEVEL, FREQUENCY SPAN, and RESOLUTION BANDWIDTH.

FREQUENCY Encoder

The center frequency control is a rotary switch that generates a Gray code. It is decoded as shown in Fig. 5-36.

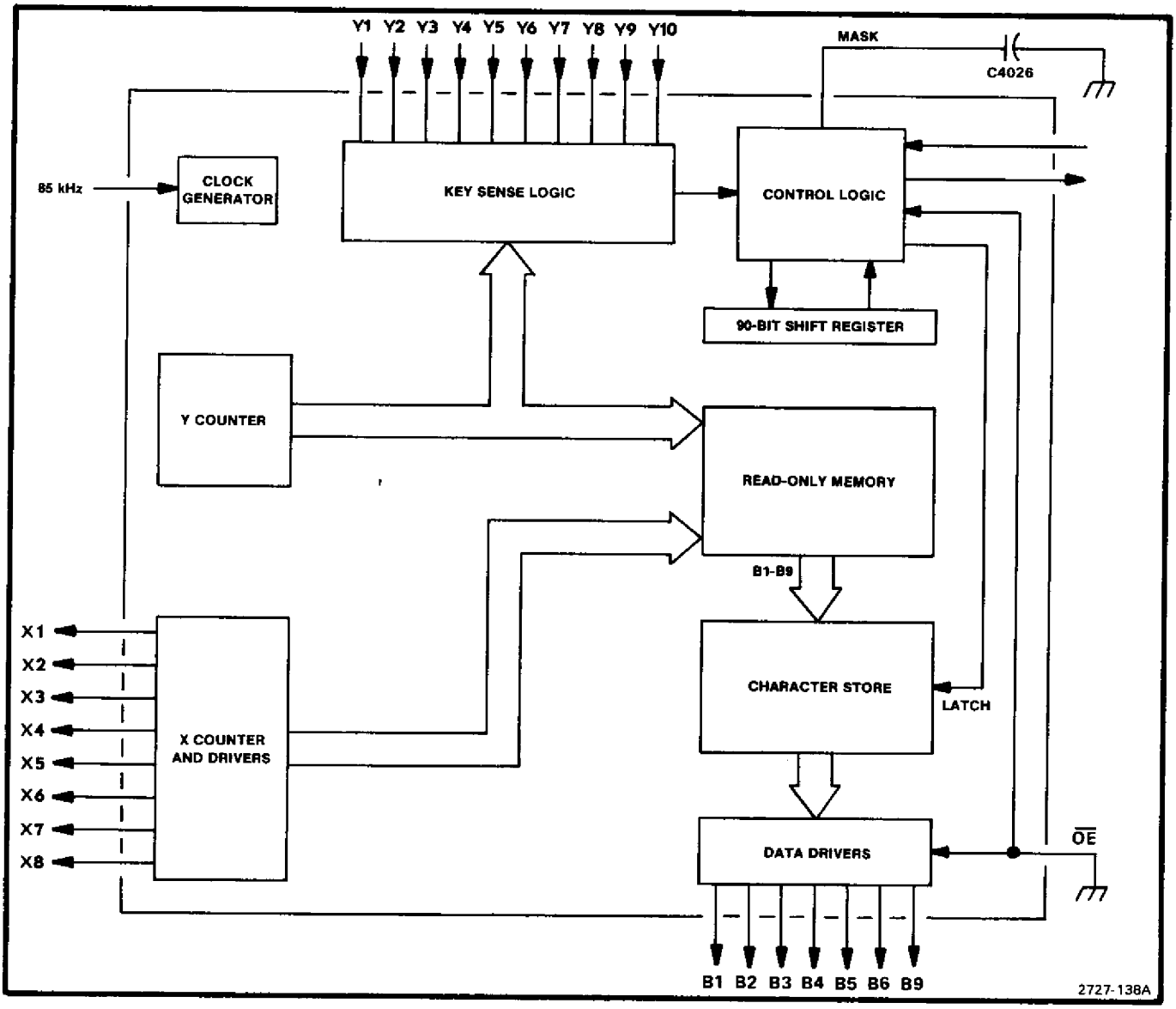


Fig. 5-35. The keyboard encoder.

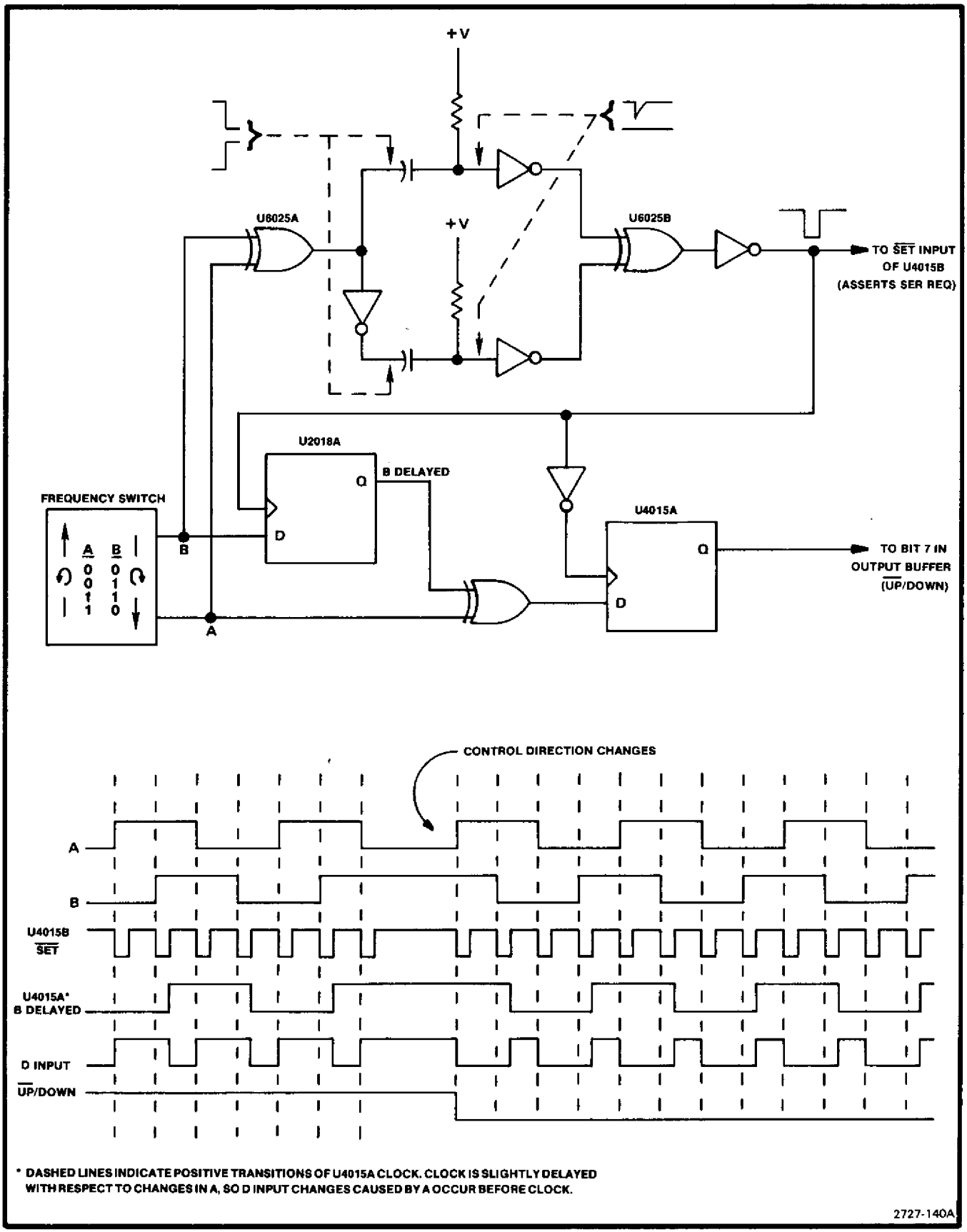


Fig. 5-36. Frequency control encoder timing.

Up/Down Encoding. The Gray code changes one bit at a time, causing U6025A to change state for each position change of the switch. This pulses a low on the input of either U5025B or U5025C (the other input remains high), making the inputs to U6025B momentarily unequal. As a result, U6025B pulses the set input of U4015B to assert $\overline{\text{SER REQ}}$.

The same pulse is inverted to clock the up/down flip-flop, U4015A. This flip-flop records the direction of change in the switch, determined by the exclusive-OR of the previous state of B and the current state of A. The trailing edge of the pulse from U6025B updates U2018A to remember the current state of B for the next cycle.

Exclusive-OR U6025D detects the direction of change in the FREQUENCY control because of the property of the Gray code. Down (counterclockwise) yields unequal inputs when the previous state of B is compared to the current state of A, while up (clockwise) yields the opposite. The up/down condition is clocked into U4015A and is read by the microcomputer as the MSB of the output port.

FREQUENCY Interrupt Interface

In its quiescent stage, U4015B is held cleared by the feedback from its Q output to its clear input. A low on its set input temporarily forces U4015B to set both its outputs high, allowing the low on the set input to set the flip-flop. When set, U4015B asserts $\overline{\text{SER REQ}}$ and drives U3014F to assert DB3 when the microcomputer performs a poll. U3014F is enabled during a poll as noted above for interrupts under Switch Encoding. U4015B is cleared (if it was asserting DB3) when the microcomputer writes back the parallel poll byte to clear all interrupts that were read.

Potentiometers

Some controls generate analog signals used by other functions in the instrument. These controls are non-programmable.

INTENSITY is an input to the Z-Axis/RF Interface board to control trace brightness.

PEAK/AVERAGE is a digital storage input that causes signals to be peak detected above, and averaged below, a display line that tracks this control.

MANUAL SCAN varies the horizontal position of the sweep in manual sweep mode.

POSITION centers the sweep and vertical deflection on the crt.

LOG CAL varies the video signal level prior to the Video Processor board.

AMPL CAL adjusts 10 MHz IF gain.

ACCESSORIES INTERFACE BOARD

The Accessories Interface board provides access to the instrument bus and connection for two analog signals. The instrument bus access may be used for diagnostics; it may also be used by future accessories.

The analog signals have two inputs; EXT VID IN and DISPLAY MARKER INPUT. The latter is used to interface the Z-Axis of the TV Sideband Adapter to the 496/496P.

The instrument bus is buffered and brought out to the rear panel with the lines named to indicate their relation to the internal bus: ADV for DATA VALID, APOLL for POLL, etc.

Two lines are added to define the 496/external device interface. One, INTL CONT, is asserted low by an external controller to disable the internal microcomputer's instrument bus buffers. This sets the address lines buffer, U2033, and control lines buffer, U2015, to drive the address, DATA VALID and POLL lines, and listen to $\overline{\text{SER REQ}}$. It also sets U2038 to indicate the direction of data through the data lines buffer, U2025, depending on the sense of the MSB of the address—AB7. When INTL CONT is low, it sets U2038 to drive the buffer in a manner similar to the Processor board data buffer—a write to the internal bus if AB7 is low and a read if AB7 is high. When INTL CONT is high, the buffer is enabled to write to the external bus when AB7 is low and read when AB7 is high.

The other line is asserted low by an external device to enable the data buffer. As long as this line, DATA BUS ENABLE, is unasserted, the data buffer is set to its high-impedance state and the data direction input has no effect on its output.

MAIN POWER SUPPLY

The Main Power Supply furnishes all the regulated voltages for the 496/496P, except for the crt high-voltage supply. In order to reduce total weight and conserve energy, the Main Power Supply is of the high-efficiency design. The power supply consists of the line input circuit, which rectifies and filters the incoming line voltage; the inverter, which drives the primary of the power transformer; the rectifier-filter circuit, which rectifies and filters the secondary voltages; the voltage reference circuit, which furnishes a stable and precise reference for the regulators; the regulator circuts, which control the voltage and current for the supplies that requires precise regulation.

The Fan Driver board houses the Fan Driver circuit, which furnishes the appropriate drive current for the fan motor. It also contains the Overvoltage Protection circuit, which shuts down the +5 V supply in case of overvoltage. Refer to Diagram 41.

MAIN POWER SUPPLY 

Line Input Circuits

Power is applied through the line filter FL301, then through the line fuse and additional normal mode/common mode EMI filtering to the power switch, from where it is sent through line selector connector J1091. The line filter prevents power line interference from entering the power supply and internally generated signals from radiating out the power cord.

Line selector connector J1091 permits the instrument to operate from either 115 V nominal or 230 V nominal line voltage source. When J1091 is in the 115 V position (pins 1 and 2), rectifiers CR3096 and CR4094 operate in conjunction with energy storage filter capacitors C6101 and C6111 as a full-wave doubler; thus, the voltage across the two capacitors is the peak-to-peak value of the line voltage. When J1091 is in the 230 V position (pins 2 and 3), CR3096, CR4095, CR3098, and CR4094 operate as a bridge rectifier. As a result, the output voltage applied to the inverter is about the same for 115 V or 230 V operation.

Thermistors RT2093 and RT2097 limit current surge to the supply at turn-on. After the analyzer is in operation, the current demand drops, the resistance value of the thermistors drops, and they have minimum effect on the circuit.

WARNING

Because C6011 and C6101 discharge very slowly, hazardous potentials exist within the power supply for several minutes after the power switch is turned off. A relaxation oscillator, formed by C5113, R5111, and DS5112, indicate the presence of voltages in the circuit until the potential across the filter capacitors is below 80 V.

S2103 is a thermal cutout switch that opens if the interior of the instrument reaches 103°C. It prevents overheating in case the cooling fan fails.

E1094 and E2095 are surge voltage protectors. When the line selector switch is in the 115 V position, only E1094 is connected across the line input. If a peak-voltage surge in excess of 230 V occurs across the input, or if the instrument is accidently connected to a 230 V source, E1094 will break down and demand enough current to open the line fuse. When the instrument is operated with the line selector at 230 V, E1094 and E2095 operate in series to protect the input against line surges of about 460 V peak.

The voltage for the line trigger source is taken off the input circuit just past S2103. It is coupled through C3085 and C3089 then off the board to the Sweep circuit to provide instrument triggering at line frequencies. The voltage at the top of R6093 is about 2 V peak-to-peak.

Inverter Circuit

The inverter consists of several stages: a multivibrator that produces a square-wave signal to drive the ramp generator and the inverter logic circuits. The ramp generator produces a low-level sawtooth ramp that is applied to the primary regulator circuit. The inverter logic circuits control the duty cycle of the inverter driver, and thus the inverter output stage. The primary regulator compares the +17 V supply output with a reference voltage, and gates the inverter logic circuits off and on to control the inverter duty cycle and thus the effective primary voltage. The inverter driver stage amplifies the signal from the inverter logic circuit and drives the output stage. The output stage consists of two power switching transistors that drive the primary of the main power transformer, T4071. Primary overcurrent sense and soft start circuit add protection.

Multivibrator. IC U6059, a low power 555 timer, is a multivibrator that operates at about 66 kHz and 80% duty cycle. Oscillator frequency is adjusted by R6061. The output square-wave signal is applied through R6052 to the primary of T6044 in the ramp generator, and directly to U6053, U6063A, U6063B, and U6069.

Ramp Generator. This circuit consists of T6044, Q5023, Q6034, and Q5032, and surrounding components. The circuit is a gated sawtooth generator that operates as follows: The negative excursion of the square-wave signal from Q6056 is coupled across T6044, forcing Q6034 into conduction. This forward-biases Q5032 and its collector moves toward +17 V, charging C5038 to this value. Shortly thereafter, Q6034 loses drive (since the pulse coupled across T6044 has died away) and the two transistors cut off. Transistor Q5023 acts as a constant-current drain to discharge C5038 linearly. This signal is coupled across divider R5036/R6032 then applied through C6039 to the input of comparator U6036, part of the primary regulator.

Primary Regulator. This circuit consists of comparator U6036 and U6046, photocoupler U6043, and related components. The circuit varies the duty cycle of the driving signal for the inverter as follows: The +17 V_1 voltage is divided by R6038 and R6037 to about +4.8 V, and applied to the inverting input of U6036. The +5 V reference is applied through R6022 to the non-inverting input of U6036, where it is combined with the ramp signal from the ramp generator stage. The non-inverting input thus receives a sawtooth signal of about 500 mV peak-to-peak imposed on +5 V dc level. This is compared with the +4.8 V on the other input, so the comparator switches with each sawtooth cycle. Now, refering to Fig. 5-37, note that as the level at pin 3 (which corresponds to +17 V supply variations) rises and falls, the duty cycle of the output waveform varies also.

The signal from the output of U6036 is applied to U6043, an optical isolator. The output of this stage is then applied to the input of U6046, a comparator. The inverting input of this device is referenced at +2.55 V, so the comparator switches at the crossing point. The purpose of the last two stages is to shift the dc level of the output signal of U6036 to CMOS levels to drive the inverter logic.

Inverter Logic. This stage consists of steering flip-flop U6063 and dual quad-input NAND gate U6069. The flip-flop is connected so it toggles back and forth and enables first one gate then the other. The square-wave signal from the multivibrator drives the clock input of U6063; the signal also enables each gate to ready it for the other signals that arrive later. Depending on the output state of U6063, either the upper or lower section of U6069 will be ready for the enabling signal. Assume for the moment that the Q output is holding pin 2 of U6069 high. This means that the complement output of the latch is holding the opposite side of the gate pair disabled. Now, when the output of U6046 moves high (U6046 controls the duty cycle of the Inverter), the upper section of U6069 produces a low state. This causes current to flow through half the primary and Q6078 only. On the opposite cycle of the multivibrator signal, the latch is reset, the lower half of U6069 is enabled, and Q6077 is in the conduction path.

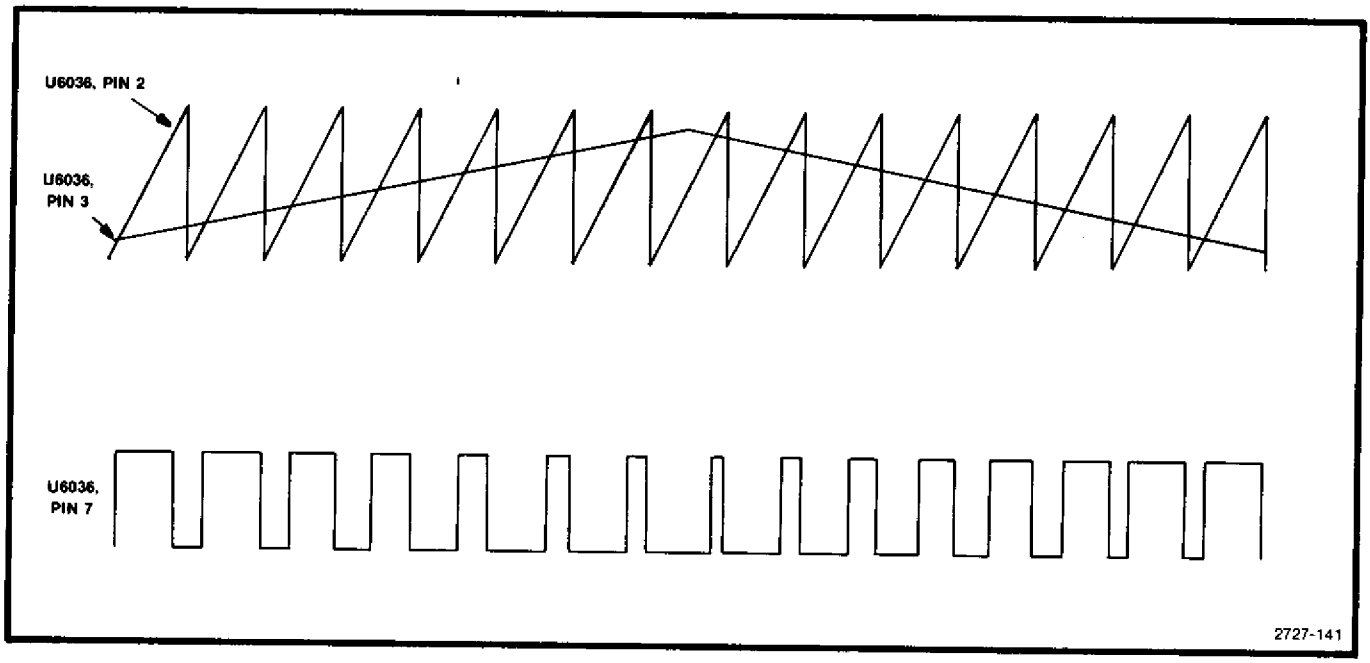


Fig. 5-37. Primary regulator input and output waveforms (stylized).

Inverter Driver. The inverter driver consists of transistors Q6077 and Q6078, transformer T6081, and related components. This is a push-pull amplifier with diode protection in the collector circuits to prevent damage from voltage transients during operation. The drive signal is induced into the two secondary windings of T6081 and coupled to the output stage.

Output Stage. This circuit consists of transistors Q2071 and Q2061, series LC tank L1081/C1063, and transformer T4071. The output transistors are connected in a half-bridge configuration, converting the previous push-pull output to a single-ended configuration. The two transistors drive the series tank which acts as an energy storage element and an averaging circuit. Output transformer T4071 is driven by the tank circuit, and in turn drives the secondary circuits.

Primary regulation, as discussed previously, is accomplished by varying the duty cycle of the main switching transistors in the inverter driver. Maximum duty cycle occurs at low input line (90 V) and fully loaded output. At maximum duty cycle, both transistors are off for only 20% of the period, or 3 μs. This short period allows any stored base charge to deplete, so there is no chance of both transistors conducting at once. Minimum duty cycle occurs at high input line (132 V) and minimum loaded output. At minimum duty cycle, each transistor is off for about 6 μs, or 40% of the total period.

Softstart and Primary Overcurrent Circuits

The soft start circuit consists of U6053 and associated components. Soft start gradually increases the switching transistor's duty cycle at turn-on or after overcurrent shutdown. This prevents excessive transistor current due to charging output capacitors. Refer to Fig. 5-38 for timing waveforms.

The primary overcurrent circuit protects against secondary shorts destroying the switching transistors. T2080 senses the collector current in Q2071 and creates a voltage on pin 5 of U6046B. If the bias on pin 5 surpasses the 2.5 V reference on pin 6, at about 5 A through Q2071, the output of U6046B sets U6063A. U6063A is a D-type flip-flop used as a timer to shut down the inverter logic for about one second. U6063A also resets the softstart circuit.

Rectifier-Filter Circuits

Transformer T4071 has three secondary windings: The first furnishes current to the +300 V and +100 V supplies; the second furnishes current to the −7 V, +7 V, and +9 V supplies; and the third furnishes current to the +17 V and −17 V supplies. The regulated supplies (+5 V reference, +5 V, −5 V, +15 V, and −15 V) derive their current from the rectifier-filter circuits.

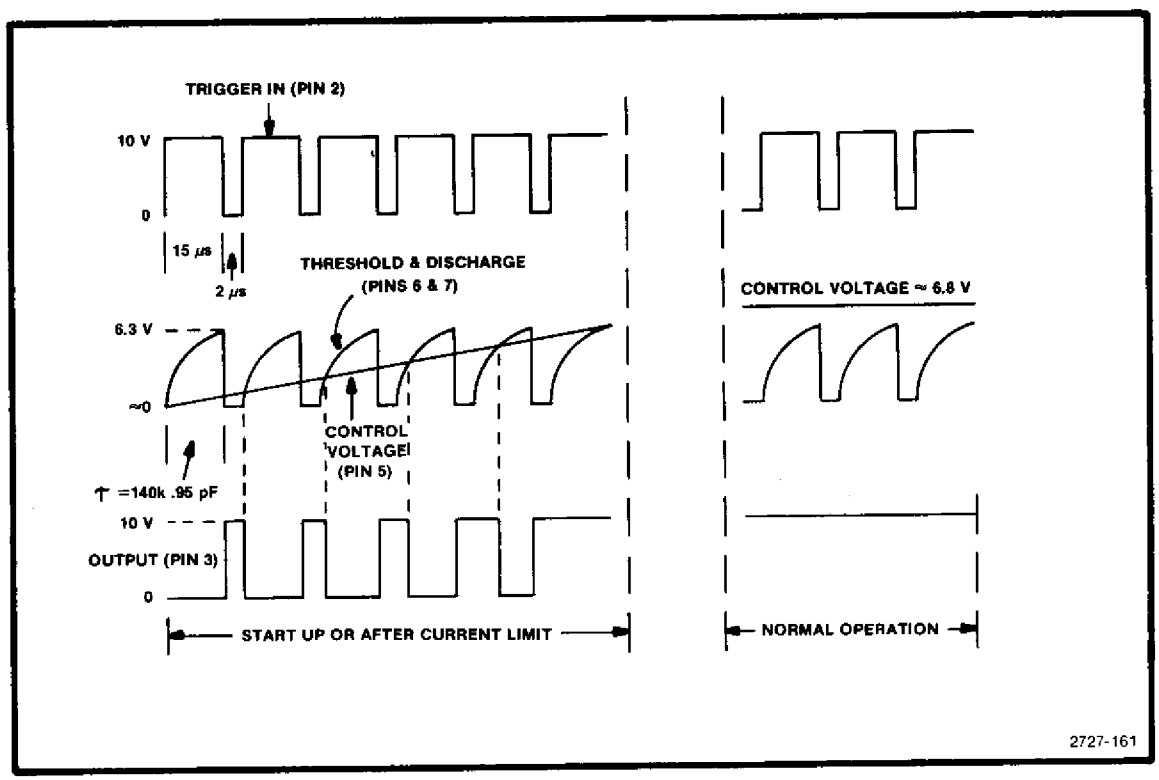


Fig. 5-38. Timing waveforms (stylized) for soft-start circuit.

The ac voltage from pins 7 and 8 of T4071 is applied to a bridge rectifier composed of CR3053, CR3056, CR3055, and CR3054. The output of this rectifier is filtered, then applied to the remainder of the instrument as the +100 V supply.

The +300 V supply is derived by stacking a 2X multiplier on the +100 V supply. CR3053, CR1042, CR1034, and CR1022 compose this circuit.

The ac voltage from pins 9 and 10 supply current to full-wave rectifier CR4061/CR4062; its output is filtered and sent to the remainder of the instrument as the +9 V supply. Two other taps off the same winding (pins 11 and 12) supply current to the bridge rectifier that consists of CR4063, CR4057, CR4053, and CR4065. The output divides across filter capacitors C3051 and C4051, to become the +7 V and −7 V supplies. The +7 V supply is only used on the power supply board; the −7 V supply is used by other circuits in the 496/496P.

The third winding of T4071 is pins 13, 14, and 15, which furnish current to full-wave bridge rectifier CR5052, CR5062, CR5065, and CR5055. The output of this rectifier is also divided to become the +17 V and −17 V supplies. The −17 V supply is used only on the power supply board; the +17 V supply is used both on the board and elsewhere in the 496/496P.

Voltage Reference Supply

The +17 V is fed through R6021 and R6020 to the voltage divider that feeds zener diode VR6026. The 6.2 V from the zener diode is divided across R6029, R6028, and R6023. +5 V REF adjustment R6028, is set for precisely +5 V at TP6027.

Regulator Circuits

Four of the available voltages from the power supply are regulated: +15 V, −15 V, +5 V, and −5 V. In function, all four regulators are the same. The circuit differences are minimal so only the +5 V regulator is discussed here. Significant differences are discussed following this description.

The voltage regulator part of the circuit is U2037A which compares the +5 V REF and +5 V SENSE voltages, amplifies the difference, and applies the change to Q2023, the driver transistor. The change is amplified by this stage and applied to the base of series-pass transistor Q2024 changing its conduction to correct for the original change to the +5 V.

The current regulator portion of the circuit is U2037B. A change in current through R2017 is applied to the non-inverting input of U2037B, which amplifies the change and applies it to the base of the driver transistor Q2023. The transistor amplifies the change which alters the bias of Q2024, causing it to restore the current flow through R2017 to its former value.

The +15 V regulator is the same as the +5 V regulator, except that the coupling circuits from the preamplifiers are separated from one another. The −15 V regulator is virtually identical to the +5 V regulator. The −5 V regulator differs from the others in that a driver stage is not required, so the preamplifiers drive the series-pass transistor (Q5013) directly.

Over-voltage Protection Circuit

Zener diode VR1015 and SCR Q1010 form the over-voltage protection circuit. If the +5 V supply passes +6 V, the potential on the gate of Q1010 biases it into conduction. This forces the +5 V supply to ground; it remains at ground potential until the analyzer is de-energized and turned on again.

Fan Drive Circuit

The Fan Drive circuit provides a temperature-controlled current drive to the fan motor. The circuit produces a three-phase drive current of approximately 240 Hz operating frequency. The actual drive circuit operates as a ring counter.

Transistors Q1038 and Q1044 form a current regulator that is controlled by thermistor RT2045, the value of which varies inversely with the internal temperature of the analyzer. The thermistor and a companion resistor R2042, fix the voltage at the emitter of Q1044 at about −13 V at turn-on, and more positive as the analyzer warms up.

The ring counter consists of three stages: Q1025 and Q1020, with R1031/C1032 and R1027/C1018 as the frequency-determining components; Q2025 and Q1018, with R1033/C1033 and R2019/C1019 as the frequency-determining components; and Q2030 and Q2020 with R2014/C2012 and R2016/C2018 as the frequency-determining components. When the analyzer is energized, one of the three ring counter stages begins conducting before the others, owing to circuit imbalances. Assume that the upper stage (Q1025 and Q1020) begins conducting before the others. The collector voltage of Q1025 is near −17 V which fixes that point as the most negative in a ring consisting of R1032, R1029, R1028, R2036, R2034, and R1036. Since the emitter voltage of the three control transistors (Q1020, Q1018, and Q2020) is the same, the voltage division around

the resistive ring is such that Q1018 and Q2020 remain cut off. When the capacitive charge that holds Q1020 in conduction bleeds off, the transistor cuts off and the next stage can begin to conduct. The remaining two are in turn prevented from operating until the RC combination discharges. The fan motor inductance works in conjunction with the RC components to regulate the switching of the stages.

This ring-counter action builds up slowly until the circuit is producing a three-phase drive signal of about 240 Hz. The inductance of the motor coils round off the otherwise sharp corners of the driving signal, so the current waveform looks a great deal like the output of a half-wave rectifier at P2020, pins 1, 2, and 3. Each of the driving signals are approximately 120° apart, so as to drive the motor.

The rackmount/benchtop versions require an external fan, B200. When this fan is connected, the internal fan (B100) is disconnected.

496P GENERAL PURPOSE INTERFACE BUS 39

The 496P, unlike the 496, includes GPIB capability provided by two boards: the GPIB board and the GPIB Interface board. The GPIB board contains ROM and RAM used by interface functions and the interface between the microcomputer and the GPIB. The GPIB Interface board holds the GPIB buffers and address switches.

Address Decoding

RAM. RAM on the GPIB board supplies I/O buffer space for GPIB transfers. The RAM ICs, four bits wide, are paired to make 8-bit bytes at each address. For instance, U1032 and U1042 are both selected when $\overline{\text{HIRAM}}$ is asserted. The 10 lower bits on the address bus select an address cell within each IC. The RAM address range, 800 to 1000 (hex), is decoded by half of U1028. Either RAM select line is enabled by $\overline{\text{GPIBRAM}}$ from the Processor board and the state of A10 on the address bus.

GPIB Interface and Address Switch Register. Either the GPIB interface (U2047) or the address switch register (U3039) is selected by the other half of U1028. The select line for either is enabled by GPIA from the Processor board and chosen by A3. When A3 equals 0, it selects the GPIB interface; when A3 equals 1, it selects the switch register. The GPIB interface is described below. The address switch register is a buffer, U3039, for the rear-panel GPIB ADDRESS, LF OR EOI, TALK ONLY, and LISTEN ONLY switches.

ROM. ROM on the GPIB board contains the portion of the instrument operating system that handles GPIB data transfers. This portion of the firmware decodes and responds to messages received on the bus, transferring control to the appropriate subroutines in Memory board firmware to execute the actions called for by the message.

The ROM address space is divided into two banks, either of which can be filled with four 2k packages or a single 8k package. Straps on the board are set to control decoder U1021 and to route signals as needed to match the ICs that are installed. For 2k ROMs, U1021 decodes A11 through A13 to assert one of its eight chip-enable outputs during a read cycle within the ROM address range (4000—8000, i.e., A14 high and A15 low). For 8k ROMs, U1021 decodes only A13 to assert either its Y0 or Y4 output. Straps on U2012 and U3012 inputs are set to apply the correct enable and address signals for either kind of ROM.

GPIB Interface

The GPIB interface is based on the 9914 general purpose interface adapter (GPIA). U2047, the GPIA, performs the majority of the functions specified in IEEE Standard 488-1978 and allows firmware implementation of the rest of those functions. These functions are not explained here, but are discussed in some detail in an appendix in the 496P Programmer's manual.

The GPIA's internal logic handles:

Source and acceptor handshakes
Talker and listener functions
Recognizing GPIB address
Service request (SRQ)
Remote/local function
Local lockout
Serial and parallel poll response
Respond to device clear
Respond to device trigger
NRFD holdoff when receiving data

GPIA Block Diagram

The bus and register organization of the GPIA is shown in Fig. 5-39. The 13 registers are the vehicles used for communication between the 496P microcomputer and the GPIB. Some registers provide a link between the microcomputer and GPIB; others are used by the microcomputer to control the GPIA and obtain status information.

The registers are addressed by signal lines RS0 through RS2 and the DBIN input (connected to the microcomputer read/write line): DBIN high selects read registers, DBIN low selects write registers. The registers are shown in Table 5-22.

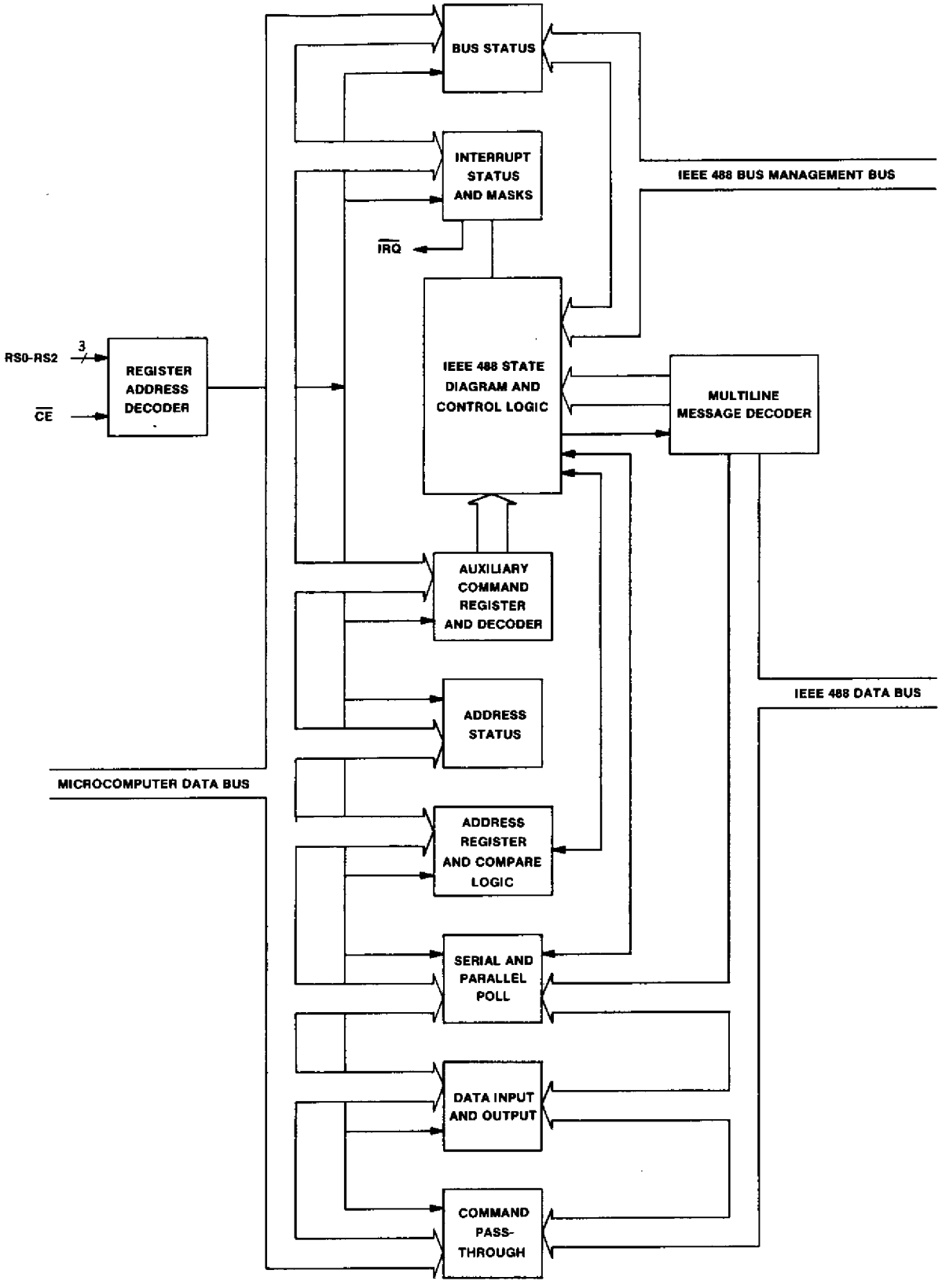


Fig. 5-39. 9914 GPIA block diagram.

Table 5-22
GPIA REGISTERS

Register	Type	RS2	RS1	RS0	DBIN & WE
Interrupt Status 0	Read	0	0	0	1
Interrupt Mask 0	Write	0	0	0	0
Interrupt Status 1	Read	0	0	1	1
Interrupt Mask 1	Write	0	0	1	0
Address Status	Read	0	1	0	1
Bus Status	Read	0	1	1	1
Auxiliary Command	Write	0	1	1	0
Address Switch	Read	1	0	0	1
Address	Write	1	0	0	0
Serial Poll	Write	1	0	1	0
Command Pass Through	Read	1	1	0	1
Parallel Poll	Write	1	1	0	0
Data In	Read	1	1	1	1
Data Out	Write	1	1	1	0

Two interrupt status registers keep track of changes that may require microcomputer attention: data byte received or sent, EOI, GET, DCL, or IFC received, a remote/local state change has occurred, and ATN going false are examples. Corresponding interrupt mask registers are set by the microcomputer to control interrupt status results in an interrupt.

The address status register indicates the remote/local state of the GPIA, the state of ATN, and the listener/talker addressed states. The bus status register reflects the current state of GPIB bus management lines.

The auxiliary command register receives commands that control chip functions and local messages to the GPIA functions (such as rtl—return to local).

The address register contains the instrument's primary address.

The serial poll register contains the status byte.

The command pass-through register connects the GPIB data lines to the microcomputer data lines to transfer commands not automatically handled by the GPIA.

The parallel poll register is used by the microcomputer to respond to a parallel poll.

The data-in and data-out registers are the route for data transferred between the microcomputer bus and the GPIB when the instrument is either addressed as a listener or talker. The 9914 automatically asserts NRFD until the microcomputer reads the data-in register.

GPIB Buffers. Two transceivers on the GPIB Interface board buffer signals on the GPIB.

The data bus buffers, in U1012, are controlled by two signals: TE (talk enable) and PE (pull-up enable). TE from the GPIA sets the direction of data flow: high means GPIA to GPIB and low GPIB to GPIA. PE low disables the driver pull-ups for open collector operation when ATN is asserted; this disables tri-state operation, which is required during a parallel poll (when ATN is asserted).

The bus management buffers in U1011 are automatically configured by TE and ATN to operate in the required direction (driving DAV and EOI when TE is high and NDAC and NFRD when TE is low).

RACKMOUNT/BENCHTOP VERSIONS

Introduction

The rackmount version of the 496/496P Spectrum Analyzer (Option 30) is designed to mount in a standard 19-inch rack. The benchtop version (Option 32) is the same as the rackmount except it has side panels with handles and it also has feet installed on the bottom. Both have a larger fan to provide additional cooling. Option 31 provides access to all front-panel connections via the cabinet rear panel.

This section describes characteristics of the rackmount/benchtop versions, mounting procedure, and servicing procedures for the rackmount/benchtop instruments.

Electrical Characteristics

Electrical characteristics for the 496/496P are applicable for the rackmount/benchtop version of the 496/496P except residual (FM'ing) response, and frequency response, when Option 31 is included. Rackmount versions, subject to externally induced vibrations from rack cooling fans or the surrounding equipment, may show degradation of the FM'ing characteristic. Because of different rack configurations, this degradation cannot be specified. In a typical fan-cooled rack, degradation increases by a factor of two.

Table 6-1
ENVIRONMENTAL CHARACTERISTICS

Rackmount versions meet MIL T-28800B, type III, class 5, style F specifications. Benchtop version meets MIL T-28800B, type III, class 5, style E specifications. Some of the details are as follows:

Temperature and Humidity	Temperature °C	Relative Humidity %
Operating	0 to 25	95 +5, −0
	25 to 40	75 ±5
	40 to 50	45 ±5
Non-operating	−55 to 75	95 +5, −0
Altitude		
Operating	10,000 feet	
Non-operating	40,000 feet	
Vibration		
Operating	Method 514 Procedure X (modified MIL-STD-810C). Vibration limit is 1 G. Resonance searches along all three axes at .0065 inch; frequency varied from 10 to 55 Hz, 15 minutes per axis, plus dwell at resonant frequency of 33 Hz for 10 minutes per axis. Total vibration time 75 minutes. Instrument secured to vibration platform during test.	
Shock	For Option 31, the semi-rigid coaxial cables running from the front panel to the rackmount cabinet grill must be removed for this test.	
Transit Drop	Not applicable.	
Bench Handling	The bail for tilting the instrument shall be folded and the semi-rigid cables from the front-panel connectors to the front grill connectors (Option 31) shall be removed for this test.	
Transportation		
Package vibration	Meets National Safe Transit Association's pre-shipment test (project 1A-B-1) when correctly packaged. One hour vibration of 1 G.	
Package drop	Operable after a 24-inch drop on any corner or flat surface.	

Table 6-2
PHYSICAL

Weight (standard accessories except manuals)	70 pounds maximum rackmount version and 68 pounds for benchtop version.
Dimensions	
Rackmount (without side rails)	8.75 X 16.89 X 25.00 inches (22.23 X 42.9 X 63.5 cm)
Benchtop (with feet and handles)	9.25 X 17.9 X 25.00 inches (23.5 X 45.47 X 63.5 cm)
Benchtop (without feet or handles)	8.75 X 16.89 X 25.00 inches (22.23 X 42.90 X 63.5 cm)

STANDARD ACCESSORIES

Standard accessories are the same as the 496/496P with the addition of rack slides for the rackmount (Tektronix Part No. 351-0375-01). An accessories drawer provides storage space in place of the front cover. Option 31 includes semi-rigid cabling to connect the front-panel connectors to the cabinet rear connectors; and a front-panel grill.

OPTIONAL ACCESSORIES

Same as the 496/496P except for the transit case

RACKMOUNTING INSTALLATION DIMENSIONS

Height. At least nine inches of vertical space is required to mount this instrument in a cabinet rack.

Width. Minimum width of the opening between the left and right front rails of the rack must be 17.9 inches. This allows room on each side of the instrument for the slide-out tracks to operate freely, permitting the instrument to move smoothly in and out of the rack.

Depth. The rackmount version requires 25 inches behind the front rails for air circulation, power cord, and the necessary mounting hardware.

SLIDE-OUT TRACKS

WARNING

If the left and right slide-out tracks are reversed, the safety latch can be defeated, allowing the instrument to be pulled out of the rack. When mounting the slide-out tracks, differentiate the left assembly from the right and mount only as directed in these instructions.

The hardware provided for mounting the slide-out tracks is shown in Fig. 6-1. Since the hardware is intended to make the tracks compatible with a variety of cabinet racks and installation methods, only part of the hardware will be needed for this installation.

Figure 6-2 shows the rackmount version installed in a cabinet-type rack. The slide-out tracks provided permit it to be extended out of the rack for access to the back connectors. To operate in the extended position, be sure the power cord and any interconnecting cables are long enough for this purpose. When not extended, the instrument is held in the rack with securing screws (see Fig. 6-2A).

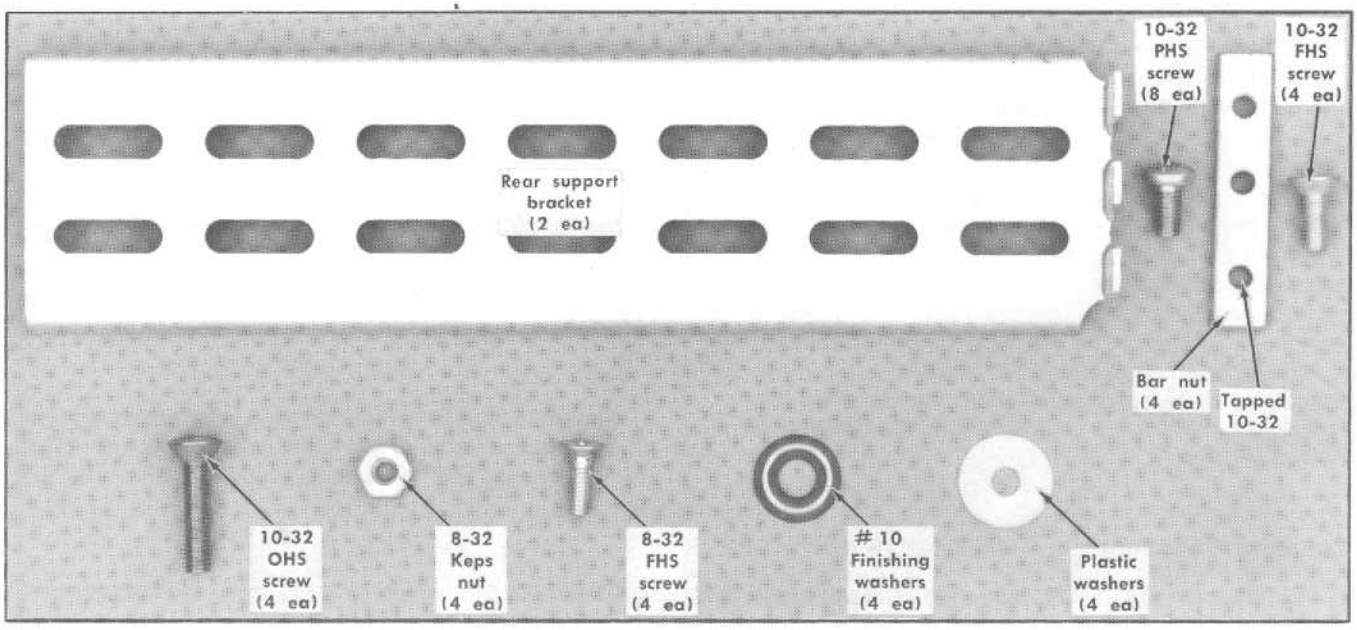


Fig. 6-1. Hardware provided for slide track mounting.

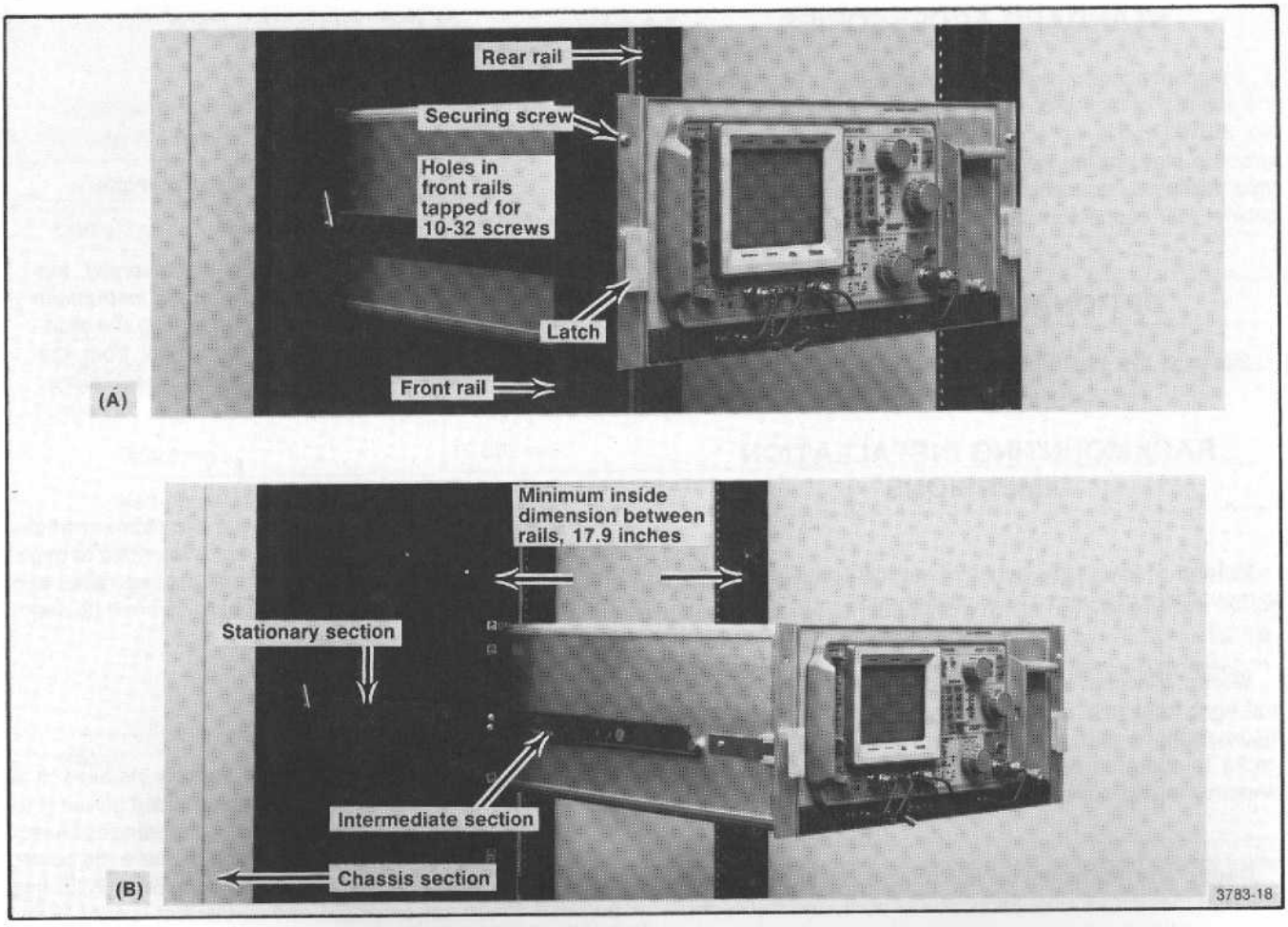


Fig. 6-2. Instrument installed in a cabinet-type rack.

The slide-out tracks consist of two assemblies—one for the left side of the instrument and one for the right side. Figure 6-3 shows the complete slide-out track assemblies. The stationary section of each assembly attaches to the front and rear rails of the rack, and the chassis section is attached to the instrument. The intermediate section slides between the stationary and chassis sections and allows the instrument to be extended out of the track. *When the instrument is shipped, the stationary and intermediate sections of the tracks are packaged as matched sets and should not be separated.* To identify the left or right assembly note the position of the automatic latch (see Fig. 6-3). When mounted in the rack, the automatic latch should be at the top of both assemblies. The chassis sections are installed on the instrument at the factory.

Mounting Procedure

The front flanges of the stationary sections may be mounted in front of (outside) or behind (inside) the front rails of the rack, depending on the type of rack. If the front rails of the rack are tapped for 10-32 screws, the front flanges are mounted outside of the rails. If the front rails of the rack are not tapped for 10-32 screws, the front flanges are mounted inside the front rail and a bar nut is used. Figure 6-4 shows these methods of mounting the stationary sections.

Use the following procedure to install the rackmount version in a rack:

1) select the proper front-rail mounting holes for the stationary sections, using the measurements shown in Fig. 6-5;

2) if the mounting flanges of the stationary sections are to be mounted in front of the rails (rails tapped for 10-32 screws), mount each stationary section as shown in Fig. 6-4A;

3) if the mounting flanges of the stationary sections are to be mounted behind the front rails (rails not tapped for 10-32 screws), mount each stationary section as shown in Fig. 6-4B;

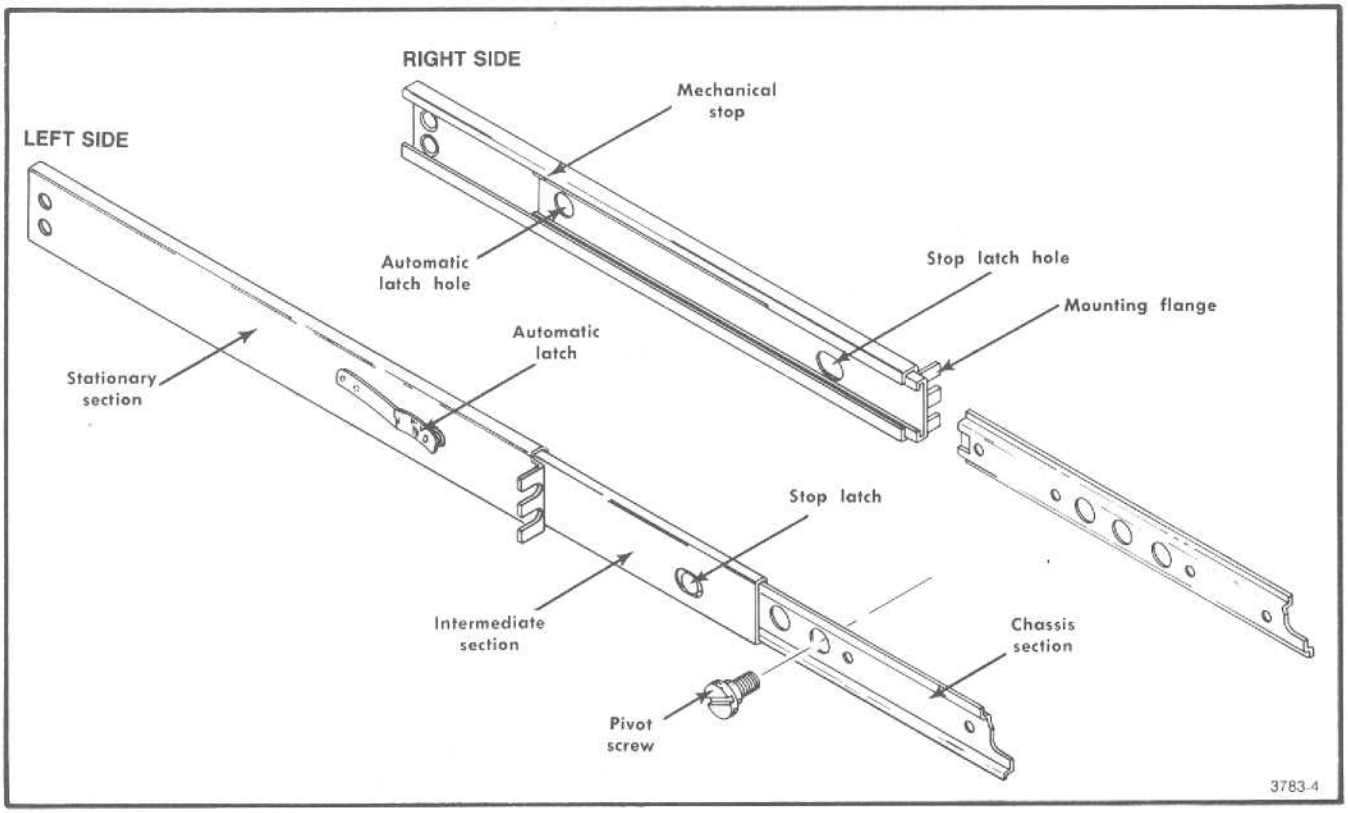


Fig. 6-3. Complete slide-out track assemblies.

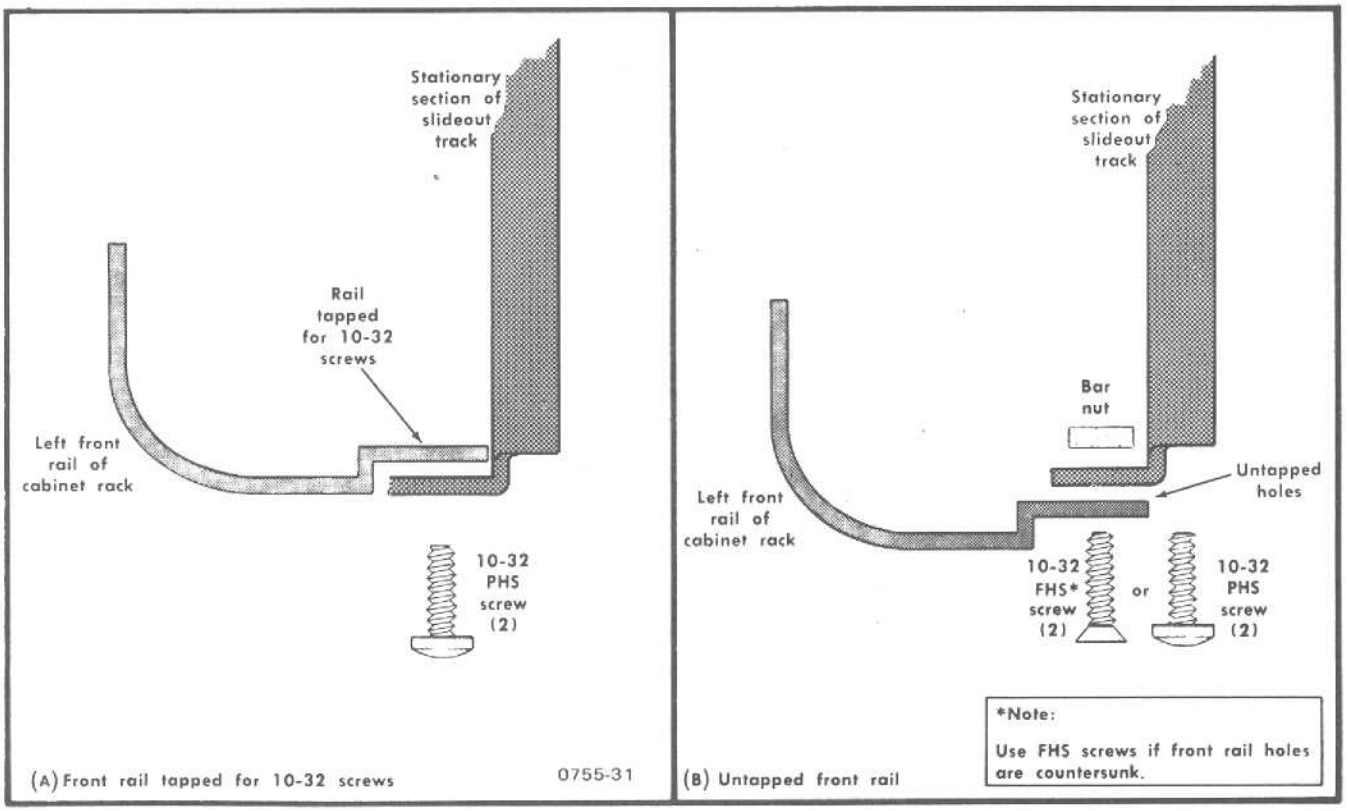


Fig. 6-4. Methods of mounting the stationary sections.

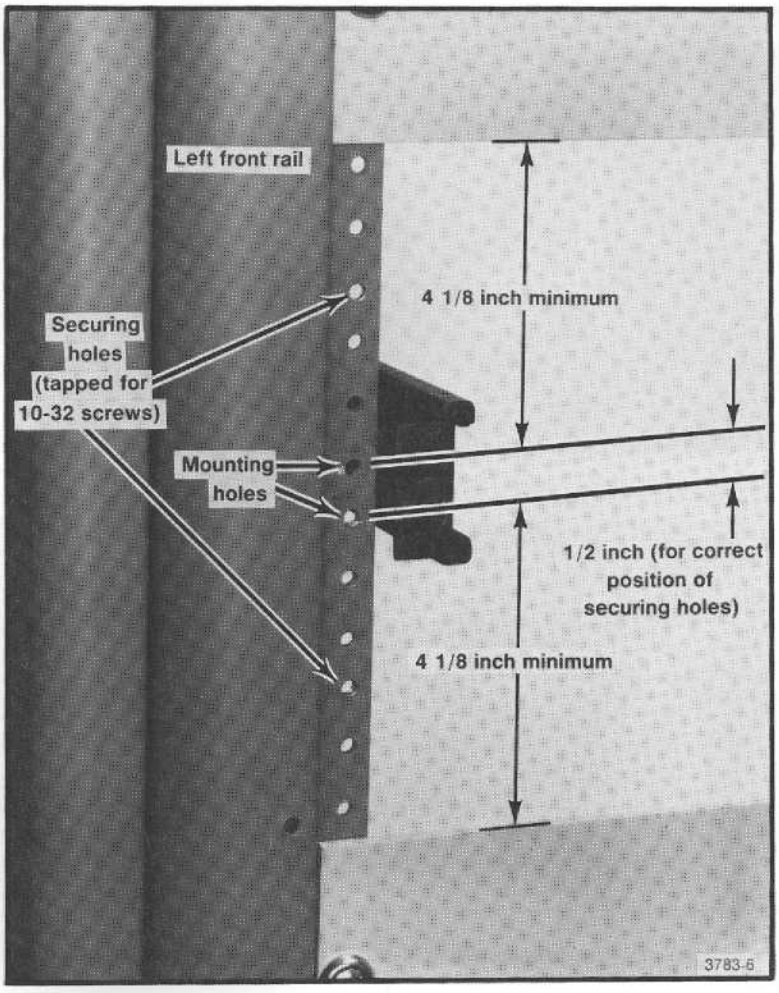


Fig. 6-5. Measurements of front-rail mounting holes for the stationary sections.

4) refer to Fig. 6-6 to insert the instrument into the rack. Do not connect the power cord or install the securing screws until all adjustments have been made;

5) position the instrument so the pivot screws (widest part of instrument) are approximately even with the front rails;

6) adjust the alignment of the stationary sections according to the procedure outlined in Fig. 6-7;

7) after the tracks operate smoothly, connect the power cord to the power source;

8) push the instrument fully into the rack and secure it to the rack with the securing screws as shown in Fig. 6-6.

CAUTION

If the rackmount version is extended out of the rack and tipped up to gain access to the bottom or back panels of the instrument, it can swing past center and fall back into the rack unless it is held. Use care when doing this to avoid damaging the front panel or equipment that may be mounted above the 496/496P.

Alternate Rear Mounting Methods

CAUTION

The following methods provide satisfactory mounting under normal conditons; however, they do not provide solid support for the rear of the instrument. If the instrument should be subjected to severe shock or vibration consult your local Tektronix Field Engineer for better rear support mounting information.

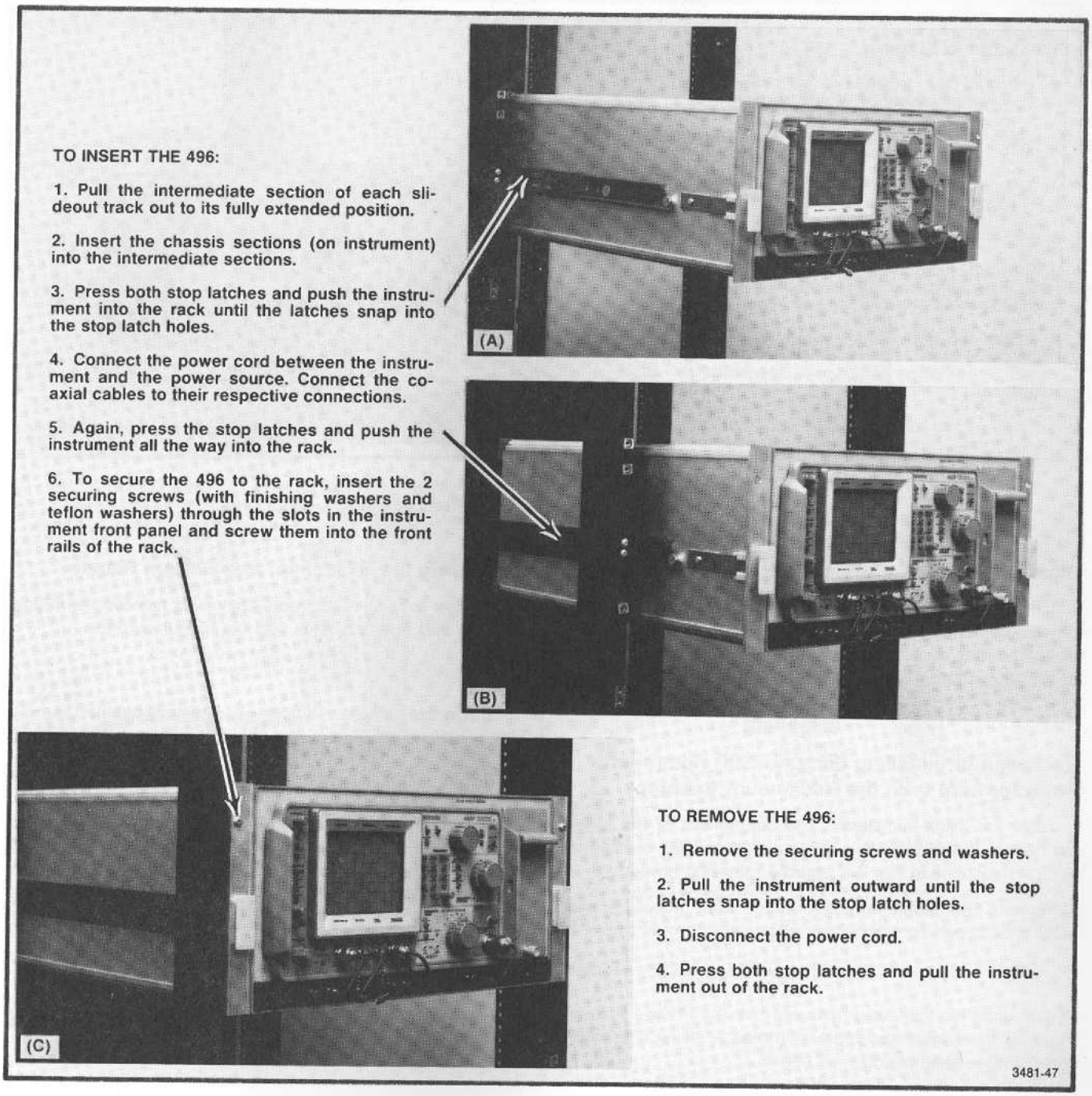


Fig. 6-6. Procedure for inserting or removing the instrument.

An alternative support method for the rear of the instrument is shown in Fig. 6-8. The rear support brackets, supplied with the instrument, are to be used in a rack which has a spacing between the front and rear rails of 11 to 24 inches. Figure 6-8A illustrates the mounting method if the rear rails are tapped for 10-32 screws and Fig. 6-8B illustrates the mounting method if the rear rails are not tapped for 10-32 screws.

If the rack does not have a rear rail, or if the distance between the front and rear rails is too great, the instrument may be mounted without the use of the slide-out tracks. Fasten the instrument to the front rails of the rack with the securing screws. This mounting method should be used only if the instrument will not be subjected to shock or vibration and it is installed in a stationary location.

TO ADJUST ALIGNMENT:

1. Position the instrument with the pivot screws approximately even with the front rails.

2. Loosen the mounting screws at the front of both stationary sections (left side shown).

3. Allow the tracks to seek their normal positions with the instrument centered in the rack.

4. Tighten the mounting screws.

5. Push the instrument all the way into the rack. If tracks do not slide smoothly, check for correct spacing between the rear supports.

6. Check the vertical positioning of the 496 front panel with respect to adjacent instruments or panels. If not correct, reposition as necessary.

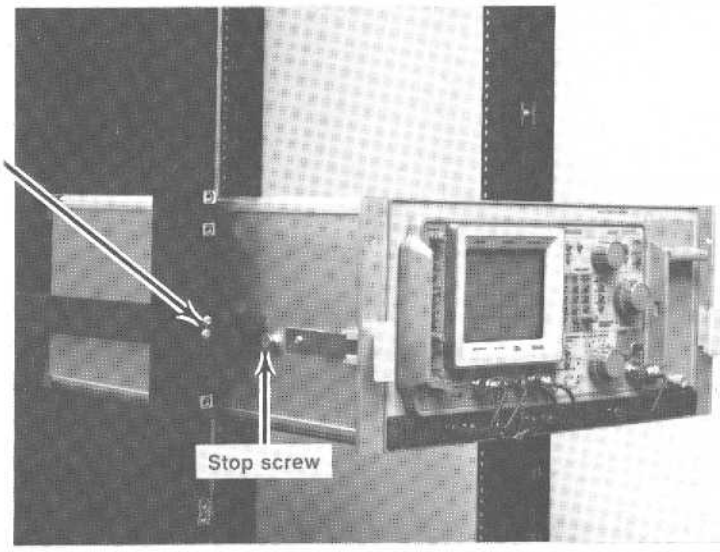


Fig. 6-7. Alignment adjustment for correct operation.

Slide-out Track Lubrication

The special finish on the sliding surfaces of the tracks provide permanent lubrication. However, if the tracks do not slide smoothly even after proper adjustment, a thin coating of paraffin rubbed onto the sliding surfaces may improve operation.

Removing or Installing the 496/496P Spectrum Analyzer from or in the Rackmount Cabinet

After the initial installation and adjustment of the slide-out tracks, the 496/496P is removed or installed by following the directions in Fig. 6-6 and the following procedure:

1) remove the rackmount instrument from the rack and place it on a bench;

2) at the rear of the instrument, remove the Phillips screws that hold the blower assembly on the back of the 496/496P and pull the assembly off;

3) use a 5/32 Allen wrench to loosen and remove the four screws that secure the rear panel of the 496/496P to the back of the rackmount cabinet;

4) push or pull the instrument from the rackmount cabinet;

5) before the 496/496P will operate, a cut-off switch must be closed. This is accomplished by reinstalling the blower assembly on the back panel of the 496/496P.

Removing the Side, Top, and Bottom Panels

1. Use a Torx "T20" screwdriver to remove the fillister screws that hold the back feet on all four corners.

2. On the side panels of the rackmount cabinet, remove the pivot and stop screw for the side rail track assembly.

3. Slide the panel back and off the cabinet. Note: When replacing the panels, be sure to start the EMI strip under the panel before sliding the panel forward; otherwise, the panel will catch the strip and bend the end. Use a pointed object such as a screwdriver to push the end of the EMI strip down while pushing the panel forward.

4. The EMI strip can be replaced by removing the back feet mounting plate and sliding the strip out of its channel.

Installing Semi-rigid Coaxial Cables to Access the Cabinet Rear Panel Connectors to the Front Panel of the Instrument (Option 31)

1. Remove the 496/496P instrument from the cabinet, then slide the bottom panel off as per instructions on removing the panels.

2. To gain access to the mounting nuts that hold the front panel grill in place, remove the horizontal support bar across the front section of the cabinet.

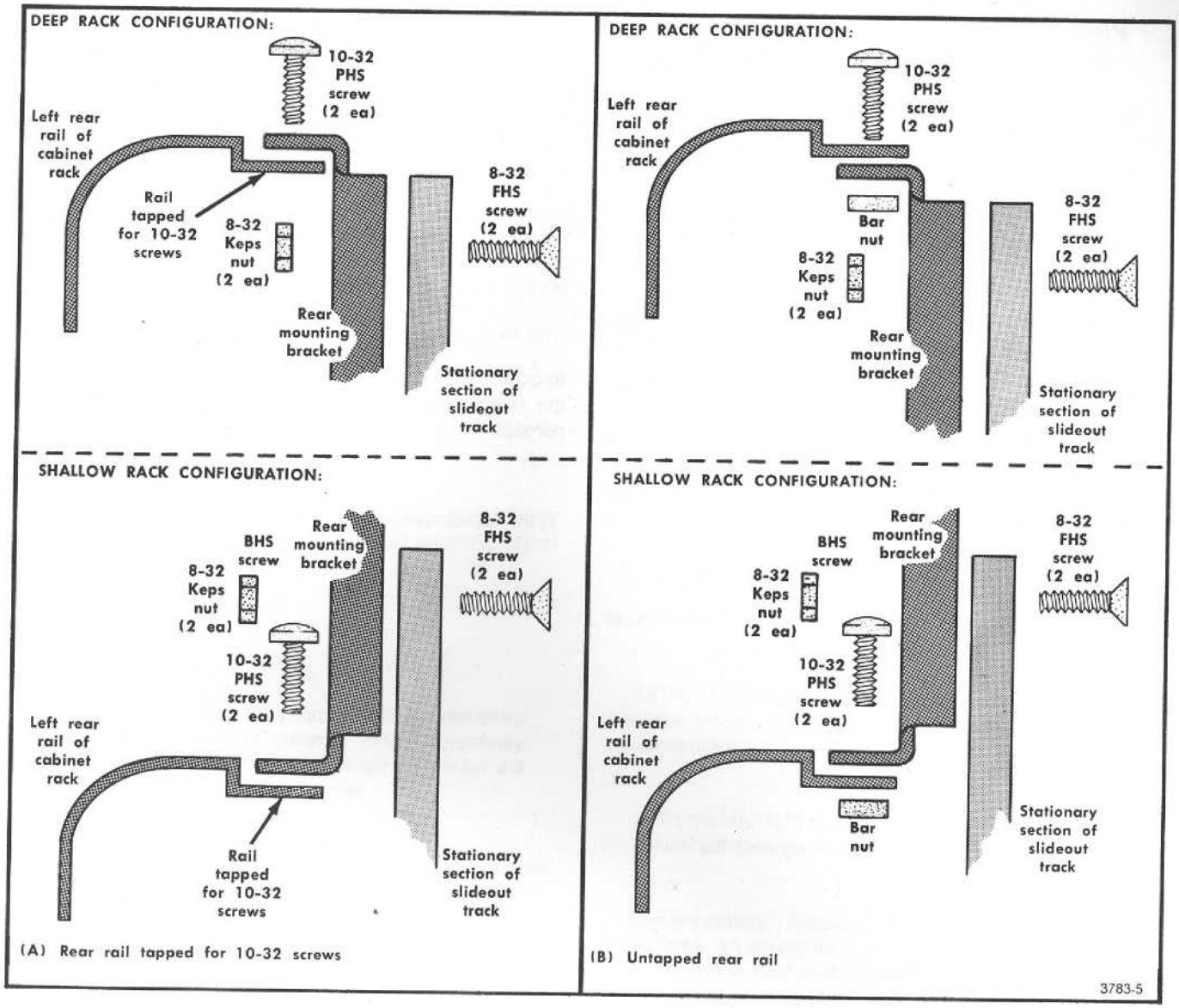


Fig. 6-8. Alternative method of installing the instrument using rear support brackets.

3. Remove the front panel grill and install the Option 31 grill. (Option 31 panel has punched openings for mounting the coaxial SMA connectors.)

4. Install the four SMA coaxial connectors in the new grill.

5. Position the cables with RF connectors in their appropriate back panel access hole. Install the mounting nuts for each connector and secure.

6. Connect the semi-rigid cables to the SMA connector, mounted in the front panel grill, and tighten until they are just snug.

CAUTION

Do not tighten coaxial connectors beyond the point the cable or connector starts to twist. Use a second wrench to hold the connector or cable nut as the other nut is tightened.

7. Attach the cable clamps to hold the cables to the mounting posts on the bottom of the instrument housing.

8. Reinstall the support brace across the bottom of the cabinet, then reinstall the bottom panel.

PREPARING THE INSTRUMENT FOR CALIBRATION OR MAINTENANCE

Before the 496/496P instrument can be removed from the rackmount/benchtop cabinet, the fan must be removed. After the instrument is removed from the cabinet the fan must be reconnected before power can be applied and the instrument turned on.

Prepare the instrument for maintenance as follows:

1) if the instrument is rackmounted and has the semi-rigid cables to the back panel (Option 31), disconnect the instrument semi-rigid cables between the 496/496P front panel and the connectors on the front grill of the cabinet;

2) disconnect all external connections to the instrument, including the power cord, and remove the rackmounted 496/496P;

3) place the rackmount/benchtop instrument on its face;

4) loosen the two fan assembly mounting screws and remove the fan assembly;

5) use a 5/32-inch Allen wrench to loosen and remove the four screws that hold the instrument to the cabinet back panel;

6) carefully align the fan assembly power connector pins to the receptacle on the back panel of the instrument and reinstall the fan assembly. Reconnect the power cord;

7) the instrument is now ready for calibration or repair.

APPENDIX A

GLOSSARY

The following glossary is presented as an aid to better understand the terms as they are used in this document and with reference to spectrum analyzers.

GENERAL TERMS

Spectrum Analyzer. An apparatus which is generally used to display the power distribution of an incoming signal as a function of frequency.

NOTE

It is useful in analyzing the characteristics of repetitive electrical waveforms in general, since repetitively sweeping through the frequency range of interest will display all components of the signal.

Center Frequency. That frequency which corresponds to the center of a frequency span, expressed in hertz.

dBc. dB below carrier level.

Effective Frequency Range. That range of frequency over which the instrument performance is specified. The lower and upper limits are expressed in hertz.

Full Span (Maximum Span). A mode of operation in which the spectrum analyzer scans an entire frequency band.

Zero Span. A mode of operation in which the frequency span is reduced to zero.

Envelope Display. The display produced on a spectrum analyzer when the resolution bandwidth is greater than the spacing of the individual frequency components.

Line Display. The display produced on a spectrum analyzer when the resolution bandwidth is less than the spacing of the signal amplitudes of the individual frequency components.

Line Spectrum. A spectrum composed of signal amplitudes of the discrete frequency components.

Maximum Safe Input Power

WITHOUT DAMAGE. The maximum power applied at the input which will not cause degradation of the instrument characteristics.

WITH DAMAGE. The minimum power applied at the input which will damage the instrument.

Intermodulation Spurious Response (Intermodulation Distortion). An unwanted spectrum analyzer response resulting from the mixing of the nth order frequencies, due to non-linear elements of the spectrum analyzer, the resultant unwanted response being displayed.

Baseline Clipper (Intensifier). Increasing the brightness of the signal relative to the baseline portion of the display.

Pulse Stretcher. A pulse shaper that produces an output pulse, whose duration is greater than that of the input pulse, and whose amplitude is proportional to that of the peak amplitude of the input pulse.

Video Filter. A post detection lowpass filter.

Scanning Velocity. Frequency span divided by sweep time and expressed in hertz per second.

TERMS RELATED TO FREQUENCY

Display Frequency. The input frequency as indicated by the spectrum analyzer and expressed in hertz.

Frequency Span (Dispersion). The magnitude of the frequency band displayed, expressed in hertz or hertz per division.

Frequency Linearity Error. The error of the relationship between the frequency of the input signal and the frequency displayed (expressed as a ratio).

Frequency Drift. Gradual shift or change in displayed frequency over the specified time due to internal changes in the spectrum analyzer, and expressed in hertz per second, where other conditions remain constant.

Residual FM (Incidental FM). Short term displayed frequency instability or jitter due to instability in the spectrum analyzer local oscillators, given in terms of peak-to-peak frequency deviation and expressed in hertz or percent of the displayed frequency.

Impulse Bandwidth. The displayed spectral level of an applied pulse divided by its spectral voltage density level assumed to be flat within the pass-band.

Static (Amplifier) Resolution Bandwidth. The specified bandwidth of the spectrum analyzer's reponse to a cw signal, if sweep time is kept substantially long.

NOTE

This bandwidth is the frequency separation of two down points, usually 6 dB, on the response curve, if it is measured either by manual scan (true static method) or by using a very low speed sweep (quasi-static method).

Shape Factor (Skirt Selectivity). The ratio of the frequency separation of the two (60 dB/6 dB) down points on the response curve to the static resolution bandwidth.

Zero Pip (Response). An output indication which corresponds to zero input frequency.

TERMS RELATED TO AMPLITUDE

Deflection Coefficient. The ratio of the input signal magnitude to the resultant output indication.

NOTE

The ratio may be expressed in terms of volts (rms) per division, decibels per division, watts per division, or any other specified factor.

Display Reference Level. A designated vertical position representing a specified input level.

NOTE

The level may be expressed in decibels (e.g., 1 mW), volts, or any other units.

Sensitivity. Measure of a spectrum analyzer's ability to display minimum level signals, at a given IF bandwidth, display mode, and any other influencing factors, and expressed in decibels (e.g., 1 mW).

Equivalent Input Noise Sensitivity. The average level of a spectrum analyzer's internally generated noise referenced to the input.

Display Flatness. The unwanted variation of the displayed amplitude over a specified frequency span, expressed in decibels.

Relative Display Flatness. The display flatness measured relative to the display amplitude at a fixed frequency within the frequency span, expressed in decibels.

NOTE

Display flatness is closely related to frequency response. The main difference is that the spectrum display is not recentered.

Frequency Response. The unwanted variation of the displayed amplitude over a specified center frequency range, measured at the center frequency, expresed in decibels.

Display Law. The mathematical law that defines the input-output function of the instrument.

NOTE

The following cases apply:

1) Linear—A display in which the scale divisions are a linear function of the input signal voltage;

2) Square law (power)—A display in which the scale divisions are a linear function of the input signal power;

3) Logarithmic—A display in which the scale divisions are a logarithmic function of the input signal voltage.

Dynamic Range. The maximum ratio of the levels of two signals simultaneously present at the input which can be measured to a specified accuracy.

Display Dynamic Range. The maximum ratio of the levels of two non-harmonically related sinusoidal signals each of which can be simultaneously measured on the screen to a specified accuracy.

Gain Compression. Maximum input level where the scale linearity error is below that specified.

Spurious Response. A response of a spectrum analyzer wherein the displayed frequency does not conform to the input frequency.

Hum Sidebands. Undesired responses created within the spectrum analyzer, appearing on the display, that are separated from the desired response by the fundamental or harmonic of the power line frequency.

Noise Sidebands. Undesired response caused by noise internal to the spectrum analyzer appearing on the display around a desired response.

Residual Response. A spurious response in the absence of an input signal. (Noise and zero pip are excluded.)

Input Impedance.. The impedance at the desired input terminal.

NOTE

Usually expressed in terms of VSWR, return loss, or other related terms for low impedance devices and resistance-capacitance parameters for high impedance devices.

TERMS RELATED TO DIGITAL STORAGE FOR SPECTRUM ANALYZERS

Digitally Stored Display.. A display method whereby the displayed function is held in a digital memory. The display is generated by reading the data out of memory.

Digitally Averaged Display. A display of the average value of digitized data computed by combining serial samples in a defined manner.

Multiple Display Memory. A digitally stored display having multiple memory sections which can be displayed separately or simultaneously.

Clear (Erase). Presets memory to a prescribed state, usually that denoting zero.

Save. A function which inhibits storage update, saving existing data in a section of a multiple memory (e.g., Save A).

View (Display). Enables viewing of contents of the chosen memory section (e.g., "View A" displays the contents of memory A; "View B" displays the contents of memory B).

Max Hold (Peak Mode). Digitally stored display mode which, at each frequency address, compares the incoming signal level to the stored level and retains the greater. In this mode, the display indicates the peak level at each frequency after several successive sweeps.

Scan Address. A number representing each horizontal data position increment on a directed beam type display. An address in a memory is associated with each scan address.

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

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MANUAL CHANGE INFORMATION

Date: 12-22-82 Change Reference: M47515

Product: 496/496P Spectrum Analyzer Manual Part No.: 070-3481-01

DESCRIPTION

TEXT CHANGES

SECTION 4, MAINTENANCE ADJUSTMENTS, 1st LO Phase Lock Calibration, page 4-20

Replace step 5 with the following and change step 5 to step 6:

5. Check Strobe Driver - Excessive noise on the display and intermittent lock are indications that the strobe pulse out of the Strobe Driver is noisy or low in amplitude. This can be caused by a mismatch in input or output impedance to the band-pass filter FL 2064. The following procedure is required if the filter or any component that affects the input or ouput impedance match is replaced.

a. With the instrument in phase lock mode, connect a test oscilloscope probe to TP 2087. Note the amplitude of the 5 MHz strobe signal. Amplitude of the sinusodial strobe signal is normally 5 to 6 volt peak-to-peak.

b. If the strobe signal amplitude is low and noisy, change the value of select capacitors C1032 and C2105 to obtain the maximum strobe pulse amplitude at TP 2087. Value of these capacitors range from 3.3 to 27 pF.

c. If the signal amplitude is still low, connect frequency counter probe to TP 2015. Frequency must range from 5.0067 to 5.0188 MHz. Frequency is a function of the Controlled Oscillator assembly and counter U1022.

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MANUAL CHANGE INFORMATION

Date: 2-1-83 Change Reference: M43880

Product: 496/496P Spectrum Analyzer Serv. Vol. 1 Manual Part No.: 070-3481-00

DESCRIPTION

TEXT CHANGES

SECTION 3, CALIBRATION, Adjustment Procedure, page 3-47, increment steps 6 thru 8 by 1.

ADD new step 6:

6. Max Span Dot (offset to align dot with display).
   a. Remove 50Ω cable from 496 RF INPUT.
   b. Set 496 CENTER FREQUENCY to exactly 0 MHz, AUTO RESOLUTION pushbutton on, FREQ SPAN to MAX, and VIEW A and VIEW B both OFF.
   c. Select R1028 on the YIG Driver board to set the MAX SPAN dot on the start spur.

NOTE

A larger resistor will move the dot to the right; a smaller resistor will move it to the left. A 1K change in resistance will move the dot approximately one minor division.

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